LTC3878
Fast, Wide Operating Range
No RSENSE Step-Down
DC/DC Controller

FEATURES
- Wide VIN Range: 4V to 38V
- ±1% 0.8V Voltage Reference
- Extremely Fast Transient Response
- tON(MIN): 43ns
- No RSENSE™ Valley Current Mode Control
- Stable with Low ESR Ceramic COUT
- Supports Smooth Start-Up Into Pre-Biased Output
- Optimized for High Step-Down Ratios
- Pin Compatible with the LTC1778 (No EXTVCC Pin)
- Power Good Output Voltage Monitor
- Dual N-Channel MOSFET Synchronous Drive
- Adjustable Switching Frequency
- Programmable Current Limit with Foldback
- Output Overvoltage Protection
- Small 16-Pin Narrow SSOP Package

APPLICATIONS
- Distributed Power Systems
- Embedded Computing
- Communications Infrastructure

DESCRIPTION
The LTC®3878 is a synchronous step-down switching DC/DC controller optimized for high switching frequency and fast transient response. The constant on-time valley current mode architecture allows for a wide input range, including very low duty factor operation. No external sense resistor or slope compensation is required. The LTC3878 is pin compatible with the LTC1778 in applications that do not use ETVCC while offering better efficiency. Consult with the factory to verify compatibility.

Operating frequency is set by an external resistor and compensated for variations in VIN to offer excellent line stability. Discontinuous mode operation provides high efficiency during light load conditions. A forced continuous control pin allows the user to reduce noise and RF interference. Safety features include output overvoltage protection and programmable current limit with foldback. Soft-start capability for supply sequencing is accomplished through an external timing capacitor. The current limit is user programmable.

The LTC3878 allows operation from 4V to 38V at the input and from 0.8V to 90% VIN at the output. The LTC3878 is available in a small 16-pin narrow SSOP package.

TYPICAL APPLICATION

High Efficiency Step-Down Converter

Efficiency vs Load Current

Efficiency (%) vs Load Current (A)

VIN = 12V
VOUT = 1.2V
SW FREQ = 400kHz
FIGURE 7 CIRCUIT
**LTC3878**

**ABSOLUTE MAXIMUM RATINGS**

(Note 1)

- Input Supply Voltage ($V_{IN}$)................. $-0.3V$ to $40V$
- $I_{ON}$ Voltage........................................ $-0.3V$ to $40V$
- $Boost$ Voltage ........................................ $-0.3V$ to $46V$
- SW Voltage ............................................. $-5V$ to $40V$
- $INTVCC$, (Boost-SW), RUN/SS, PGOOD Voltages................................. $-0.3V$ to $6V$
- FCB, $V_{RING}$ Voltages........................................ $-0.3V$ to $INTVCC + 0.3V$
- $V_{FB}$, $I_{TH}$ Voltages...................................... $-0.3V$ to $2.7V$
- Operating Temperature Range (Note 4).......... $-40°C$ to $85°C$
- Junction Temperature (Note 2)...................... $125°C$
- Storage Temperature Range......................... $-65°C$ to $150°C$
- Lead Temperature (Soldering, 10 sec)............. $300°C$

**PIN CONFIGURATION**

**ORDER INFORMATION**

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<td>LTC3878EGN#TRPBF</td>
<td>3878</td>
<td>16-Lead Plastic SSOP</td>
<td>$-40°C$ to $85°C$ (Note 4)</td>
</tr>
<tr>
<td>LTC3878IGN#PBF</td>
<td>LTC3878IGN#TRPBF</td>
<td>3878</td>
<td>16-Lead Plastic SSOP</td>
<td>$-40°C$ to $85°C$ (Note 4)</td>
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Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

**ELECTRICAL CHARACTERISTICS**

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. $V_{IN} = 15V$ unless otherwise noted.

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<tr>
<td>$I_Q$</td>
<td>Input DC Supply Current Normal Shutdown Supply Current</td>
<td>$I_{TH} = 1.2V$ (Note 3)</td>
<td>$0.792 \pm 0.8 \pm 0.808$</td>
<td>$V$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{FBREF}$</td>
<td>Feedback Reference Voltage</td>
<td>$V_{IN} = 4V$ to $38V$, $I_{TH} = 1.2V$ (Note 3)</td>
<td>$0.002$</td>
<td>$% / V$</td>
<td></td>
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<tr>
<td>$I_{FB}$</td>
<td>Feedback Voltage Line Regulation $I_{TH} = 0.5V$ to $1.9V$ (Note 3)</td>
<td>$-0.05 \pm 0.03$</td>
<td>$%$</td>
<td></td>
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<tr>
<td>$I_{FB}$</td>
<td>Feedback Input Current</td>
<td>$V_{FB} = 0.8V$</td>
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<td></td>
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<tr>
<td>$\theta_{M(EA)}$</td>
<td>Error Amplifier Transconductance</td>
<td>$I_{TH} = 1.2V$ (Note 3)</td>
<td>$1.4 \pm 1.7 \pm 2$</td>
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<tr>
<td>$V_{FCB}$</td>
<td>FCB Threshold</td>
<td>$V_{FCB} = 0.8V$</td>
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<tr>
<td>$I_{ON}$</td>
<td>On-Time</td>
<td>$I_{ON} = 30 \mu A$</td>
<td>$198 \pm 233 \pm 268$</td>
<td>$ns$</td>
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<tr>
<td>$I_{ON}$</td>
<td>Minimum On-Time</td>
<td>$I_{ON} = 15 \mu A$</td>
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<td>$ns$</td>
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<tr>
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<td>Minimum On-Time</td>
<td>$I_{ON} = 180 \mu A$</td>
<td>$43 \pm 75$</td>
<td>$ns$</td>
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# ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$, $V_IN = 15V$ unless otherwise noted.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
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<td>Minimum Off-Time</td>
<td>$I_{ON} = 30\mu A$</td>
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<tr>
<td>$V_{SENSE(MAX)}$</td>
<td>Valley Current Sense Threshold</td>
<td>$V_{RNG} = 1V$, $V_{FB} = 0.76V$</td>
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<td></td>
<td>Peak Current = Valley + Ripple</td>
<td>$V_{RNG} = 0V$, $V_{FB} = 0.76V$</td>
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<tr>
<td></td>
<td></td>
<td>$V_{RNG} = INTV_{CC}$, $V_{FB} = 0.76V$</td>
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<td>$V_{SENSE(MIN)}$</td>
<td>Minimum Current Sense Threshold</td>
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<tr>
<td></td>
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<td>$V_{RNG} = 0V$, $V_{FB} = 0.84V$</td>
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<tr>
<td></td>
<td></td>
<td>$V_{RNG} = INTV_{CC}$, $V_{FB} = 0.84V$</td>
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<td>$V_{RUN/SS}$ Rising</td>
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<td>$INTV_{CC(UVLO)}$</td>
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<td></td>
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<tr>
<td></td>
<td>BG Driver Pull-Up On-Resistance</td>
<td>BG High</td>
</tr>
<tr>
<td></td>
<td>BG Driver Pull-Down On-Resistance</td>
<td>BG Low</td>
</tr>
<tr>
<td></td>
<td>TG Rise Time</td>
<td>$C_{LOAD} = 3300pF$ (Note 5)</td>
</tr>
<tr>
<td></td>
<td>TG Fall Time</td>
<td>$C_{LOAD} = 3300pF$ (Note 5)</td>
</tr>
<tr>
<td></td>
<td>BG Rise Time</td>
<td>$C_{LOAD} = 3300pF$ (Note 5)</td>
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<td></td>
<td>BG Fall Time</td>
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<td></td>
<td>TG/BG $t_{1D}$</td>
<td>$C_{LOAD} = 3300pF$ Each Driver (Note 5)</td>
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<td>$C_{LOAD} = 3300pF$ Each Driver (Note 5)</td>
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<td>Internal $V_{CC}$ Voltage</td>
<td>$6V &lt; V_{IN} &lt; 38V$</td>
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<td></td>
<td>Internal $V_{CC}$ Load Regulation</td>
<td>$I_{CC} = 0mA$ to $20mA$</td>
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<td>PGOOD Upper Threshold</td>
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<tr>
<td></td>
<td>PGOOD Turn-On Delay</td>
<td>12</td>
</tr>
</tbody>
</table>

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** $T_J$ is calculated from the ambient temperature $T_A$ and power dissipation $P_D$ as follows:

$$T_J = T_A + (P_D \times 110°C/W)$$

**Note 3:** The LTC3878 is tested in a feedback loop that adjusts $V_{FB}$ to achieve a specified error amplifier output voltage ($I_{TH}$).

**Note 4:** The LTC3878E is guaranteed to meet specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3878I is guaranteed to meet specifications over the full –40°C to 85°C operating temperature range.

**Note 5:** Rise and fall time are measured using 10% and 90% levels. Delay times are measured using 50% levels.
TYPICAL PERFORMANCE CHARACTERISTICS

Transient Response FCM (Forced Continuous Mode)

Load Step 0A to 10A to 0A
VIN = 12V
VOUT = 1.2V
FCB = 0V
SW FREQ = 400kHz
FIGURE 7 CIRCUIT

-transient Response FCM Positive Load Step

Load Step 0A to 10A
VIN = 12V
VOUT = 1.2V
FCB = 0V
SW FREQ = 400kHz
FIGURE 7 CIRCUIT

-transient Response FCM Negative Load Step

Load Step 10A to 0A
VIN = 12V
VOUT = 1.2V
FCB = 0V
SW FREQ = 400kHz
FIGURE 7 CIRCUIT

Transient Response DCM (Discontinuous Mode)

Load Step 1A to 11A to 1A
VIN = 12V
VOUT = 1.2V
FCB = INTVCC
SW FREQ = 400kHz
FIGURE 7 CIRCUIT

Normal Start-Up, RUN/SS Release from Zero

VIN = 12V
VOUT = 1.2V
FCB = 0V
SW FREQ = 400kHz
FIGURE 7 CIRCUIT

Start-Up VIN Cycled Low and High

VIN = 12V
VOUT = 1.2V
FCB = 0V
SW FREQ = 400kHz
FIGURE 7 CIRCUIT

Efficiency vs Load Current

CONTINUOUS MODE

DISCONTINUOUS MODE

VIN = 12V
VOUT = 1.2V
SW FREQ = 400kHz
FIGURE 7 CIRCUIT

Efficiency vs Input Voltage

VOUT = 1.2V
SW FREQ = 400kHz
FIGURE 7 CIRCUIT

Frequency vs Input Voltage

VIN = 12V
VOUT = 1.2V
FIGURE 7 CIRCUIT
TYPICAL PERFORMANCE CHARACTERISTICS

Frequency vs Load Current

- CONTINUOUS MODE
- DISCONTINUOUS MODE

Load Regulation FCM

\( V_{\text{IN}} = 15V \)
\( V_{\text{OUT}} = 1.2V \)

Current Sense Voltage vs \( I_{\text{TH}} \) Voltage

On-Time vs \( I_{\text{ON}} \) Current

Current Limit Foldback

\( V_{\text{RING}} = 1V \)

Feedback Reference Voltage vs Temperature

\( V_{\text{RING}} = 0.2V \)
\( V_{\text{RING}} = 0.5V \)
\( V_{\text{RING}} = 0.8V \)
\( V_{\text{RING}} = 1.0V \)
\( V_{\text{RING}} = 1.5V \)
\( V_{\text{RING}} = 1.8V \)
\( V_{\text{RING}} = 2.0V \)
PIN FUNCTIONS

RUN/SS (Pin 1): Run Control and Soft-Start Input. A capacitor to ground on this pin sets the ramp time to full output current (approximately 3s/µF) when RUN/SS is open. The switching outputs are disabled when below 1.5V. The device is in micropower shutdown when under 0.7V. If left open, there is an internal 1.2µA pull-up current on RUN/SS. INTVCC is enabled when RUN/SS exceeds 0.7V.

PGOOD (Pin 2): Power Good Output. This open-drain logic output is pulled to ground when the output voltage is outside of a ±7.5% window around the regulation point.

VRNG (Pin 3): VDS Sense Voltage Range Input. The maximum allowed bottom MOSFET VDS sense voltage between SW and PGND is equal to (0.133)VRNG. The voltage applied to VRNG can be any value between 0.2V and 2V. If VRNG is tied to SGND, the device operates with a maximum valley current sense threshold of 93mV typical. If VRNG is tied to INTVCC, the device operates with a maximum valley current sense threshold of 186mV typical.

FCB (Pin 4): Forced Continuous Input. Connect this pin to INTVCC to enable discontinuous mode for light load operation. Connect this pin to SGND to force continuous mode operation in all conditions.

ITH (Pin 5): Current Control Threshold and Error Amplifier Compensation Point. The current comparator threshold increases with this control voltage. The voltage ranges from 0V to 2.4V, with 0.8V corresponding to zero sense voltage (zero current).

SGND (Pin 6): Signal Ground. All small-signal components should be connected to SGND. Connect SGND to PGND using a single PCB trace.

ION (Pin 7): On-Time Current Input. Tie a resistor from VIN to this pin to set the one-shot timer current and thus the switching frequency.

VFB (Pin 8): Error Amplifier Feedback Input. This pin connects the error amplifier to an external resistive divider from VOUT.

NC (Pin 9): For factory use only. Can be connected to any voltage equal to or less than INTVCC.

VIN (Pin 10): Main Input Supply. The supply voltage can range from 4V to 38V. For increased noise immunity decouple this pin to PGND with an RC filter.

INTVCC (Pin 11): Internal 5.3V Regulator Output. The driver and control circuits are powered from this voltage. Decouple this pin to PGND with a minimum of 1µF, 10V X5R or X7R ceramic capacitor.

BG (Pin 12): Bottom Gate Drive. This pin drives the gate of the bottom N-Channel power MOSFET between PGND and INTVCC.

PGND (Pin 13): Power Ground. Connect this pin as close as practical to the source of the bottom N-channel power MOSFET, the (–) terminal of CINTVCC and the (–) terminal of CVIN.

SW (Pin 14): Switch Node. The (–) terminal of the bootstrap capacitor, CB, connects to this node. This pin swings from a diode voltage below ground up to VIN.

TG (Pin 15): Top Gate Drive. This pin drives the gate of the top N-channel power MOSFET between SW and BOOST.

BOOST (Pin 16): Boosted Floating Driver Supply. The (+) terminal of the bootstrap capacitor, CB, connects to this node. This node swings from (INTVCC − VSHOTTKY) to VIN + (INTVCC − VSHOTTKY).
LTC1778 Compatibility

The LTC3878 is compatible with the LTC1778 in applications which do not use the EXTVC\textsubscript{CC} function. The LTC3878 offers improved gate drive and reduced dead time, which allows higher efficiency than the LTC1778. On the LTC1778 Pin 9 is EXTVC\textsubscript{CC}, but on the LTC3878 it is a no connect. The other notable difference is that the shutdown latch-off timer is removed. The LTC3878 should be a drop in, pin-for-pin replacement in most applications that do not use EXTVC\textsubscript{CC}. The LTC3878 should be tested and verified in each application without assuming compatibility. Contact a Linear applications expert to answer any questions regarding LTC3878/LTC1778 compatibility.

Main Control Loop

The LTC3878 is a valley current mode controller IC for use in DC/DC step-down converters. In normal continuous operation, the top MOSFET is turned on for a fixed interval determined by a one-shot timer, OST. When the top MOSFET is turned off, the bottom MOSFET is turned on until the current comparator, I\textsubscript{CMP}, trips, restarting the one-shot timer and initiating the next cycle. Inductor valley current is measured by sensing the voltage between the PGND and SW pins using the bottom MOSFET on-resistance. The voltage on the \textit{I}_{TH} pin sets the comparator threshold corresponding to inductor valley current. The error amplifier EA adjusts this voltage by comparing the feedback signal V\textsubscript{FB} from the output voltage to the feedback reference voltage V\textsubscript{FBREF}. Increasing the load current causes a drop in the feedback voltage relative to the reference. The EA senses the feedback voltage drop and adjusts the \textit{I}_{TH} voltage higher until the average inductor current matches the load current.

With DC current loads less than 1/2 of the peak-to-peak ripple the inductor current can drop to zero or become negative. In discontinuous operation, negative inductor current is detected and prevented by the current reversal comparator \textit{I}_{REV}, which shuts off MB. Both switches remain off with the output capacitor supplying the load current until the EA moves the \textit{I}_{TH} voltage above the zero current level (0.8V) to initiate another switching cycle. When the FCB (forced continuous bar) pin is below the internal FCB threshold reference, V\textsubscript{FCB}, the regulator is forced to operate in continuous mode by disabling reversal comparator, \textit{I}_{REV}, thereby allowing the inductor current to become negative.

The continuous mode operating frequency can be determined by dividing the calculated duty cycle, \textit{V}_{OUT}/\textit{V}_{IN}, by the fixed on-time. The OST generates an on-time proportional to the ideal duty cycle, thus holding the frequency approximately constant with changes in \textit{V}_{IN}. The nominal frequency can be adjusted with an external resistor, R\textsubscript{ON}.

Foldback current limiting is provided to protect against low impedance shorts. If the controller is in current limit and \textit{V}_{OUT} drops to less 50% of regulation, the current limit set-point “folds back” to progressively lower values. To recover from foldback current limit, the excessive load or low impedance short needs to be removed.

Pulling the RUN/SS pin low forces the controller into its shutdown state, turning off both MT and MB. Releasing the pin allows an internal 1.2\textmu{A} current source to charge up an external soft-start capacitor, C\textsubscript{SS}. When the RUN/SS pin is less than 0.7V, the device is in the low power shutdown condition with a nominal bias current of 18\textmu{A}. When RUN/SS is greater than 0.7V and less than 1.5V, INTV\textsubscript{CC} and all internal circuitry are enabled while MT and MB are forced off. Current-limited soft-start begins when RUN/SS exceeds 1.5V. Normal operation at full current limit is achieved at approximately 3V on RUN/SS. Foldback current limit is defeated during soft-start.
The basic LTC3878 application circuit is shown on the first page of this data sheet. External component selection is largely determined by maximum load current and begins with the selection of sense resistance and power MOSFET switches. The LTC3878 uses the on-resistance of the synchronous power MOSFET to determine the inductor current. The desired ripple current and operating frequency largely determines the inductor value. Finally, C_{IN} is selected for its ability to handle the large RMS current into the converter, and C_{OUT} is chosen with low enough ESR to meet output voltage ripple and transient specifications.

**Maximum \( V_{DS} \) Sense Voltage and \( V_{RNG} \) Pin**

Inductor current is measured by sensing the bottom MOSFET \( V_{DS} \) voltage that appears between the PGND and SW pins. The maximum allowed \( V_{DS} \) sense voltage is set by the voltage applied to the \( V_{RNG} \) pin and is approximately equal to \((0.133)V_{RNG}\). The current mode control loop does not allow the inductor current valleys to exceed \((0.133)V_{RNG}\). In practice, one should allow margin, to account for variations in the LTC3878 and external component values. A good guide for setting \( V_{RNG} \) is:

\[
V_{RNG} = 7.5 \times (\text{Maximum } V_{DS} \text{ Sense Voltage})
\]

An external resistive divider from \( INTV_{CC} \) can be used to set the voltage on the \( V_{RNG} \) pin between 0.2V and 2V, resulting in peak sense voltages between 26.6mV and 266mV. The wide peak voltage sense range allows for a variety of applications and MOSFET choices. The \( V_{RNG} \) pin can also be tied to either SGND or \( INTV_{CC} \) to force internal defaults. When \( V_{RNG} \) is tied to SGND, the device operates at a valley current sense threshold of 93mV typical. If \( V_{RNG} \) is tied to \( INTV_{CC} \), the device operates at a valley current sense threshold of 186mV typical.

**Power MOSFET Selection**

The LTC3878 requires two external N-channel power MOSFETs, one for the top (main) switch and one for the bottom (synchronous) switch. Important parameters for the power MOSFETs are the breakdown voltage \( V_{BR(DSS)} \), threshold voltage \( V_{GS(TH)} \), on-resistance \( R_{DS(ON)} \), reverse transfer capacitance \( C_{RSS} \) and maximum current \( I_{DS(MAX)} \).

The gate drive voltages are set by the 5.3V \( INTV_{CC} \) supply. Consequently, logic-level threshold MOSFETs must be used in LTC3878 applications. If the input voltage is expected to drop below 5V, then sub-logic level threshold MOSFETs should be considered.

Using the bottom MOSFET as the current sense element requires particular attention be paid to its on-resistance. MOSFET on-resistance is typically specified with a maximum value \( R_{DS(ON)(MAX)} \) at 25°C. In this case additional margin is required to accommodate the rise in MOSFET on-resistance with temperature.

\[
R_{DS(ON)(MAX)} = \frac{\text{Max } V_{DS} \text{ Sense Voltage}}{I_{OUT} \times \rho_T}
\]

The \( \rho_T \) term is a normalization factor (unity at 25°C) accounting for the significant variation in on-resistance with temperature, typically about 0.4%/°C, as shown in Figure 1. For a maximum junction temperature of 100°C using a value of \( \rho_T = 1.3 \) is reasonable.

The power dissipated by the top and bottom MOSFETs depends upon their respective duty cycles and the load current. When the LTC3878 is operating in continuous mode, the duty cycles for the MOSFETs are:

\[
D_{TOP} = \frac{V_{OUT}}{V_{IN}} \quad \quad D_{BOT} = \frac{V_{IN} - V_{OUT}}{V_{IN}}
\]

![Figure 1. \( R_{DS(ON)} \) vs Temperature](image-url)
The resulting power dissipation in the MOSFETs at maximum output current are:

\[ P_{\text{TOP}} = D_{\text{TOP}} \cdot I_{\text{OUT(MAX)}}^2 \cdot P_{\tau(TOP)} \cdot R_{\text{DS(ON)(MAX)}} + V_{\text{IN}}^2 \left( \frac{I_{\text{OUT(MAX)}}}{2} \right) (C_{\text{MILLER}}) \]

\[ P_{\text{BOT}} = D_{\text{BOT}} \cdot I_{\text{OUT(MAX)}}^2 \cdot P_{\tau(BOT)} \cdot R_{\text{DS(ON)(MAX)}} \]

\[ D_{\text{TGHIGH}} \text{ is pull-up driver resistance and } D_{\text{TGLOW}} \text{ is the TG driver pull-down resistance. } V_{\text{MILLER}} \text{ is the Miller effect } V_{\text{GS}} \text{ voltage and is taken graphically from the power MOSFET data sheet.} \]

MOSFET input capacitance is a combination of several components but can be taken from the typical “gate charge” curve included on the most data sheets (Figure 2). The curve is generated by forcing a constant input current into the gate of a common source, current source, loaded stage and then plotting the gate versus time. The initial slope is the effect of the gate-to-source and gate-to-drain capacitance. The flat portion of the curve is the result of the Miller multiplication effect of the drain-to-gate capacitance as the drain drops the voltage across the current source load. The upper sloping line is due to the drain-to-gate accumulation capacitance and the gate-to-source capacitance. The Miller charge (the increase in coulombs on the horizontal axis from a to b while the curve is flat) is specified from a given \( V_{\text{DS}} \) drain voltage, but can be adjusted for different \( V_{\text{DS}} \) voltages by multiplying by the ratio of the application \( V_{\text{DS}} \) to the curve specified \( V_{\text{DS}} \) values. A way to estimate the \( C_{\text{MILLER}} \) term is to take the change in gate charge from points a and b or the parameter \( Q_{\text{GD}} \) on a manufacturer’s data sheet and divide by the specified \( V_{\text{DS}} \) test voltage, \( V_{\text{DS(TEST)}} \).

\[ C_{\text{MILLER}} = \frac{Q_{\text{GD}}}{V_{\text{DS(TEST)}}} \]

\( C_{\text{MILLER}} \) is the most important selection criteria for determining the transition loss term in the top MOSFET but is not directly specified on MOSFET data sheets.

Both MOSFETs have \( I^2R \) power loss, and the top MOSFET includes an additional term for transition loss, which are highest at high input voltages. For \( V_{\text{IN}} < 20V \), the high current efficiency generally improves with larger MOSFETs, while for \( V_{\text{IN}} > 20V \), the transition losses rapidly increase to the point that the use of a higher \( R_{\text{DS(ON)}} \) device with lower \( C_{\text{MILLER}} \) actually provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage when the top switch duty factor is low or during a short-circuit when the synchronous switch is on close to 100% of the period.

Operating Frequency

The choice of operating frequency is a tradeoff between efficiency and component size. Lowering the operating frequency improves efficiency by reducing MOSFET switching losses but requires larger inductance and/or capacitance to maintain low output ripple voltage. Conversely, raising the operating frequency degrades efficiency but reduces component size.

The operating frequency of LTC3878 applications is determined implicitly by the one-shot timer that controls the on-time, \( t_{\text{ON}} \), of the top MOSFET switch. The on-time is set by the current into the \( I_{\text{ON}} \) pin according to:

\[ t_{\text{ON}} = \frac{0.7V}{I_{\text{ON}} \cdot (10pF)} \]

Tying a resistor \( R_{\text{ON}} \) from \( V_{\text{IN}} \) to the \( I_{\text{ON}} \) pin yields an on-time inversely proportional to \( V_{\text{IN}} \). For a step-down converter, this results in pseudo fixed frequency operation as the input supply varies.

\[ f_{\text{OP}} = \frac{V_{\text{OUT}}}{0.7V \cdot R_{\text{ON}} \cdot (10pF)} \text{ [Hz]} \]
Figure 3 shows how \( R_{ON} \) relates to switching frequency for several common output voltages.

When designing for pseudo fixed frequency, there is systematic error because the \( I_{ON} \) pin voltage is approximately 0.7V, not zero. This causes the \( I_{ON} \) current to be inversely proportional to \( (V_{IN} - 0.7V) \) and not \( V_{IN} \). The \( I_{ON} \) current error increases as \( V_{IN} \) decreases. To correct this error, an additional resistor \( R_{ON2} \) can be connected from the \( I_{ON} \) pin to the 5.3V INTVCC supply.

\[
R_{ON2} = \frac{5.3V - 0.7V}{0.7V} R_{ON}
\]

Likewise, the maximum frequency of operation is determined by the fixed on-time, \( t_{ON} \), and the minimum off-time, \( t_{OFF(MIN)} \). The fixed on-time is determined by dividing the duty factor by the nominal frequency of operation:

\[
f_{MAX} = \frac{1}{\frac{V_{OUT}}{V_{IN} \cdot f_{OP}} + t_{OFF(MIN)}} \quad [\text{Hz}]
\]

The LTC3878 is a PFM (pulse frequency mode) regulator where pulse density is modulated, not pulse width. Consequently, frequency increases with a load step and decreases with a load release. The steady-state operating frequency, \( f_{OP} \), should be set sufficiently below \( f_{MAX} \) to allow for device tolerances and transient response.

**Inductor Value Calculation**

Given the desired input and output voltages, the inductor value and operation frequency determine the ripple current:

\[
\Delta I_L = \left( \frac{V_{OUT}}{f_{OP} \cdot L} \right) \left( 1 - \frac{V_{OUT}}{V_{IN}} \right)
\]

Lower ripple current reduces core losses in the inductor, ESR losses in the output capacitors and output voltage ripple. Highest efficiency operation is obtained at low frequency with small ripple current. However, achieving this requires a large inductor. There is a trade-off between component size, efficiency and operating frequency.
A reasonable starting point is to choose a ripple current that is about 40% of I_{OUT(MAX)}. The largest ripple current occurs at the highest V_{IN}. To guarantee that ripple current does not exceed a specified maximum, the inductance should be chosen according to:

\[
L = \left( \frac{V_{OUT}}{f_{OP} \cdot \Delta I_{L(MAX)}} \right) \left( 1 - \frac{V_{OUT}}{V_{IN(MAX)}} \right)
\]

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot tolerate the core loss of low cost powdered iron cores, forcing the use of more expensive ferrite materials such as molypermalloy or Kool Mu cores. A variety of inductors designed for high current, low voltage applications are available from manufacturers such as Sumida, Panasonic, Coiltronics, Coilcraft, Toko, Vishay, Pulse and Wurth.

**Inductor Core Selection**

Once the inductance value is determined, the type of inductor must be selected. Core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates “hard,” which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

**C_{IN} and C_{OUT} Selection**

The input capacitance C_{IN} is required to filter the square wave current at the drain of the top MOSFET. Use a low ESR capacitor sized to handle the maximum RMS current.

\[
I_{RMS} \equiv I_{OUT(MAX)} \cdot \frac{V_{OUT}}{V_{IN}} \cdot \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}
\]

This formula has a maximum at V_{IN} = 2V_{OUT}, where I_{RMS} = I_{OUT(MAX)}/2. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life, which makes it advisable to de-rate the capacitor.

The selection of C_{OUT} is primarily determined by the ESR required to minimize voltage ripple and load step transients. The \(\Delta V_{OUT}\) is approximately bounded by:

\[
\Delta V_{OUT} \leq \Delta I_L \left( \frac{ESR + \frac{1}{8 \cdot f_{OP} \cdot C_{OUT}}}{} \right)
\]

Since \(\Delta I_L\) increases with input voltage, the output ripple is highest at maximum input voltage. Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering and has the necessary RMS current rating.

Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, specialty polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Specialty polymer capacitors offer very low ESR but have lower specific capacitance than other types. Tantalum capacitors have the highest specific capacitance but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR, but can be used in cost-sensitive applications providing that consideration is given to ripple current ratings and long-term reliability. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing. When used as input capacitors, care must be taken to ensure that ringing from inrush currents and switching does not pose an overvoltage hazard to the power switches and controller. To dampen input voltage transients, add a small 5\(\mu\)F to 40\(\mu\)F aluminum electrolytic capacitor with an ESR in the range of 0.5\(\Omega\) to 2\(\Omega\). High performance though-hole capacitors may also be used, but an additional ceramic capacitor in parallel is recommended to reduce the effect of lead inductance.
Top MOSFET Driver Supply (C_B, D_B)

An external bootstrap capacitor, C_B, connected to the BOOST pin supplies the gate drive voltage for the topside MOSFET. This capacitor is charged through diode D_B from INTV_CC when the switch node is low. When the top MOSFET turns on, the switch node rises to VIN and the BOOST pin rises to approximately VIN + INTV_CC. The boost capacitor needs to store approximately 100 times the gate charge required by the top MOSFET. In most applications 0.1μF to 0.47μF, X5R or X7R dielectric capacitor is adequate.

It is recommended that the BOOST capacitor be no larger than 10% of the INTV_CC capacitor C_VCC, to ensure that the C_VCC can supply the upper MOSFET gate charge and BOOST capacitor under all operating conditions. Variable frequency in response to load steps offers superior transient performance but requires higher instantaneous gate drive. Gate charge demands are greatest in high frequency low duty factor applications under high di/dt load steps and at start-up.

Setting Output Voltage

The LTC3878 output voltage is set by an external feedback resistive divider carefully placed across the output, as shown in Figure 5. The regulated output voltage is determined by:

\[ V_{OUT} = 0.8V \left(1 + \frac{R_B}{R_A}\right) \]

To improve the transient response, a feed-forward capacitor, C_FF, may be used. Great care should be taken to route the V_FB line away from noise sources, such as the inductor or the SW line.

Discontinuous Mode Operation and FCB Pin

The FCB (forced continuous bar) pin determines whether the LTC3878 operates in forced continuous mode or allows discontinuous conduction mode. Tying this pin above 0.8V enables discontinuous operation, where the bottom MOSFET turns off when the inductor current reverses polarity. The load current at which current reverses and discontinuous operation begins depends on the amplitude of the inductor ripple current and will vary with changes in VIN. In steady-state operation, discontinuous conduction mode occurs for DC load currents less than 1/2 the peak-to-peak ripple current. Tying the FCB pin below the 0.8V threshold forces continuous switching, where inductor current is allowed to reverse at light loads and maintain synchronous switching.

In addition to providing a logic input to force continuous operation, the FCB pin provides a means to maintain a fly back winding output when the primary is operating in discontinuous mode. The secondary output VOUT2 is normally set as shown in Figure 6 by the turns ratio N of the transformer. However, if the controller goes into discontinuous mode and halts switching due to a light primary load current, then VOUT2 will droop. An external resistor divider from VOUT2 to the FCB pin sets a minimum voltage VOUT2(MIN) below which continuous operation is forced until VOUT2 has risen above its minimum.

\[ V_{OUT2(MIN)} = 0.8V \left(1 + \frac{R_4}{R_3}\right) \]
Fault Conditions: Current Limit and Foldback

The maximum inductor current is inherently limited in a current mode controller by the maximum sense voltage. In the LTC3878, the maximum sense voltage is controlled by the voltage on the VRNG pin. With valley current mode control, the maximum sense voltage and the sense resistance determine the maximum allowed inductor valley current. The corresponding output current limit is:

\[
I_{\text{LIMIT}} = \frac{V_{\text{SNS(MAX)}}}{R_{\text{DS(ON)}}} \cdot PT + \frac{1}{2} \cdot \Delta I_L
\]

The current limit value should be checked to ensure that \( I_{\text{LIMIT(MIN)}} > I_{\text{OUT(MAX)}} \). The current limit value should be greater than the inductor current required to produce maximum output power at the worst-case efficiency. Worst-case efficiency typically occurs at the highest \( V_{\text{IN}} \) and highest ambient temperature. It is important to check for consistency between the assumed MOSFET junction temperatures and the resulting value of \( I_{\text{LIMIT}} \) which heats the MOSFET switches.

Caution should be used when setting the current limit based on the \( R_{\text{DS(ON)}} \) of the MOSFETs. The maximum current limit is determined by the minimum MOSFET on-resistance. Data sheets typically specify nominal and maximum values for \( R_{\text{DS(ON)}} \) but not a minimum. A reasonable assumption is that the minimum \( R_{\text{DS(ON)}} \) lies the same amount below the typical value as the maximum lies above it. Consult the MOSFET manufacturer for further guidelines.

To further limit current in the event of a short circuit to ground, the LTC3878 includes foldback current limiting. If the output falls by more than 50%, then the maximum sense voltage is progressively lowered to about one-sixth of its full value.

INTVCC Regulator

An internal P-channel low dropout regulator produces the 5.3V supply that powers the drivers and internal circuitry within the LTC3878. The INTVCC pin can supply up to 50mA RMS and must be bypassed to ground with a minimum of 1µF low ESR tantalum or ceramic capacitor (10V, X5R or X7R). Output capacitance greater than 10µF is discouraged. Good bypassing is necessary to supply the high transient currents required by the MOSFET gate drivers.

Applications using large MOSFETs with a high input voltage and high frequency of operation may cause the LTC3878 to exceed its maximum junction temperature rating or RMS current rating. In continuous mode operation, this current is \( I_{\text{GATECHG}} = f_{\text{OP}}(Q_{\text{G(TOP)}} + Q_{\text{G(BOT)}}) \). The junction temperature can be estimated from the equations given in Note 2 of the Electrical Characteristics. For example, with a 30V input supply, the LTC3878 is limited to less than 16.5mA:

\[
T_J = 70°C + (16.5mA)(30)(110°C/W) = 125°C
\]

Using the INTVCC regulator to supply external loads greater than 5mA is discouraged. INTVCC is designed to supply the LTC3878 with minimal external loading. When using the regulator to supply larger external loads, carefully consider all operating load conditions. During load steps and soft-start, transient current requirements significantly exceed the RMS values. Additional loading on INTVCC takes away from the drive available to source gate charge during high frequency transient load steps.

Soft-Start with the RUN/SS Pin

The RUN/SS pin both enables the LTC3878 and provides a means of programmable current limited soft-start. Pulling the RUN/SS pin below 0.7V puts the LTC3878 into a low quiescent current shutdown (\( I_Q < 15\muA \)). Releasing the pin allows an internal 1.2µA current source to charge up the external timing capacitor \( C_{SS} \). If RUN/SS has been pulled all the way to ground, there is a delay before starting. This delay is created by charging \( C_{SS} \) from ground to 1.5V through a 1.2µA current source.

\[
t_{\text{DELAY}} = \frac{1.5V}{1.2\mu A} \cdot C_{SS} = (1.3s/\mu F) C_{SS}
\]

When the voltage on RUN/SS reaches 1.5V, the LTC3878 begins to switch. \( I_{\text{TH}} \) is clamped to be no greater than RUN/SS – 0.6V, and the device begins switching when \( I_{\text{TH}} \) exceeds 0.9V. As the RUN/SS voltage rises to 3V, the clamp on \( I_{\text{TH}} \) increases until it reaches the full-scale 2.4V limit after an additional delay of 1.3s/µF. During this time, the soft-start current limit is set to:

\[
I_{\text{LIMIT(SS)}} = I_{\text{LIMIT}} \cdot \frac{(\text{RUN/SS} – 0.6V) – 0.8V}{2.4V – 0.8V}
\]
Applications Information

Regulator output current is negative when \(I_{TH}\) is between 0V and 0.8V and positive when \(I_{TH}\) is between 0.8V and the maximum full-scale set-point of 2.4V. In normal operating conditions the RUN/SS pin will continue to charge positive until the voltage is equal to INTVCC.

**INTVCC Undervoltage Lockout**

Whenever INTVCC drops below approximately 3.4V, the device enters undervoltage lockout (UVLO). In a UVLO condition, the switching outputs TG and BG are disabled. At the same time, the RUN/SS pin is pulled down from INTVCC to 0.8V with a 3µA current source. When the INTVCC UVLO condition is removed, RUN/SS ramps from 0.8V and begins a normal current limited soft-start. This feature is important when regulator start-up is not initiated by applying a logic drive to RUN/SS. Soft-start from INTVCC UVLO release greatly reduces the possibility for start-up oscillations caused by the regulator starting up at INTVCC(UVLR) and then shutting down at INTVCC(UVLO) due to inrush current.

**Efficiency Considerations**

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Although all dissipative elements in the circuit produce losses, four main sources account for most of the losses in LTC3878 circuits.

1. **DC \(I^2R\) losses.** These arise from the resistances of the MOSFETs, inductor and PC board traces and cause the efficiency to drop at high output currents. In continuous mode the average output current flows though the inductor \(L\), but is chopped between the top and bottom MOSFETs. If the two MOSFETs have approximately the same \(R_{DS(ON)}\), then the resistance of one MOSFET can simply by summed with the resistances of \(L\) and the board traces to obtain the DC \(I^2R\) loss. For example, if \(R_{DS(ON)} = 0.01\Omega\) and \(R_L = 0.005\Omega\), the loss will range from 15mW to 1.5W as the output current varies from 1A to 10A.

2. **Transition loss.** This loss arises from the brief amount of time the top MOSFET spends in the saturated region during switch node transitions. It depends upon the input voltage, load current, driver strength and MOSFET capacitance, among other factors. The loss is significant at input voltages above 20V.

3. **INTVCC current.** This is the sum of the MOSFET driver and control currents.

4. **\(C_{IN}\) loss.** The input capacitor has the difficult job of filtering the large RMS input current to the regulator. It must have a very low ESR to minimize the AC \(I^2R\) loss and sufficient capacitance to prevent the RMS current from causing additional upstream losses in fuses or batteries.

Other losses, which include the \(C_{OUT}\) ESR loss, bottom MOSFET reverse recovery loss and inductor core loss generally account for less than 2% additional loss.

When making adjustments to improve efficiency, the input current is the best indicator of changes in efficiency. If you make a change and the input current decreases, then the efficiency has increased. If there is no change in input current there is no change in efficiency.

**Checking Transient Response**

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, \(V_{OUT}\) immediately shifts by an amount equal to \(\Delta I_{LOAD}\) (ESR), where ESR is the effective series resistance of \(C_{OUT}\). \(\Delta I_{LOAD}\) also begins to charge or discharge \(C_{OUT}\), generating a feedback error signal used by the regulator to return \(V_{OUT}\) to its steady-state value. During this recovery time, \(V_{OUT}\) can be monitored for overshoot or ringing that would indicate a stability problem. The \(I_{TH}\) pin external components shown in the Design Example will provide adequate compensation for most applications.

A rough compensation check can be made by calculating the gain crossover frequency, \(f_{GCO}\). \(g_m(EA)\) is the error amplifier transconductance, \(R_C\) is the compensation resistor and feedback divider attenuation is assumed to be 0.8/VOUT. This equation assumes that no feed-forward compensation is used on feedback and that \(C_{OUT}\) sets the dominant output pole.

\[
f_{GCO} = g_m(EA) \cdot R_C \cdot \frac{I_{LIMIT}}{1.6} \cdot \frac{1}{2 \cdot \pi \cdot C_{OUT}} \cdot \frac{0.8}{V_{OUT}}
\]
APPLICATIONS INFORMATION

As a rule of thumb the gain crossover frequency should be less than 20% of the switching frequency. For a detailed explanation of switching control loop theory see Application Note 76.

High Switching Frequency Operation

Special care should be taken when operating at switching frequencies greater than 800kHz. At high switching frequencies there may be an increased sensitivity to PCB noise which may result in off-time variation greater than normal. This off-time instability can be prevented in several ways. First, carefully follow the recommended layout techniques. Second, use 2µF or more of X5R or X7R ceramic input capacitance per Amps of load current. Third, if necessary, increase the bottom MOSFET ripple voltage to 30mVp-p or greater. This ripple voltage is equal to RDS(ON) typical at 25°C • Ip-p.

Design Example

Figure 7 is a power supply design example with the following specifications: VIN = 4.5V to 28V (12V nominal), VOUT = 1.2V ±5%, IOUT(MAX) = 15A and f = 400kHz. Start by calculating the timing resistor, RON:

\[ R_{ON} = \frac{1.2V}{0.7V \times 400kHz \times 10µF} = 429k \]

Select the nearest standard resistor value of 432k for a nominal operating frequency of 396kHz. Set the inductor value to give 35% ripple current at maximum VIN using the adjusted operating frequency:

\[ L = \frac{1.2V}{396kHz \times 0.35 \times 15A} \left( 1 - \frac{1.2V}{28} \right) = 0.55µH \]

Select 0.56µH which is the nearest value.

The resulting maximum ripple current is:

\[ \Delta I_L = \frac{1.2V}{396kHz \times 0.56µH} \left( 1 - \frac{1.2V}{28} \right) = 5.1A \]

Choose the synchronous bottom MOSFET switch and calculate the VRNG current limit set-point. To calculate VRNG and VDS, the \( \rho \tau \) term normalization factor (unity at 25°C) is required to account for variation in MOSFET on-resistance with temperature. Choosing an RJK0330 (RDS(ON) = 2.8mΩ (nominal) 3.9mΩ (maximum), VGS = 4.5V, \( \theta_{JA} = 40°C/W \) yields a drain source voltage of:

\[ V_D = \left( I_{LIMIT} - \frac{1}{2}(I_{RIPPLE}) \right) 3.9mΩ (\rho \tau) \]

Figure 7. Design Example: 1.2V/15A at 400kHz
LTC3878

APPLICATIONS INFORMATION

$V_{\text{RNG}}$ sets current limit by fixing the maximum peak $V_{DS}$ voltage on the bottom MOSFET switch. As a result, the average DC current limit includes significant temperature and component variability. Design to guarantee that the average DC current limit will always exceed the rated operating output current by assuming worst-case component tolerance and temperature.

The worst-case minimum $\text{INTV}_{\text{CC}}$ is 5.15V. The bottom MOSFET worst-case $R_{\text{DS(ON)}}$ is 3.9mΩ and the junction temperature is 80°C above a 70°C ambient with $\rho_{150^\circ\text{C}} = 1.5$. Set $T_{\text{ON}}$ equal to the minimum specification of 15% low and the inductor 15% high.

By setting $I_{\text{LIMIT}}$ equal to 15A we get 79mV for peak $V_{DS}$ voltage which corresponds to a $V_{\text{RNG}}$ equal to 592mV:

$$V_{DS} = \left(15A - \frac{1}{2} \cdot 5.1A \cdot \frac{0.85}{1.15}\right) \frac{3.9mΩ \cdot 1.5}{5.15V} \cdot 1.5$$

$$V_{\text{RNG}} = 7.5 \cdot V_{DS}$$

Verify that the calculated nominal $T_J$ is less than the assumed worst-case $T_J$ in the bottom MOSFET:

$$P_{\text{BOT}} = \frac{28V - 1.2V}{28V} (15A)^2 \cdot 1.5 \cdot 3.9mΩ = 1.25W$$

$$T_J = 70^\circ\text{C} + 1.25W \cdot 40^\circ\text{C/W} = 120^\circ\text{C}$$

Because the top MOSFET is on for a short time, an RJK0305DPB ($R_{\text{DS(ON)}} = 10mΩ$ (nominal) $13mΩ$ (maximum) ($C_{\text{MILLER}} = Q_{\text{C}}/10V = 150pF$, $V_{\text{BOOST}} = 5V$), $V_{\text{GS}} = 4.5V$, $V_{\text{MILLER}} = 3V$, $\theta_{JA} = 40^\circ\text{C/W}$) is sufficient. Checking its power dissipation at current limit with $\rho_{100^\circ\text{C}} = 1.4$:

$$P_{\text{TOP}} = \frac{1.2V}{28V} (15A)^2 \cdot 1.4 \cdot 13mΩ + (28V)^2 \left(\frac{15A}{2}\right)$$

$$\left(150pF\right) \left(\frac{2.5Ω}{5V-3V} + \frac{1.2Ω}{3V}\right) 400kHz$$

$$= 0.18W + 0.58W = 0.65W$$

$$T_J = 70^\circ\text{C} + 0.76W \cdot 40^\circ\text{C/W} = 100^\circ\text{C}$$

The junction temperatures will be significantly less at nominal current, but this analysis shows that careful attention to heat sinking will be necessary.

Select $C_{\text{IN}}$ to give an RMS current rating greater than 4A at 85°C. The output capacitor $C_{\text{OUT1}}$ is chosen for a low ESR of 4.5mΩ to minimize output voltage changes due to inductor ripple current and load steps. The output voltage ripple is given as:

$$\Delta V_{\text{OUT(ripple)}} = \Delta I_{\text{L(MAX)}} (\text{ESR})$$

$$= 5.1 \cdot 4.5mΩ = 23mV$$

However, a 0A to 10A load step will cause an output change of up to:

$$\Delta V_{\text{OUT(STEP)}} = \Delta I_{\text{LOAD}} (\text{ESR})$$

$$= 10A \cdot 4.5mΩ = 45mV$$

Optional 2 × 47µF ceramic output capacitors are included to minimize the effect of ESR and ESL in the output ripple and to improve load step response.

PC Board Layout Checklist

The LTC3878 PC board layout can be designed with or without a ground plane. A ground plane is generally preferred based on performance and noise concerns.

When using a ground plane, use a dedicated ground plane layer. In addition, for high current it is recommended to use a multilayer board to help with heat sinking power components.

- The ground plane layer should have no traces and be as close as possible to the routing layer connecting the power MOSFETs.
- Place LTC3878 Pins 9 to 16 facing the power components. Keep components connected to Pin 1 close to LTC3878 (noise sensitive components).
- Place $C_{\text{IN}}$, $C_{\text{OUT}}$, MOSFETs, $D_{\text{B}}$ and inductor all in one compact area. It may help to have some components on the bottom side of the board.
- Use an immediate via to connect components to the ground plane SGND and PGND of LTC3878. Use several larger vias for power components.
- Use compact switch node (SW) plane to improve cooling of the MOSFETs and to keep EMI down.
APPLICATIONS INFORMATION

- Use planes for $V_{IN}$ and $V_{OUT}$ to maintain good voltage filtering and to keep power losses low.

- Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power component. You can connect the copper areas to any DC net. ($V_{IN}$, $V_{OUT}$, GND or to any other DC rail in your system).

- Place decoupling capacitor $C_{C2}$ next to the $I_{TH}$ and SGND pins with short, direct trace connections.

When laying out a printed circuit board without a ground plane, use the following checklist to ensure proper operation of the controller. These items are illustrated in Figure 7.

- Segregate the signal and power grounds. All small-signal components should return to the SGND pin at one point. SGND and PGND should be tied together underneath the IC and then connect directly to the source of M2.

- Place M2 as close to the controller as possible, keeping the PGND, BG and SW traces short.

- Keep the high dV/dT SW, BOOST and TG nodes away from sensitive small-signal nodes.

- Connect the input capacitor(s), $C_{IN}$, close to the power MOSFETs. This capacitor carries the MOSFET AC current.

- Connect the INTVCC decoupling capacitor $C_{VCC}$ closely to the INTVCC and PGND pins.

- Connect the top driver boost capacitor, $C_B$, closely to the BOOST and SW pins.

- Connect the $V_{IN}$ pin decoupling $C_F$ closely to the $V_{IN}$ and PGND pins.

---

**Figure 8. LTC3878 Layout Diagram Without Ground Plane**
LTC3878

TYPICAL APPLICATIONS

4.5V to 14V Input, 1.2V/20A Output at 300kHz

4.5V to 24V Input, 1.8V/10A Output at 500kHz
**TYPICAL APPLICATIONS**

**4.5V to 32V Input, 1V/5A Output at 250kHz**

**4.5V to 28V Input, 2.5V/5A Output at 500kHz**
Typical Applications

13V to 32V Input, 12V/5A Output at 300kHz

[Diagram of LTC3878 application circuit]
TYPICAL APPLICATIONS

Positive-to-Negative Converter, −5V/5A at 300kHz

VIN 4.5V TO 20V
VOUT 5V 5A
12V 7.7A
20V 9.1A

C1: TDK C3225X5R1E106MT
COUT1: KEMET A700D127M006ATE015 ×3
COUT2: MURATA GRM31CR61A106KA01 ×4
L1: IHLP5050EZ-01 2.2µH

Typical Applications
PACKAGE DESCRIPTION

GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)

NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN INCHES (MILLIMETERS)
3. DRAWING NOT TO SCALE
   "DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE
   **DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE
## REVISION HISTORY

<table>
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<td>Added Note 4 to Order Information section</td>
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<td>Added labels to G22 and G24 in Typical Performance Characteristics</td>
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<td>Modified Pin 3 $V_{RMG}$ description</td>
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<td>Modified $R_{DS(ON)}$ equation</td>
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<td>Modified $R_{ON}$ description in Applications Information</td>
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<td>Edited Figure 7</td>
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<td>Edited Design Example section</td>
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<td>Edited Figure 8</td>
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<td>Edited Typical Applications</td>
<td>20, 21, 22, 23</td>
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<td>Updated Related Parts</td>
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## TYPICAL APPLICATION

4.5V to 14V Input, 0.9V/25A Output at 300kHz

### RELATED PARTS

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<tr>
<th>PART NUMBER</th>
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<tr>
<td>LTC3879</td>
<td>No R\textsubscript{SENSE} Constant On-Time Synchronous Step-Down DC/DC Controller</td>
<td>Very Fast Transient Response, ( I\text{ON(MIN)} = 43\text{ns}, 4V \leq V\text{IN} \leq 38V, 0.6V \leq V\text{OUT} \leq 0.9V\text{IN}, \text{MSOP-16}, 3\text{mm} \times 3\text{mm} \text{QFN-16} )</td>
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<td>LTC3854</td>
<td>Small Footprint Wide ( V\text{IN} ) Range Synchronous Step-Down DC/DC Controller</td>
<td>Fixed 400kHz Operating Frequency 4.5V \leq V\text{IN} \leq 38V, 0.8V \leq V\text{OUT} \leq 5.25V, 2mm \times 3mm \text{QFN-12}</td>
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<td>LTC3851A</td>
<td>No R\textsubscript{SENSE} Wide ( V\text{IN} ) Range Synchronous Step-Down DC/DC Controller</td>
<td>Phase-Lockable Fixed Operating Frequency 250kHz to 750kHz, 4V \leq V\text{IN} \leq 38V, 0.8V \leq V\text{OUT} \leq 5.25V, \text{MSOP-16}, 3\text{mm} \times 3\text{mm} \text{QFN-16}, \text{SSOP-16}</td>
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<tr>
<td>LTC3875</td>
<td>High Frequency Synchronous Step-Down DC/DC Controller</td>
<td>Fixed Operating Frequency 250kHz to 1MHz, 4.5V \leq V\text{IN} \leq 38V, 0.6V \leq V\text{OUT} \leq 0.9V\text{IN}, 3\text{mm} \times 3\text{mm} \text{QFN-16}</td>
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<td>LTC3850/LTC3850-1</td>
<td>Dual 2-Phase, High Efficiency Synchronous Step-Down DC/DC Controllers, R\textsubscript{SENSE} or DCR Current Sensing and Tracking</td>
<td>Phase-Lockable Fixed Operating Frequency 250kHz to 780kHz, 4V \leq V\text{IN} \leq 30V, 0.8V \leq V\text{OUT} \leq 5.25V</td>
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<td>LTC3850-2</td>
<td>Dual 2-Phase, High Efficiency Synchronous Step-Down DC/DC Controllers, R\textsubscript{SENSE} or DCR Current Sensing and Tracking</td>
<td>Phase-Lockable Fixed Operating Frequency 250kHz to 780kHz, 4V \leq V\text{IN} \leq 30V, 0.8V \leq V\text{OUT} \leq 5.25V</td>
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<tr>
<td>LTC3853</td>
<td>Triple Output, Multiphase Synchronous Step-Down DC/DC Controller, R\textsubscript{SENSE} or DCR Current Sensing and Tracking</td>
<td>Phase-Lockable Fixed Operating Frequency 250kHz to 750kHz, 4V \leq V\text{IN} \leq 24V, V\text{OUT} \leq 13.5V</td>
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<td>LTC3857/LTC3857-1</td>
<td>Low ( I\text{D} ), Dual Output 2-Phase Synchronous Step-Down DC/DC Controller with 99% Duty Cycle</td>
<td>Phase-Lockable Fixed Operating Frequency 50kHz to 900kHz, 4V: V\text{IN} \leq 38V, 0.8V \leq V\text{OUT} \leq 24V, I\text{D} = 50\mu\text{A}</td>
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<tr>
<td>LTC3868/LTC3868-1</td>
<td>Low ( I\text{D} ), Dual Output 2-Phase Synchronous Step-Down DC/DC Controller with 99% Duty Cycle</td>
<td>Phase-Lockable Fixed Operating Frequency 50kHz to 900kHz, 4V: V\text{IN} \leq 24V, 0.8V \leq V\text{OUT} \leq 14V, I\text{D} = 170\mu\text{A}</td>
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