FEATURES

- \( V_{IN} \) and \( V_{OUT} \) Limited Only by External Components
- Adjustable Slope Compensation
- Adjustable Overcurrent Protection with Automatic Restart
- Adjustable Operating Frequency (70kHz to 700kHz) with One External Resistor
- Synchronizable to an External Clock
- \( \pm 1.5\% \) Reference Accuracy
- Current Mode Operation for Excellent Line and Load Transient Response
- RUN Pin with Precision Threshold and Adjustable Hysteresis
- Programmable Soft-Start with One External Capacitor
- Low Quiescent Current: 360\( \mu \)A
- Small 10-Lead MSOP and 3mm \( \times \) 3mm DFN

APPLICATIONS

- Telecom Power Supplies
- 42V and 12V Automotive Power Supplies
- Isolated Electronic Equipment

DESCRIPTION

The LTC®3805 is a current mode controller for flyback DC/DC converters designed to drive an N-channel MOSFET in high input and output voltage converter applications. Operating frequency and slope compensation can be programmed by external resistors. Programmable overcurrent sensing protects the converter from short-circuits. Soft-start can be programmed using an external capacitor and the soft-start capacitor also programs an automatic restart feature.

The LTC3805 provides \( \pm 1.5\% \) output voltage accuracy and consumes only 360\( \mu \)A of quiescent current during normal operation and only 40\( \mu \)A during micropower start-up. Using a 9.5V internal shunt regulator, the LTC3805 can be powered from a high \( V_{IN} \) through a resistor or it can be powered directly from a low impedance DC voltage of 9V or less.

The LTC3805 is available in the 10-lead MSOP package and the 3mm \( \times \) 3mm DFN package.

TC3805
Adjustable Frequency
Current Mode Flyback
DC/DC Controller
LTC3805

**ABSOLUTE MAXIMUM RATINGS** (Note 1)

V\(_{CC}\) to GND
- Low Impedance Source ........................................... –0.3V to 8.8V
- Current Fed ..................................................... 25mA into V\(_{CC}\)*
SYNC .............................................................. –0.3V to 6V
SSFLT .............................................................. –0.3V to 5V
FB, I\(_{TH}\), FS ................................................... –0.3V to 3.5V
RUN .............................................................. –0.3V to 18V
OC, I\(_{SENSE}\) .......................................................... –0.3V to 1V
Operating Junction Temperature Range
(Note 2, 3) .................................................... –55°C to 150°C
Storage Temperature Range .................................. –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
MSE Package .................................................. 300°C

*LTC3805 internal clamp circuit regulates V\(_{CC}\) voltage to 9.5V

**PIN CONFIGURATION**

**ORDER INFORMATION**

<table>
<thead>
<tr>
<th>LEAD FREE FINISH</th>
<th>TAPE AND REEL</th>
<th>PART MARKING*</th>
<th>PACKAGE DESCRIPTION</th>
<th>TEMPERATURE RANGE</th>
</tr>
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<tbody>
<tr>
<td>LTC3805EDD#PBF</td>
<td>LTC3805EDD#TRPBF</td>
<td>LCJM</td>
<td>10-Lead (3mm x 3mm) Plastic DFN</td>
<td>–40°C to 85°C</td>
</tr>
<tr>
<td>LTC3805IDD#PBF</td>
<td>LTC3805IDD#TRPBF</td>
<td>LCJM</td>
<td>10-Lead (3mm x 3mm) Plastic DFN</td>
<td>–40°C to 125°C</td>
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<tr>
<td>LTC3805EMSE#PBF</td>
<td>LTC3805EMSE#TRPBF</td>
<td>LTCJK</td>
<td>10-Lead Plastic MSOP</td>
<td>–40°C to 85°C</td>
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<tr>
<td>LTC3805IMSE#PBF</td>
<td>LTC3805IMSE#TRPBF</td>
<td>LTCJK</td>
<td>10-Lead Plastic MSOP</td>
<td>–40°C to 125°C</td>
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<td>–40°C to 150°C</td>
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<tr>
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<td>LTCJK</td>
<td>10-Lead Plastic MSOP</td>
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<table>
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<tr>
<th>LEAD BASED FINISH</th>
<th>TAPE AND REEL</th>
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<th>PACKAGE DESCRIPTION</th>
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<td>10-Lead (3mm x 3mm) Plastic DFN</td>
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<tr>
<td>LTC3805IDD</td>
<td>LTC3805IDD#TR</td>
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<td>–40°C to 125°C</td>
</tr>
<tr>
<td>LTC3805EMSE</td>
<td>LTC3805EMSE#TR</td>
<td>LTCJK</td>
<td>10-Lead Plastic MSOP</td>
<td>–40°C to 85°C</td>
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<td>LTC3805IMSE</td>
<td>LTC3805IMSE#TR</td>
<td>LTCJK</td>
<td>10-Lead Plastic MSOP</td>
<td>–40°C to 125°C</td>
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<tr>
<td>LTC3805HMSE</td>
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<tr>
<td>LTC3805MPMSE</td>
<td>LTC3805MPMSE#TR</td>
<td>LTCJK</td>
<td>10-Lead Plastic MSOP</td>
<td>–55°C to 150°C</td>
</tr>
</tbody>
</table>

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: [http://www.linear.com/leadfree/](http://www.linear.com/leadfree/)

For more information on tape and reel specifications, go to: [http://www.linear.com/tapeandreel/](http://www.linear.com/tapeandreel/)
### Electrical Characteristics

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at $T_A = 25°C$, $V_{CC} = 8V$, unless otherwise noted (Note 2).

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
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<tr>
<td>$V_{TURNON}$</td>
<td>$V_{CC}$ Turn-On Voltage</td>
<td></td>
<td>7.75</td>
<td>8.4</td>
<td>9</td>
<td>V</td>
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<td>$V_{TURNOFF}$</td>
<td>$V_{CC}$ Turn-Off Voltage</td>
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<td>3.75</td>
<td>3.95</td>
<td>4.15</td>
<td>V</td>
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<tr>
<td>$V_{HYST}$</td>
<td>$V_{CC}$ Hysteresis</td>
<td></td>
<td>4.5</td>
<td></td>
<td></td>
<td>V</td>
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<tr>
<td>$V_{CLAMP1mA}$</td>
<td>$V_{CC}$ Shunt Regulator Voltage $V_{CC}$ Sinking 1mA, $V_{RUN} = 0$</td>
<td>●</td>
<td>8.8</td>
<td>9.25</td>
<td>9.65</td>
<td>V</td>
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<tr>
<td>$V_{CLAMP25mA}$</td>
<td>$V_{CC}$ Shunt Regulator Voltage $V_{CC}$ Sinking 25mA, $V_{RUN} = 0$</td>
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<td>8.9</td>
<td>9.5</td>
<td>9.9</td>
<td>V</td>
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<tr>
<td>$I_{CC}$</td>
<td>Input DC Supply Current</td>
<td>Normal Operation ($f_{OSC} = 200kHz$) (Note 4)</td>
<td>360</td>
<td></td>
<td></td>
<td>µA</td>
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<td></td>
<td>$V_{RUN} &lt; V_{RUNON}$ or $V_{CC} &lt; V_{TURNON} - 100mV$ (Micropower Start-Up)</td>
<td>●</td>
<td>40</td>
<td>90</td>
<td></td>
<td>µA</td>
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<td>$V_{RUNON}$</td>
<td>RUN Turn-On Voltage</td>
<td>$V_{CC}$ Sinking 1mA</td>
<td>1.122</td>
<td>1.207</td>
<td>1.292</td>
<td>V</td>
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<td>$V_{RUNOFF}$</td>
<td>RUN Turn-Off Voltage</td>
<td>$V_{CC}$ Sinking 1mA</td>
<td>1.092</td>
<td>1.170</td>
<td>1.248</td>
<td>V</td>
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<td>$I_{RUN(HYST)}$</td>
<td>RUN Hysteresis Current</td>
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<td>4</td>
<td>5</td>
<td>5.8</td>
<td>µA</td>
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<tr>
<td>$V_{FB}$</td>
<td>Regulated Feedback Voltage</td>
<td>$0°C \leq T_J \leq 85°C$ (E-Grade) (Note 5)</td>
<td>0.788</td>
<td>0.800</td>
<td>0.812</td>
<td>V</td>
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<tr>
<td></td>
<td>$-40°C \leq T_J \leq 85°C$ (E-Grade) (Note 5)</td>
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<td>0.780</td>
<td>0.800</td>
<td>0.812</td>
<td>V</td>
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<tr>
<td></td>
<td>$-40°C \leq T_J \leq 125°C$ (I-Grade) (Note 5)</td>
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<td>0.800</td>
<td>0.812</td>
<td>V</td>
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<tr>
<td></td>
<td>$-40°C \leq T_J \leq 150°C$ (H-Grade) (Note 5)</td>
<td>●</td>
<td>0.770</td>
<td>0.800</td>
<td>0.820</td>
<td>V</td>
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<tr>
<td></td>
<td>$-55°C \leq T_J \leq 150°C$ (MP-Grade)</td>
<td>●</td>
<td>0.770</td>
<td>0.800</td>
<td>0.820</td>
<td>V</td>
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<tr>
<td>$I_{FB}$</td>
<td>$V_{FB}$ Input Current</td>
<td>$V_{TH} = 1.3V$ (Note 5)</td>
<td>20</td>
<td></td>
<td></td>
<td>nA</td>
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<tr>
<td>$g_m$</td>
<td>Error Amplifier Transconductance</td>
<td>$I_{TH}$ Pin Load $= +5µA$ (Note 5)</td>
<td>333</td>
<td></td>
<td></td>
<td>µA/V</td>
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<tr>
<td>$\Delta V_{O(LINE)}$</td>
<td>Output Voltage Line Regulation $V_{TURNOFF} &lt; V_{CC} &lt; V_{CLAMP1mA}$ (Note 5)</td>
<td></td>
<td>0.05</td>
<td></td>
<td>mV/V</td>
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<tr>
<td>$\Delta V_{O(LOAD)}$</td>
<td>Output Voltage Load Regulation $I_{TH}$ Sinking 5µA (Note 5)</td>
<td></td>
<td>3</td>
<td></td>
<td>mV/µA</td>
<td></td>
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<tr>
<td></td>
<td>$I_{TH}$ Sourcing 5µA (Note 5)</td>
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<td>3</td>
<td></td>
<td></td>
<td>mV/µA</td>
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<tr>
<td>$f_{OSC}$</td>
<td>Oscillator Frequency</td>
<td>$R_S = 350k$</td>
<td>70</td>
<td></td>
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<td>kHz</td>
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<td></td>
<td>$R_S = 36k$</td>
<td></td>
<td>700</td>
<td></td>
<td></td>
<td>kHz</td>
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<tr>
<td>$D_{CON(MIN)}$</td>
<td>Minimum Switch-On Duty Cycle</td>
<td>$f_{OSC} = 200kHz$</td>
<td>6</td>
<td>9</td>
<td></td>
<td>%</td>
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<tr>
<td>$D_{CON(MAX)}$</td>
<td>Maximum Switch-On Duty Cycle</td>
<td>$f_{OSC} = 200kHz$</td>
<td>70</td>
<td>80</td>
<td>95</td>
<td>%</td>
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<tr>
<td>$f_{SYNC}$</td>
<td>As a Function of $f_{OSC}$</td>
<td>$70kHz &lt; f_{OSC} &lt; 700kHz$, $70kHz &lt; f_{SYNC} &lt; 700kHz$</td>
<td>67</td>
<td>133</td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>$V_{SYNC}$</td>
<td>Minimum SYNC Amplitude</td>
<td></td>
<td>2.9</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{SS}$</td>
<td>Soft-Start Current</td>
<td>$I_{SS}$</td>
<td>6</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>$I_{TO}$</td>
<td>Fault Timeout Current</td>
<td>$I_{TO}$</td>
<td>2</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>$I_{SS(INT)}$</td>
<td>Internal Soft-Start Time</td>
<td>$I_{SS}$ Internal Soft-Start Time</td>
<td>1.8</td>
<td></td>
<td></td>
<td>ms</td>
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<tr>
<td>$I_{TO(INT)}$</td>
<td>Internal Fault Timeout</td>
<td>$I_{TO}$ Internal Fault Timeout</td>
<td>4.5</td>
<td></td>
<td></td>
<td>ms</td>
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<tr>
<td>$I_{RISE}$</td>
<td>Gate Drive Rise Time</td>
<td>$C_{LOAD} = 3000pF$</td>
<td>30</td>
<td></td>
<td></td>
<td>ns</td>
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<tr>
<td>$I_{FALL}$</td>
<td>Gate Drive Fall Time</td>
<td>$C_{LOAD} = 3000pF$</td>
<td>30</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$V_{(MAX)}$</td>
<td>Peak Current Sense Voltage</td>
<td>$R_{SL} = 0$ (Note 6)</td>
<td>85</td>
<td>100</td>
<td>115</td>
<td>mV</td>
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<tr>
<td>$I_{SL(MAX)}$</td>
<td>Peak Slope Compensation Output Current</td>
<td>$R_{SL} = 0$ (Note 7)</td>
<td>10</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>$V_{OCT}$</td>
<td>Overcurrent Threshold</td>
<td>$R_{OCT} = 0$ (Note 8)</td>
<td>85</td>
<td>100</td>
<td>115</td>
<td>mV</td>
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<tr>
<td>$I_{DC}$</td>
<td>Overcurrent Threshold Adjust Current</td>
<td></td>
<td>10</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
</tbody>
</table>
ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3805 is tested under pulsed conditions such that $T_J = T_A$. The LTC3805E is guaranteed to meet specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3805I is guaranteed over the –40°C to 125°C operating junction temperature range, the LTC3805H is guaranteed over the full –40°C to 150°C operating junction temperature range, and the LTC3805MP is tested and guaranteed over the full –55°C to 150°C operating temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

Note 3: $T_J$ is calculated from the ambient temperature $T_A$ and power dissipation $P_D$ according to the following formula:

$$T_J = T_A + (P_D \times 45°C/W)$$

Note 4: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency.

Note 5: The LTC3805 is tested in a feedback loop that servos $V_{FB}$ to the output of the error amplifier while maintaining $I_{TH}$ at the midpoint of the current limit range.

Note 6: Peak current sense voltage is reduced dependent on duty cycle and an optional external resistor in series with the SENSE pin. For details, refer to Programmable Slope Compensation in the Applications Information section.

Note 7: Guaranteed by design.

Note 8: Overcurrent threshold voltage is reduced dependent on an optional external resistor in series with the OC pin. For details, refer to Programmable Overcurrent in the Applications Information section.
TYPICAL PERFORMANCE CHARACTERISTICS

Reference Voltage vs Temperature

Reference Voltage vs Supply Voltage

Oscillator Frequency vs \(R_{FS}\)

Reference Voltage vs Temperature

Oscillator Frequency vs Supply Voltage

Oscillator Frequency vs \(R_{FS}\)

RUN Undervoltage Lockout Thresholds vs Temperature

RUN Hysteresis Current vs Temperature

V\(_{CC}\) Undervoltage Lockout Thresholds vs Temperature

Start-Up \(I_{CC}\) Supply Current vs Temperature
**TYPICAL PERFORMANCE CHARACTERISTICS**

- **ICC Supply Current vs Temperature**
- **VCC Shunt Regulator Voltage vs Temperature**
- **Peak Current Sense Voltage vs Temperature**
- **Overcurrent Threshold vs Temperature**
- **Internal Soft-Start Time vs Temperature**
- **External Soft-Start Current vs Temperature**
- **External Timeout Current vs Temperature**

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**Graphs and Data Tables**

- Supply Current and Temperature graph
- Shunt Regulator Voltage and Temperature graph
- Peak Current Sense Voltage and Temperature graph
- Overcurrent Threshold and Temperature graph
- Internal Soft-Start Time and Temperature graph
- External Soft-Start Current and Temperature graph
- External Timeout Current and Temperature graph

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**Linear Technology**

- Source: LTC3805

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**PIN FUNCTIONS**

**SSFLT (Pin 1):** Soft-Start Pin. A capacitor placed from this pin to GND (Exposed Pad) controls the rate of rise of converter output voltage during start-up. This capacitor is also used for time out after a fault prior to restart.

**ITH (Pin 2):** Error Amplifier Compensation Point. Normal operating voltage range is clamped between 0.7V and 1.9V.

**FB (Pin 3):** Receives the feedback voltage from an external resistor divider across the output.

**RUN (Pin 4):** An external resistor divider connects this pin to VIN and sets the thresholds for converter operation.

**FS (Pin 5):** A resistor connected from this pin to ground sets the frequency of operation.

**SYNC (Pin 6):** Input to synchronize the oscillator to an external source.

**ISENSE (Pin 7):** Performs two functions: for current mode control, it monitors the switch current, using the voltage across an external current sense resistor. Pin 7 also injects a current ramp that develops slope compensation voltage across an optional external programming resistor.

**OC (Pin 8):** Overcurrent Pin. Connect this pin to the external switch current sense resistor. An additional resistor programs the overcurrent trip level.

**VCC (Pin 9):** Supply Pin. A capacitor must closely decouple VCC to GND (Exposed Pad).

**GATE (Pin 10):** Gate Drive for the External N-channel MOSFET. This pin swings from GND to VCC.

**GND (Exposed Pad Pin 11):** Ground. A capacitor must closely decouple GND to VCC (Pin 9). The exposed pad must be soldered to electrical ground on PCB for electrical contact and rated thermal performance.
The LTC3805 is a programmable-frequency current mode controller for flyback, boost and SEPIC DC/DC converters. The LTC3805 is designed so that none of its pins need to come in contact with the input or output voltages of the power supply circuit of which it is a part, allowing the conversion of voltages well beyond the LTC3805’s absolute maximum ratings.

**Main Control Loop**

Please refer to the Block Diagram of this data sheet and the Typical Application shown on the front page. An external resistive voltage divider presents a fraction of the output voltage to the FB pin. The divider is designed so that when the output is at the desired voltage, the FB pin voltage equals the 800mV internal reference voltage. If the load current increases, the output voltage decreases slightly, causing the FB pin voltage to fall below the 800mV reference. The error amplifier responds by feeding current into the ITH pin causing its voltage to rise. Conversely, if the load current decreases, the FB voltage rises above the 800mV reference and the error amplifier sinks current away from the ITH pin causing its voltage to fall.

The voltage at the ITH pin controls the pulse-width modulator formed by the oscillator, current comparator and SR latch. Specifically, the voltage at the ITH pin sets the current comparator’s trip threshold. The current comparator’s ISENSE input monitors the voltage across an external current sense resistor in series with the source of the external MOSFET. At the start of a cycle, the LTC3805’s oscillator sets the SR latch and turns on the external power MOSFET. The current through the external power MOSFET rises as does the voltage on the ISENSE pin. The LTC3805’s current comparator trips when the voltage on the ISENSE pin exceeds a voltage proportional to the voltage on the ITH pin. This resets the SR latch and turns off the external power MOSFET. In this way, the peak current levels through the external MOSFET and the flyback transformer’s primary and secondary windings are controlled by the voltage on the ITH pin. If the current comparator does not trip, the LTC3805 automatically limits the duty cycle to 80%, resets the SR latch, and turns off the external MOSFET.

The path from the FB pin, through the error amplifier, current comparator and the SR latch implements the closed-loop current mode control required to regulate the output voltage against changes in input voltage or output current. For example, if the load current increases, the output voltage decreases slightly, and sensing this, the error amplifier sources current from the ITH pin, raising the current comparator threshold, thus increasing the peak currents through the transformer primary and secondary. This delivers more current to the load and restores the output voltage to the desired level.

The ITH pin serves as the compensation point for the control loop. Typically, an external series RC network is connected from ITH to ground and is chosen for optimal response to load and line transients. The impedance of this RC network converts the output current of the error amplifier to the ITH voltage which sets the current comparator threshold and commands considerable influence over the dynamics of the voltage regulation loop.
**OPERATION**

**Start-Up/Shutdown**

The LTC3805 has two shutdown mechanisms to disable and enable operation: an undervoltage lockout on the VCC supply pin voltage, and a precision-threshold RUN pin. The voltage on both pins must exceed the appropriate threshold before operation is enabled. The LTC3805 transitions into and out of shutdown according to the state diagram shown in Figure 1. Operation in fault timeout is discussed in a subsequent section. During shutdown the LTC3805 draws only a small 40µA current.

The undervoltage lockout (UVLO) mechanism prevents the LTC3805 from trying to drive the external MOSFET gate with insufficient voltage on the VCC pin. The voltage at the VCC pin must initially exceed VTURNON = 8.4V to enable LTC3805 operation. After operation is enabled, the voltage on the VCC pin may fall as low as VTURNOFF = 4V before undervoltage lockout disables the LTC3805. This wide UVLO hysteresis range supports the use of trickle charger powering schemes. See the Applications Information section for more detail.

The RUN pin is connected to the input voltage using a voltage divider. Converter operation is enabled when the voltage on the RUN pin exceeds VRUNON = 1.207V and disabled when the voltage falls below VRUNOFF = 1.170V. Additional hysteresis is added by a 5µA current source acting on the voltage divider’s Thevenin resistance. Setting the input voltage range and hysteresis is further discussed in the Applications Information section.

**Setting the Oscillator Frequency**

Connect a frequency set resistor RF from the FS pin to ground to set the oscillator frequency over a range from 70kHz to 700kHz. The oscillator frequency is calculated from:

\[
\frac{f_{osc}}{24 \cdot 10^9} = \frac{1}{R_F - 1500}
\]

The oscillator may be synchronized to an external clock using the SYNC input. The rising edge of the external clock on the SYNC pin triggers the beginning of a switching period, i.e., the GATE pin going high. The pulse width of the external clock is quite flexible.

**Overcurrent Protection**

With the OC pin connected to the external MOSFET’s current sense resistor, the converter is protected in the event of an overload or short-circuit on the output. During normal operation the peak value of current in the external MOSFET, as measured by the current sense resistor (plus any adjustment for slope compensation), is set by the voltage on the ITH pin operating through the current comparator. As the output current increases, so does the voltage on the ITH pin and so does the peak MOSFET current.
First, consider operation without overcurrent protection. For some maximum converter output current, the voltage on the ITH pin rises to and is clamped at approximately 1.9V. This corresponds to a 100mV limit on the voltage at the ISENSE pin. As the output current is further increased, the duty cycle is reduced as the output voltage sags. However, the peak current in the external MOSFET is limited by the 100mV threshold at the ISENSE pin.

As the output current is increased further, eventually, the duty cycle is reduced to the 6% minimum. Since the external MOSFET is always turned on for this minimum amount of time, the current comparator no longer limits the current through the external MOSFET based on the 100mV threshold. If the output current continues to increase, the current through the MOSFET could rise to a level that would damage the converter.

To prevent damage, the overcurrent pin, OC, is also connected to the current sense resistor, and a fault is triggered if the voltage on the OC pin exceeds 100mV. To protect itself, the converter stops operating as described in the next section. External resistors can be used to adjust the overcurrent threshold to voltages higher or lower than 100mV as described in the Applications Information section.

Add a capacitor CSS from the SSFLT pin to GND to increase both the soft-start time and the time for fault timeout. During soft-start, CSS is charged with a 6µA current. When the LTC3805 comes out of shutdown, the LTC3805 quickly charges CSS to about 0.7V at which point GATE begins switching. From that point, GATE continues switching with increasing duty cycle until the SSFLT pin reaches about 2.25V at which point soft-start is over and closed-loop regulation begins. The voltage on the SSFLT pin additionally further charges to about 4.75V.

CSS also performs the timeout function in the event of a fault. After a fault, CSS is slowly discharged from about 4.75V to about 0.7V by a 2µA current. When the voltage on the SSFLT pin reaches 0.7V the converter attempts to restart. More detail on programming the external soft-start fault timeout is described in the Applications Information section.

Powering the LTC3805
A built-in shunt regulator from the VCC pin to GND limits the voltage on the VCC pin to approximately 9.5V as long as the shunt regulator is not forced to sink more than 25mA. The shunt regulator is always active, even when the LTC3805 is in shutdown, since it serves the vital function of protecting the VCC pin from overvoltage. The shunt regulator permits the use of a wide variety of powering schemes for the LTC3805 even from high voltage sources that exceed the LTC3805’s absolute maximum ratings. Further details on powering schemes are described in the Applications Information section.

Adjustable Slope Compensation
The LTC3805 injects a 10µA peak current ramp out of its ISENSE pin which can be used, in conjunction with an external resistor, for slope compensation in designs that require it. This current ramp is approximately linear and begins at zero current at 6% duty cycle, reaching peak current at 80% duty cycle. Additional details are provided in the Applications Information section.
Many LTC3805 application circuits can be derived from the topology shown on the first page of this data sheet and from the topology shown in Figure 2.

The LTC3805 itself imposes no limits on allowed input voltage $V_{IN}$ or output voltage $V_{OUT}$. These are all determined by the ratings of the external power components. The factors are: Q1 maximum drain-source voltage ($V_{DSS}$), on-resistance ($R_{DS(ON)}$) and maximum drain current, $T_1$ saturation flux level and winding insulation breakdown voltages, $C_{IN}$ and $C_{OUT}$ maximum working voltage, equivalent series resistance (ESR), and maximum ripple current ratings, and D1 and $R_{SENSE}$ power ratings.

$VCC$ Bias Power

The $VCC$ pin must be bypassed to the GND pin with a minimum 1µF ceramic or tantalum capacitor located immediately adjacent to the two pins. Proper supply bypassing is necessary to supply the high transient currents required by the MOSFET gate driver.

For maximum flexibility, the LTC3805 is designed so that it can be operated from voltages well beyond the LTC3805's absolute maximum ratings. Figure 2 shows the simplest case, in which the LTC3805 is powered with a resistor $R_{VCC}$ connected between the input voltage and $VCC$. The built-in shunt regulator limits the voltage on the $VCC$ pin to around 9.5V as long as the internal shunt regulator is not forced to sink more than 25mA. This powering scheme has the drawback that the power loss in the resistor reduces converter efficiency and the 25mA shunt regulator maximum may limit the maximum-to-minimum range of input voltage.

In some cases, the input or output voltage is within the operational range of $VCC$ for the LTC3805. In this case, the LTC3805 is operated directly from either the input or output voltage. Figure 3 shows a 5V output converter in which $R_{START}$ and $C_{VCC}$ form a start-up trickle charger while D2 powers $VCC$ from the output once the converter is in normal operation. Note that $R_{START}$ need only supply the very small 40µA micropower start-up current while...
APPLICATIONS INFORMATION

CVCC is charged to VTURNON. At this point, assuming VRUN > VRUNON, the converter begins switching the external MOSFET and ramps up the converter output voltage at a rate set by the capacitor CSS on the SSFLT pin. Since RSTART cannot supply enough current to operate the external MOSFET, CVCC begins discharging and VCC drops. The soft-start must be fast enough and the discharge of CVCC slow enough so that the output voltage reaches its target value of 5V before VCC drops to VTURNOFF or the converter would fail to start.

The typical application circuit in Figure 9 shows a different flyback converter bias power strategy for a case in which neither the input or output voltage is suitable for providing bias power to the LTC3805. A small NPN preregulator transistor and a Zener diode are used to accelerate the rise of VCC and reduce the value of the VCC bias capacitor. The flyback transformer has an additional bias winding to provide bias power. Note that this topology is very powerful because, by appropriate choice of transformer turns ratio, the output voltage can be chosen without regard to the value of the input voltage or the VCC bias power for the LTC3805. The number of turns in the bias winding is chosen according to

\[ N_{BIAS} = N_{SEC} \frac{V_{CC} + V_{D4}}{V_{OUT} - V_{D1}} \]

where NBIAS is the number of turns in the bias winding, NSEC is the number of turns in the secondary winding, VCC is the desired voltage to power the LTC3805, VOUT is the converter output voltage, VD1 is the forward voltage drop of D1 and VD4 is the forward voltage drop of D4.

Note that since VOUT is regulated by the converter control loop, VCC is also regulated although not as precisely. The value of VCC is often constrained since NBIAS and NSEC are often a limited range of small integer numbers. For proper operation, the value of VCC must be between VTURNON and VTURNOFF. Since the ratio of VTURNON to VTURNOFF is over two to one, this requirement is relatively easy to satisfy. Figure 9 shows a similar low power nonisolated telecom converter using a trickle charger.

Transformer Design Considerations

Transformer specification and design is perhaps the most critical part of applying the LTC3805 successfully. In addition to the usual list of caveats dealing with high frequency power transformer design, the following should prove useful.

Turns Ratios

Due to the use of the external feedback resistor divider ratio to set output voltage, the user has relative freedom in selecting transformer turns ratio to suit a given application. Simple ratios of small integers, e.g., 1:1, 2:1, 3:2, etc. can be employed which yield more freedom in setting total turns and transformer inductance. Simple integer turns ratios also facilitate the use of “off-the-shelf” configurable transformers. Turns ratio can be chosen on the basis of desired duty cycle. However, remember that the input supply voltage plus the secondary-to-primary referred version of the flyback pulse (including leakage spike) must not exceed the allowed external MOSFET breakdown rating.
APPLICATIONS INFORMATION

Leakage Inductance
Transformer leakage inductance (on either the primary or secondary) causes a voltage spike to occur after the MOSFET (Q1) turn-off. This is increasingly prominent at higher load currents, where more stored energy must be dissipated. In some cases an RC “snubber” circuit will be required to avoid overvoltage breakdown at the MOSFET’s drain node. Application Note 19 is a good reference on snubber design. A bifilar or similar winding technique is a good way to minimize troublesome leakage inductances. However, remember that this will limit the primary-to-secondary breakdown voltage, so bifilar winding is not always practical.

Setting Undervoltage and Hysteresis on $V_{IN}$
The RUN pin is connected to a resistive voltage divider connected to $V_{IN}$ as shown in Figure 4. The voltage threshold for the RUN pin is $V_{RUNON}$ rising and $V_{RUNOFF}$ falling. Note that $V_{RUNON} - V_{RUNOFF} = 35\text{mV}$ of built-in voltage hysteresis that helps eliminate false trips.

To introduce further user-programmable hysteresis, the LTC3805 sources $5\mu\text{A}$ out of the RUN pin when operation of LTC3805 is enabled. As a result, the falling threshold for the RUN pin also depends on the value of $R_1$ and can be programmed by the user. The falling threshold for $V_{IN}$ is therefore

$$V_{IN(RUN,FALLING)} = V_{RUNOFF} \cdot \frac{R_1 + R_2}{R_2} - R_1 \cdot 5\mu\text{A}$$

where $R_1(5\mu\text{A})$ is the additional hysteresis introduced by the $5\mu\text{A}$ current sourced by the RUN pin. When in shutdown, the RUN pin does not source the $5\mu\text{A}$ current and the rising threshold for $V_{IN}$ is simply

$$V_{IN(RUN,RISING)} = V_{RUNON} \cdot \frac{R_1 + R_2}{R_2}$$

External Run/Stop Control
To implement external run control, place a small N-channel MOSFET from the RUN pin to GND as shown in Figure 4. Drive the gate of this MOSFET high to pull the RUN pin to ground and prevent converter operation.

Selecting Feedback Resistor Divider Values
The regulated output voltage is determined by the resistor divider across $V_{OUT}$ ($R_3$ and $R_4$ in Figure 2). The ratio of $R_4$ to $R_3$ needed to produce a desired $V_{OUT}$ can be calculated:

$$R_3 = \frac{V_{OUT} - 0.8\text{V}}{0.8\text{V}} \cdot R_4$$

Choose resistance values for $R_3$ and $R_4$ to be as large as possible in order to minimize any efficiency loss due to the static current drawn from $V_{OUT}$, but just small enough so that when $V_{OUT}$ is in regulation the input current to the $V_{FB}$ pin is less than 1% of the current through $R_3$ and $R_4$. A good rule of thumb is to choose $R_4$ to be less than 80k.

---

Figure 4. Setting RUN Pin Voltage and Run/Stop Control
Feedback in Isolated Applications

Isolated applications do not use the FB pin and error amplifier but control the I_{TH} pin directly using an opto-isolator driven on the other side of the isolation barrier as shown in Figure 5. A detailed version is shown in Figure 9. For isolated converters, the FB pin is grounded which provides pull-up on the I_{TH} pin. This pull-up is not enough to properly bias the opto-isolator which is typically biased using a resistor to VCC. Since the I_{TH} pin cannot sink the opto-isolator bias current, a diode is required to block it from the I_{TH} pin. A low leakage Schottky diode or low forward voltage PN junction diode should be used to ensure that the opto-isolator is able to pull I_{TH} down to its lower clamp.

Oscillator Synchronization

The oscillator may be synchronized to an external clock by connecting the synchronization signal to the SYNC pin. The LTC3805 oscillator and turn-on of the switch are synchronized to the rising edge of the external clock. The frequency of the external sync signal must be ±33% with respect to f_{OSC} (as programmed by R_{FS}). Additionally, the value of f_{SYNC} must be between 70kHz and 700kHz.

Current Sense Resistor Considerations

The external current sense resistor (R_{SENSE} in Figure 2) allows the user to optimize the current limit behavior for the particular application. As the current sense resistor is varied from several ohms down to tens of milliohms, peak switch current goes from a fraction of an ampere to several amperes. Care must be taken to ensure proper circuit operation, especially with small current sense resistor values.

For example, with the peak current sense voltage of 100mV on the I_{SENSE} pin, a peak switch current of 5A requires a sense resistor of 0.020Ω. Note that the instantaneous peak power in the sense resistor is 0.5W and it must be rated accordingly. The LTC3805 has only a single sense line to this resistor. Therefore, any parasitic resistance in the ground side connection of the sense resistor will increase its apparent value. In the case of a 0.020Ω sense resistor, one miliohm of parasitic resistance will cause a 5% reduction in peak switch current. So the resistance of printed circuit copper traces and vias cannot necessarily be ignored.

Programmable Slope Compensation

The LTC3805 injects a ramping current through its I_{SENSE} pin into an external slope compensation resistor R_{SLOPE}. This current ramp starts at zero right after the GATE pin has been high for the LTC3805’s minimum duty cycle of 6%. The current rises linearly towards a peak of 10µA at the maximum duty cycle of 80%, shutting off once the GATE pin goes low. A series resistor R_{SLOPE} connecting the I_{SENSE} pin to the current sense resistor R_{SENSE} develops a ramping voltage drop. From the perspective of the I_{SENSE} pin, this ramping voltage adds to the voltage across the sense resistor, effectively reducing the current comparator threshold in proportion to duty cycle. This stabilizes the control loop against subharmonic oscillation. The amount of reduction in the current comparator threshold (∆V_{SENSE}) can be calculated using the following equation:

\[ ∆V_{SENSE} = \frac{\text{Duty Cycle} - 6\%}{80\%} \times 10\text{µA} \times R_{SLOPE} \]

Note: LTC3805 enforces 6% < Duty Cycle < 80%. A good starting value for R_{SLOPE} is 3k, which gives a 30mV drop in current comparator threshold at 80% duty cycle. Designs that do not operate at greater than 50% duty cycle do not need slope compensation and may replace R_{SLOPE} with a direct connection.
APPLICATIONS INFORMATION

Overcurrent Threshold Adjustment

Figure 6 shows the connection of the overcurrent pin, OC, along with the ISENSE pin and the current sense resistor RSENSE located in the source circuit of the power NMOS which is driven by the GATE pin. The internal overcurrent threshold on the OC pin is set at VOC = 100mV which is the same as the peak current sense voltage VIN(MAX) = 100mV on the ISENSE pin. The role of the slope compensation adjustment resistor RSLOPE and the slope compensation current ISLOPE is discussed in the prior section. In combination with the overcurrent threshold adjust current IOC = 10µA, an external resistor ROC can be used to lower the overcurrent trip threshold from 100mV. This section describes how to pick ROC to achieve the desired performance. In the discussion that follows be careful to distinguish between “current limit” where the converter continues to run with the ISENSE pin limiting current on a cycle-by-cycle basis while the output voltage falls below the regulation point and “overcurrent protection” where the OC pin senses an overcurrent and shuts down the converter for a timeout period before attempting an automatic restart.

One overcurrent protection strategy is for the converter to never enter current limit but to maintain output voltage regulation up to the point of tripping the overcurrent protection. Operation at minimum input voltage VIN(MIN) hits current limiting for the smallest output current and is the design point for this strategy.

First, for operation at VIN(MIN), calculate the duty cycle Duty Cycle VIN(MIN) using the appropriate formula depending on whether the converter is a boost, flyback or SEPIC. Then use Duty Cycle VIN(MIN) to calculate ∆VSENSE(VIN(MIN)) using the formula in the prior section. For overcurrent protection to trip at exactly the point where current limiting would begin set:

\[ R_{OC(CRIT)} = \frac{\Delta V_{SENSE(VIN(MIN))}}{10\mu A} \]

To find the actual output current that trips overcurrent protection, calculate the peak switch current IPK(VIN(MIN)) from:

\[ IPK(VIN(MIN)) = \frac{100mV - \Delta V_{SENSE(VIN(MIN))}}{R_{SENSE}} \]

Then calculate the converter output current that corresponds to IPK(VIN(MIN)). Again, the calculation depends both on converter type and the details of converter design including inductor current ripple. For minimum input voltage, ROC(CRIT) produces an overcurrent trip at an output current just before loss of output voltage regulation and the onset of current limiting. Note that the output current that causes an overcurrent trip is higher for higher input voltages but that an overcurrent trip will always occur before loss of output voltage regulation. If desired to meet a specific design target, an increase in ROC above ROC(CRIT) can be used to reduce the trip threshold and make the converter trip for a lower output current.

This calculation is based on steady-state operation. Depending on design, overcurrent protection can also be triggered during a start-up transient, particularly if large output filter capacitors are being charged as output voltage rises. If that is a problem, output capacitor charging can...
be slowed by using a larger value of SSFLT capacitor. It is also possible to trip overcurrent protection during a load step especially if the trip threshold is lowered by making $R_{OC} > R_{OC(CRIT)}$.

Another overcurrent protection strategy is keep the converter running as current limiting reduces the duty cycle and the output voltage sags. In this case, the goal is often keep the converter in normal operation over as wide a range as possible, including current limiting, and to trigger the overcurrent trip only to prevent damage. To implement this strategy use a value of $R_{OC}$ smaller than $R_{OC(CRIT)}$. This also reduces sensitivity to overcurrent trips caused by transient operation. In the limit, set $R_{OC} = 0$ and connect the OC pin directly to $R_{SENSE}$. This causes an overcurrent trip near minimum duty cycle or around 6%.

In some cases it may be desirable to increase the trip threshold even further. In this strategy, the converter is allowed to operate all the way down to minimum duty cycle at which point the cycle-by-cycle current limit of the $I_{SENSE}$ pin is lost and switch current goes up proportionally to the output current. Figures 7 and 8 show two ways to do this. Figure 7 is for relatively low currents with relatively large values of $R_{SENSE}$. Using this circuit the overcurrent trip threshold is increased from 100mV to:

$$V_{OC} = \frac{R_{SENSE1} + R_{SENSE2}}{R_{SENSE1}} \cdot 100\text{mV}$$

where it is assumed that the values of $R_{SENSE1}$ and $R_{SENSE2}$ are so small that the $I_{OC} = 10\mu\text{A}$ threshold adjustment current produces a negligible change in $V_{OC}$.

For larger currents, values of the current sense resistors must be very small and the circuit of Figure 7 becomes impractical. The circuit of Figure 8 can be substituted and the current sense threshold is increased from 100mV to:

$$V_{OC} = \frac{R1 + R2}{R1} \cdot 100\text{mV}$$

where the values of $R1$ and $R2$ should be kept below 10Ω to prevent the $I_{OC} = 10\mu\text{A}$ threshold adjustment current from producing a shift in $V_{OC}$.

External Soft-Start Fault Timeout

The external soft-start is programmed by a capacitor $C_{SS}$ from the SSFLT pin to GND. At the initiation of soft-start the voltage on the SSFLT pin is quickly charged to 0.7V at which point GATE begins switching. From that point, a 6µA current charges the voltage on the SSFLT pin until the voltage reaches about 2.25V at which point soft-start is over and the converter enters closed-loop regulation. The soft-start time $t_{SS(EXT)}$ as a function of the soft-start capacitor, $C_{SS}$, is therefore:

$$t_{SS(EXT)} = C_{SS} \cdot \frac{2.25 - 0.7V}{6\mu\text{A}}$$

After soft-start is complete, the voltage on the SSFLT pin continues to charge to about a final value of 4.75V. Note that choosing a value of $C_{SS}$ less than 5.8nF has no effect since it would attempt to program an external soft-start time $t_{SS(EXT)}$ less than the mandatory minimum.
internal soft-start time $t_{SS(IN)} = 1.8\text{ms}$. However, in noisy environments a small $C_{SS}$ can be valuable to limit jitter in the oscillator.

If there is an overcurrent fault detected on the OC pin, the LTC3805 enters a shutdown mode while a $2\mu\text{A}$ current discharges the voltage on the SSFLT pin from $4.75\text{V}$ to about $0.7\text{V}$. The fault timeout $t_{FTO(EXT)}$ is therefore:

$$t_{FTO(EXT)} = \frac{C_{SS} \times (4.75\text{V} - 0.7\text{V})}{2\mu\text{A}}$$

At this point, the LTC3805 attempts a restart.

In the event of a persistent fault, such as a short-circuit on the converter output, the converter enters a “hiccup” mode where it continues to try and restart at repetition rate determined by $C_{SS}$. If the fault is eventually removed the converter successfully restarts.

**Applications Information**

**Typical Application**

![Figure 9. Low Power Isolated Telecom Supply with NPN Preregulator](image-url)
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1699 Rev C)

MSE Package
10-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1664 Rev H)

NOTES:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE MO-229 VARIATION OF (WEED-2).
2. DRAWING NOT TO SCALE
3. DIMENSIONS IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD dimension DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD SHALL NOT EXCEED 0.254mm (.010") PER SIDE.
## Revision History

(Revision history begins at Rev E)

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Figure 10. Low Power Nonisolated Telecom Supply with Trickle Charger

Efficiency and Power Loss vs Load Current and $V_{IN}$: $V_O = 3.3V$

NOTE: CAN ALSO USE NPN PREREGULATOR AS SHOWN IN FIGURE 9

RELATED PARTS

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<td>Boost, Flyback, SEPIC and Inverting Controller</td>
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