High Efficiency, Synchronous, 4-Switch Buck-Boost Controller

**Features**
- Single Inductor Architecture Allows $V_{IN}$ Above, Below or Equal to the Regulated $V_{OUT}$
- Programmable Input or Output Current
- Wide $V_{IN}$ Range: 4V to 38V
- 1% Output Voltage Accuracy: $0.8V < V_{OUT} < 38V$
- Synchronous Rectification: Up to 98% Efficiency
- Current Mode Control
- Phase-Lockable Fixed Frequency: 200kHz to 600kHz
- No Reverse Current During Start-Up
- Power Good Output Voltage Monitor
- Internal 5.5V LDO
- Quad N-Channel MOSFET Synchronous Drive
- $V_{OUT}$ Disconnected from $V_{IN}$ During Shutdown
- True Soft-Start and $V_{OUT}$ Short Protection, Even in Boost Mode
- Available in 28-Lead QFN (4mm × 5mm) and 28-Lead SSOP Packages

**Applications**
- Automotive Systems
- Distributed DC Power Systems
- High Power Battery-Operated Devices
- Industrial Control

**Description**

The LTC®3789 is a high performance buck-boost switching regulator controller that operates from input voltages above, below or equal to the output voltage. The constant-frequency, current mode architecture allows a phase-lockable frequency of up to 600kHz, while an output current feedback loop provides support for battery charging. With a wide 4V to 38V (40V maximum) input and output range and seamless, low noise transitions between operating regions, the LTC3789 is ideal for automotive, telecom and battery-powered systems.

The operating mode of the controller is determined through the MODE/PLLIN pin. The MODE/PLLIN pin can select between pulse-skipping mode and forced continuous mode operation and allows the IC to be synchronized to an external clock. Pulse-skipping mode offers high efficiency and low ripple at light loads, while forced continuous mode operates at a constant frequency for noise-sensitive applications.

A PGGOOD pin indicates when the output is within 10% of its designed set point. The LTC3789 is available in low-profile 28-pin 4mm × 5mm QFN and narrow SSOP packages.

For more information [www.linear.com/LTC3789](http://www.linear.com/LTC3789)
**LTC3789**

### Absolute Maximum Ratings (Note 1)

- **Input Supply Voltage \((V_{IN})\):** 40V to –0.3V
- **Topside Driver Voltages** (BOOST1, BOOST2): 46V to –0.3V
- **Switch Voltage** (SW1, SW2): 6V to –0.3V
- **Current Sense Voltages** \((I_{SENSE^+}, I_{SENSE^-})\): 40V to –0.3V
- **BOOST1, BOOST2 – SW1, SW2:** 6V to –0.3V
- **TG1, TG2:** 6V to –0.3V
- **INTVCC Voltage:** 14V to –0.3V
- **INTVCC Peak Output Current:** 100mA
- **OPERATING JUNCTION TEMPERATURE RANGE:** –40°C to 125°C
- **STORAGE TEMPERATURE RANGE:** –65°C to 125°C
- **LEAD TEMPERATURE (SOLDERING, 10 sec.)**
  - **GN Package:** 300°C
  - **UFD Package:** 125°C

### Pin Configuration

- **TOP VIEW**
- **GN PACKAGE**
  - 28-LEAD NARROW PLASTIC SSOP
  - **\( T_{JMAX} = 125°C, \theta_{JA} = 80°C/W \)**

### Order Information

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<td>LTC3789EGN#TRPBF</td>
<td>LTC3789</td>
<td>28-Lead Narrow Plastic SSOP</td>
<td>–40°C to 125°C</td>
</tr>
<tr>
<td>LTC3789IGN#PBF</td>
<td>LTC3789IGN#TRPBF</td>
<td>LTC3789</td>
<td>28-Lead Narrow Plastic SSOP</td>
<td>–40°C to 125°C</td>
</tr>
<tr>
<td>LTC3789EUFD#PBF</td>
<td>LTC3789EUFD#TRPBF</td>
<td>3789</td>
<td>28-Lead (4mm × 5mm) Plastic QFN</td>
<td>–40°C to 125°C</td>
</tr>
<tr>
<td>LTC3789IUFD#PBF</td>
<td>LTC3789IUFD#TRPBF</td>
<td>3789</td>
<td>28-Lead (4mm × 5mm) Plastic QFN</td>
<td>–40°C to 125°C</td>
</tr>
</tbody>
</table>

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: [http://www.linear.com/leadfree/](http://www.linear.com/leadfree/)

For more information on tape and reel specifications, go to: [http://www.linear.com/tapeandreel/](http://www.linear.com/tapeandreel/)
**ELECTRICAL CHARACTERISTICS**  

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_IN = 15V, V_RUN = 5V, unless otherwise noted.

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<thead>
<tr>
<th>SYMBOL</th>
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<tbody>
<tr>
<td>V_IN</td>
<td>Input Supply Voltage</td>
<td></td>
<td>4</td>
<td>38</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>V_OUT</td>
<td>Output Voltage</td>
<td></td>
<td>0.8</td>
<td>38</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>V_FB</td>
<td>Regulated Feedback Voltage</td>
<td>( I_{TH} ) Voltage = 1.2V (Note 4), ( T_A = -40°C ) to 85°C ( I_{TH} = 1.2V, T_A = 125°C, T_A = -40°C ) to 125°C</td>
<td>● 0.792</td>
<td>0.800</td>
<td>0.808</td>
<td>V</td>
</tr>
<tr>
<td>I_FB</td>
<td>Feedback Current</td>
<td>(Note 4) ( I_{TH} = 1.2V, T_A = 125°C, T_A = -40°C ) to 125°C</td>
<td>-15</td>
<td>-50</td>
<td>nA</td>
<td></td>
</tr>
<tr>
<td>V_REFLNREG</td>
<td>Reference Voltage Line Regulation</td>
<td>( V_{IN} = 4V ) to 38V (Note 4)</td>
<td>0.002</td>
<td>0.02</td>
<td>%/V</td>
<td></td>
</tr>
<tr>
<td>V_LOADREG</td>
<td>Output Voltage Load Regulation</td>
<td>(Note 4) Measured in Servo Loop, ( \Delta I_{TH} ) Voltage = 1.4V to 2V Measured in Servo Loop, ( \Delta I_{TH} ) Voltage = 2V to 2.5V</td>
<td>● 0.01</td>
<td>0.1</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>●</td>
<td></td>
<td></td>
<td>● -0.01</td>
<td>-0.1</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>( g_m )</td>
<td>Transconductance Amplifier ( g_m )</td>
<td>( I_{TH} = 1.2V, ) Sink/Source 5( \mu )A (Note 4)</td>
<td>1.5</td>
<td></td>
<td>mmho</td>
<td></td>
</tr>
<tr>
<td>I_0</td>
<td>Input DC Supply Current</td>
<td>Normal Mode</td>
<td>3</td>
<td></td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Shutdown</td>
<td>40</td>
<td>60</td>
<td>( \mu )A</td>
<td></td>
</tr>
<tr>
<td>UVLO</td>
<td>Undervoltage Lockout</td>
<td>INTVCC Ramping Down</td>
<td>3.4</td>
<td>3.6</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>UVLO Hyst</td>
<td>Undervoltage Hysteresis</td>
<td></td>
<td>0.4</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>I_SENSE+ I_SENSE-</td>
<td>SENSE Pins Current</td>
<td>( V_{SENSE} = V_{SENSE}^+ = 0V )</td>
<td>0.2</td>
<td>±1</td>
<td>( \mu )A</td>
<td></td>
</tr>
<tr>
<td>I_OSENSE+ I_OSENSE-</td>
<td>IOSENSE Pins Current</td>
<td>( V_{IOSENSE} = V_{IOSENSE}^+ = 10V )</td>
<td>10</td>
<td>14</td>
<td>( \mu )A</td>
<td></td>
</tr>
<tr>
<td>I_SS</td>
<td>Soft-Start Charge Current</td>
<td>( V_{SS} = 0V )</td>
<td>2</td>
<td>3</td>
<td>4</td>
<td>( \mu )A</td>
</tr>
<tr>
<td>V_RUN(ON)</td>
<td>RUN Pin On-Threshold</td>
<td>( V_{RUN} ) Rising</td>
<td>1.22</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>V_RUN(HYS)</td>
<td>RUN Pin On-Hysteresis</td>
<td></td>
<td>150</td>
<td></td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>I_RUN</td>
<td>RUN Pin Source Current</td>
<td></td>
<td>1.2</td>
<td></td>
<td>( \mu )A</td>
<td></td>
</tr>
<tr>
<td>I_RUN(HYS)</td>
<td>RUN Pin Hysteresis Current</td>
<td></td>
<td>5</td>
<td></td>
<td>( \mu )A</td>
<td></td>
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<tr>
<td>V_SENSE(MAX)</td>
<td>Maximum Current Sense Threshold</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td></td>
<td>Buck Region, (( I_L ) Valley)</td>
<td>( V_{FB} = 0.7V )</td>
<td>73</td>
<td>90</td>
<td>107</td>
<td>mV</td>
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<tr>
<td></td>
<td>Boost Region, (( I_L ) Peak)</td>
<td>( V_{FB} = 0.7V )</td>
<td>123</td>
<td>140</td>
<td>157</td>
<td>mV</td>
</tr>
<tr>
<td>V_SENSE(AVG)</td>
<td>Maximum Input/Output Average Current Sense Threshold</td>
<td>( I_{ILIM} ) = 0V ( I_{ILIM} ) Floating</td>
<td>48</td>
<td>50</td>
<td>52.5</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( I_{ILIM} ) = INTVCC</td>
<td>90</td>
<td>100</td>
<td>106</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>130</td>
<td>145</td>
<td>160</td>
<td>mV</td>
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<tr>
<td>R_DSPFET(ON)</td>
<td>Driver Pull-Up On-Resistance</td>
<td></td>
<td>2.6</td>
<td></td>
<td>( \Omega )</td>
<td></td>
</tr>
<tr>
<td>R_DSNFET(ON)</td>
<td>Driver Pull-Down On-Resistance</td>
<td></td>
<td>1.5</td>
<td></td>
<td>( \Omega )</td>
<td></td>
</tr>
<tr>
<td>TG ( t_r ) TG ( t_f )</td>
<td>Top Gate Rise Time</td>
<td>Top Gate Fall Time</td>
<td></td>
<td>25</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>BG ( t_r ) BG ( t_f )</td>
<td>Bottom Gate Rise Time</td>
<td>Bottom Gate Fall Time</td>
<td></td>
<td>25</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>TG/BG ( t_{1D} )</td>
<td>Top Gate Off to Bottom Gate On Delay Synchronous Switch-On Delay Time</td>
<td>( C_{LOAD} = 3300pF ) Each Driver (Note 6)</td>
<td>60</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>BG/TG ( t_{1D} )</td>
<td>Bottom Gate Off to Top Gate On Delay Top Switch-On Delay Time</td>
<td>( C_{LOAD} = 3300pF ) Each Driver (Note 6)</td>
<td>60</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>DFMAX.BOOST</td>
<td>Maximum Duty Factor</td>
<td>% Switch C On</td>
<td>90</td>
<td></td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>DON(MIN,BOOST)</td>
<td>Minimum Duty Factor for Main Switch in Boost Operation</td>
<td>% Switch C On</td>
<td>9</td>
<td></td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>DON(MIN,BUCK)</td>
<td>Minimum Duty Factor for Synchronous Switch in Buck Operation</td>
<td>% Switch B On</td>
<td>9</td>
<td></td>
<td>%</td>
<td></td>
</tr>
</tbody>
</table>
# LTC3789

## Electrical Characteristics

The icon denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at \( T_A = 25^\circ C \) (Note 2). \( V_{IN} = 15V, V_{RUN} = 5V, \) unless otherwise noted.

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</tr>
</thead>
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<td>INTVCC</td>
<td>Linear Regulator</td>
<td>6.5V &lt; ( V_{IN} ) &lt; 40V, ( V_{EXTVCC} = 0V )</td>
<td>5.2</td>
<td>5.5</td>
<td>5.8</td>
<td>V</td>
</tr>
<tr>
<td>( V_{LDivist} )</td>
<td>INTVCC Load Regulation</td>
<td>( I_{CC} = 0mA ) to 20mA, ( V_{EXTVCC} = 0V )</td>
<td>0.2</td>
<td>1.0</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>( V_{INTVCCext} )</td>
<td>INTVCC Voltage</td>
<td>6.5V &lt; ( V_{EXTVCC} &lt; 14V )</td>
<td>5.2</td>
<td>5.5</td>
<td>5.8</td>
<td>V</td>
</tr>
<tr>
<td>( V_{LDdoext} )</td>
<td>INTVCC Load Regulation</td>
<td>( I_{CC} = 0mA ) to 20mA, ( V_{EXTVCC} = 12V )</td>
<td>0.2</td>
<td>1.0</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>( V_{EXTVCC} )</td>
<td>EXTVCC Switchover Voltage</td>
<td>( I_{CC} = 0mA ) to 20mA, EXTVCC Ramping Positive</td>
<td>4.7</td>
<td>4.8</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( V_{LDohys} )</td>
<td>EXTVCC Hysteresis</td>
<td></td>
<td>0.25</td>
<td>V</td>
<td></td>
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### Oscillator and Phase-Locked Loop

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<tbody>
<tr>
<td>( f_{nom} )</td>
<td>Nominal Frequency</td>
<td>( V_{FREQ} = 1.2V )</td>
<td>350</td>
<td>400</td>
<td>440</td>
<td>kHz</td>
</tr>
<tr>
<td>( f_{low} )</td>
<td>Low Fixed Frequency</td>
<td>( V_{FREQ} = 0V )</td>
<td>175</td>
<td>200</td>
<td>225</td>
<td>kHz</td>
</tr>
<tr>
<td>( f_{high} )</td>
<td>High Fixed Frequency</td>
<td>( V_{FREQ} = 2.4V )</td>
<td>570</td>
<td>640</td>
<td>710</td>
<td>kHz</td>
</tr>
<tr>
<td>( f_{sync} )</td>
<td>Synchronizable Frequency</td>
<td>MODE/PLLIN = External Clock</td>
<td>200</td>
<td>600</td>
<td></td>
<td>kHz</td>
</tr>
<tr>
<td>( R_{MODE/PLLIN} )</td>
<td>MODE/PLLIN Input Resistance</td>
<td></td>
<td>220</td>
<td>kΩ</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{FREQ} )</td>
<td>Frequency Setting Current</td>
<td></td>
<td>8</td>
<td>10</td>
<td>12</td>
<td>μA</td>
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### PGOOD Output

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<tr>
<td>( V_{PG} )</td>
<td>PGOOD Voltage Low</td>
<td>( I_{PGOOD} = 2mA )</td>
<td>0.1</td>
<td>0.3</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( I_{PGOOD} )</td>
<td>PGOOD Leakage Current</td>
<td>( V_{PGOOD} = 5V )</td>
<td>±1</td>
<td></td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>( V_{PG} )</td>
<td>PGOOD Trip Level</td>
<td>( V_{FB} ) with Respect to Set Output Voltage</td>
<td></td>
<td></td>
<td></td>
<td>%</td>
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</table>

### Notes

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LTC3789 is tested under pulse load conditions such that \( T_J = T_A \). The LTC3789 is guaranteed to meet performance specifications from 0°C to 85°C operating junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3789I is guaranteed to meet performance specifications over the full –40°C to 125°C operating junction temperature range.

**Note 3:** \( T_J \) is calculated from the ambient temperature \( T_A \) and power dissipation \( P_D \) according to the following formula:

\[
T_J = T_A + (P_D \times 80^\circ C/W)
\]

\[
T_J = T_A + (P_D \times 34^\circ C/W)
\]

**Note 4:** The LTC3789 is tested in a feedback loop that servos \( V_{ITH} \) to a specified voltage and measures the resultant \( V_{FB} \).

**Note 5:** Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See the Applications Information section.

**Note 6:** Do not apply a voltage or current to these pins. They must be connected to capacitive loads only, otherwise permanent damage may occur.
TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ C$ unless otherwise noted.
TYPICAL PERFORMANCE CHARACTERISTICS  $T_A = 25°C$ unless otherwise noted.

Forced Continuous Mode

Pulse-Skipping Mode

Oscillator Frequency vs Temperature

Undervoltage Threshold at $\text{INTV}_{\text{CC}}$ vs Temperature

Undervoltage Threshold at $V_{\text{IN}}$ vs Temperature
TYPICAL PERFORMANCE CHARACTERISTICS  \( T_A = 25^\circ C \) unless otherwise noted.

- Maximum Current Sense Threshold vs Duty Factor (Boost)
- Maximum Current Sense Threshold vs Duty Factor (Buck)
- Maximum Current Limit vs Temperature
- Peak Current Threshold vs \( V_{ITH} \) (Boost)
- Valley Current Threshold vs \( V_{ITH} \) (Buck)
- Current Foldback Limit
TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ$C unless otherwise noted.

**Load Step**

- **VIN = 6V**
- **VOUT = 12V**
- **LOAD STEP = 200mA TO 2A**

- **VIN = 12V**
- **VOUT = 12V**
- **LOAD STEP = 300mA TO 3A**

- **VIN = 18V**
- **VOUT = 12V**
- **LOAD STEP = 300mA TO 3A**

**Line Transient**

- **VIN = 6V**
- **VOUT (AC) = 30V TO 5V**
- **IOUT = 2A/DIV**

- **VIN = 12V**
- **VOUT (AC) = 5V TO 30V**
- **IOUT = 2A/DIV**

For more information [www.linear.com/LTC3789](http://www.linear.com/LTC3789)
PIN FUNCTIONS (SSOP/QFN)

**VFB (Pin 1/Pin 26):** Error Amplifier Feedback Pin. Receives the feedback voltage for the controller from an external resistive divider across the output.

**SS (Pin 2/Pin 27):** External Soft-Start Input. The LTC3789 regulates the VFB voltage to the smaller of 0.8V or the voltage on the SS pin. A internal 3µA pull-up current source is connected to this pin. A capacitor to ground at this pin sets the ramp time to final regulated output voltage.

**SENSE+ (Pin 3/Pin 28):** The (+) Input to the Current Sense Comparator. The ITH pin voltage and controlled offsets between the SENSE– and SENSE+ pins, in conjunction with RSENSE, set the current trip threshold.

**SENSE– (Pin 4/Pin 1):** The (–) Input to the Current Sense Comparator.

**ITH (Pin 5/Pin 2):** Error Amplifier Output and Switching Regulator Compensation Point. The channel's current comparator trip point increases with this control voltage.

**SGND (Pin 6/Pins 3, Exposed Pad Pin 29):** Small Signal Ground. Must be routed separately from high current grounds to the common (–) terminals of the Cin capacitors. In the QFN package, the exposed pad is SGND. It must be soldered to PCB ground for rated thermal performance.

**MODE/PLLIN (Pin 7/Pin 4):** Mode Selection or External Synchronization Input to Phase Detector. This is a dual-purpose pin. When external frequency synchronization is not used, this pin selects the operating mode. The pin can be tied to SGND or INTVCC. SGND or below 0.8V enables forced continuous mode. INTVCC enables pulse-skipping mode. For external sync, apply a clock signal to this pin. The internal PLL will synchronize the internal oscillator to the clock, and forced continuous mode will be enabled. The PLL composition network is integrated into the IC.

**FREQ (Pin 8/Pin 5):** Frequency Set Pin. There is a precision 10µA current flowing out of this pin. A resistor to ground sets a voltage which, in turn, programs the frequency. Alternatively, this pin can be driven with a DC voltage to vary the frequency of the internal oscillator.

**RUN (Pin 9/Pin 6):** Run Control Input. Forcing the pin below 0.5V shuts down the controller, reducing quiescent current. There are 1.2µA pull-up currents for this pin. Once the RUN pin rises above 1.22V, the IC is turned on, and an additional 5µA pull-up current is added to the pin.

**VINSNS (Pin 10/Pin 7):** VIN Sense Input to the Buck-Boost Transition Comparator. Connect this pin to the drain of the top N-channel MOSFET on the input side.

**VOUTSNS (Pin 11/Pin 8):** VOUT Sense Input to the Buck-Boost Transition Comparator. Connect this pin to the VOUT.

**ILIM (Pin 12/Pin 9):** Input/Output Average Current Range Input. This pin tied to SGND, INTVCC or left floating, sets the maximum average current sense threshold.

**ILIMS* (Pin 13/Pin 10):** The (+) Input to the Input/Output Average Current Sense Amplifier.

**ILIMS– (Pin 14/Pin 11):** The (–) Input to the Input/Output Average Current Sense Amplifier.

**TRIM (Pin 15/Pin 12):** Tie this pin to GND for normal operation. Do not allow this pin to float.

**EXTVCC (Pin 20/Pin 17):** External Power Input to an Internal LDO Connected to INTVCC. This LDO supplies INTVCC power, bypassing the internal LDO powered from VIN whenever EXTVCC is higher than 4.8V. See EXTVCC Connection in the Applications Information section. Do not exceed 14V on this pin.
**PIN FUNCTIONS**  
(SSOP/QFN)

**INTV\textsubscript{CC} (Pin 21/Pin 18):** Output of the Internal Linear Low Dropout Regulator. The driver and control circuits are powered from this voltage source. Must be bypassed to power ground with a minimum of 4.7\( \mu \)F tantalum, ceramic, or other low ESR capacitor.

**V\textsubscript{IN} (Pin 22/Pin 19):** Main Supply Pin. A bypass capacitor should be tied between this pin and the power ground pin.

**BG1, BG2 (Pins 23, 19/Pins 20, 16):** High Current Gate Drives for Bottom (Synchronous) N-Channel MOSFETs. Voltage swing at these pins is from ground to INTV\textsubscript{CC}.

**PGND (Pin 24/Pin 21):** Driver Power Ground. Connects to C\textsubscript{OUT} and R\textsubscript{SENSE} (\( -\) ) terminal(s) of C\textsubscript{IN}.

**BOOST1, BOOST2 (Pins 25, 18/Pins 22, 15):** Bootstrapped Supplies to the Top Side Floating Drivers. Capacitors are connected between the BOOST and SW pins and Schottky diodes are tied between the BOOST and INTV\textsubscript{CC} pins. Voltage swing at the BOOST1 pin is from INTV\textsubscript{CC} to (\( V\text{IN} + \text{INTV}_{\text{CC}} \)). Voltage swing at the BOOST2 pin is from INTV\textsubscript{CC} to (\( V\text{OUT} + \text{INTV}_{\text{CC}} \)).

**TG1, TG2 (Pins 26, 17/Pins 23, 14):** High Current Gate Drives for Top N-Channel MOSFETs. These are the outputs of floating drivers with a voltage swing equal to INTV\textsubscript{CC} – 0.5V superimposed on the switch node voltage SW.

**SW1, SW2 (Pins 27, 16/Pins 24, 13):** Switch Node Connections to Inductors. Voltage swing at the SW1 pin is from a Schottky diode (external) voltage drop below ground to V\text{IN}. Voltage swing at the SW2 pin is from a Schottky diode voltage drop below ground to V\text{OUT}.

**PGOOD (Pin 28/Pin 25):** Open-Drain Logic Output. PGOOD is pulled to ground when the voltage on the V\text{FB} pin is not within \( \pm10\% \) of its regulation window, after the internal 20\( \mu \)s power-bad mask timer expires.
OPERATION

MAIN CONTROL LOOP

The LTC3789 is a current mode controller that provides an output voltage above, equal to or below the input voltage. The LTC proprietary topology and control architecture employs a current-sensing resistor. The inductor current is controlled by the voltage on the $I_{TH}$ pin, which is the output of the error amplifier EA. The $V_{FB}$ pin receives the voltage feedback signal, which is compared to the internal reference voltage by the EA. If the input/output current regulation loop is implemented, the sensed inductor current is controlled by either the sensed feedback voltage or the input/output current.

INTVCC/EXTVCC Power

Power for the top and bottom MOSFET drivers and most other internal circuitry is derived from the INTVCC pin. When the EXTVCC is left open or tied to a voltage less than 4.5V, an internal 5.5V low dropout (LDO) regulator supplies INTVCC power from $V_{IN}$. If EXTVCC is taken above 4.8V, the 5.5V regulator is turned off, and another LDO regulates INTVCC from EXTVCC. The EXTVCC LDO allows the INTVCC power to be derived from a high efficiency external source such as the LTC3789 regulator output to reduce IC power dissipation. The absolute maximum voltage on EXTVCC is 14V.

Internal Charge Pump

Each top MOSFET driver is biased from the floating bootstrap capacitors $C_A$ and $C_B$, which are normally recharged by INTVCC through an external diode when the top MOSFET is turned off. When the LTC3789 operates exclusively in the buck or boost regions, one of the top MOSFETs is constantly on. An internal charge pump recharges the bootstrap capacitor to compensate for the small leakage current through the bootstrap diode so that the MOSFET can be kept on. However, if a high leakage diode is used such that the internal charge pump cannot provide sufficient charges to the external bootstrap capacitor, an internal UVLO comparator, which constantly monitors the drop across the capacitor, will sense the $(BOOST – SW)$ voltage when it is below 3.6V. It will turn off the top MOSFET for about one-twelfth of the clock period every four cycles to allow $C_A$ or $C_B$ to recharge.

Shutdown and Start-Up

The controller can be shut down by pulling the RUN pin low. When the RUN pin voltage is below 0.5V, the LTC3789 goes into low quiescent current mode. Releasing RUN allows an internal 1.2μA current to pull up the pin and enable the controller. When RUN is above the accurate threshold of 1.22V, the internal LDO will power up the INTVCC. At the same time, a 6μA pull-up current will kick in to provide more RUN pin hysteresis. The RUN pin may be externally pulled up or driven directly by logic. Be careful not to exceed the absolute maximum rating of 6V on this pin.

The start-up of the controller’s output voltage $V_{OUT}$ is controlled by the voltage on the SS pin. When the voltage on the SS pin is less than the 0.8V internal reference, the LTC3789 regulates the $V_{FB}$ voltage to the SS voltage instead of the 0.8V reference. This allows the SS pin to be used to program soft-start by connecting an external capacitor from the SS pin to SGND. An internal 3μA pull-up current charges this capacitor, creating a voltage ramp on the SS pin. As the SS voltage rises linearly from 0V to 0.8V (and beyond), the output voltage $V_{OUT}$ rises smoothly from zero to its final value. Alternatively, the SS pin can be used to cause the start-up of $V_{OUT}$ to track that of another supply. When RUN is pulled low to disable the controller, or when INTVCC is below the undervoltage lockout threshold of 3.4V, the SS pin is pulled low by an internal MOSFET. In undervoltage lockout, the controller is disabled and the external MOSFETs are held off.
OPERATION

POWER SWITCH CONTROL

Figure 1 shows a simplified diagram of how the four power switches are connected to the inductor, V<sub>IN</sub>, V<sub>OUT</sub> and GND. Figure 2 shows the regions of operation for the LTC3789 as a function of duty cycle, D. The power switches are properly controlled so the transfer between regions is continuous.

Buck Region (V<sub>IN</sub>> V<sub>OUT</sub>)

Switch D is always on and switch C is always off in this region. At the start of every cycle, synchronous switch B is turned on first. Inductor current is sensed when synchronous switch B is turned on. After the sensed inductor valley current falls below a reference voltage, which is proportional to V<sub>ITH</sub>, synchronous switch B is turned off and switch A is turned on for the remainder of the cycle. Switches A and B will alternate, behaving like a typical synchronous buck regulator. The duty cycle of switch A increases until the maximum duty cycle of the converter reaches D<sub>MAX_BUCK</sub>, given by:

\[
D_{\text{MAX_BUCK}} = \left(1 - \frac{1}{12}\right) \cdot 100\% = 91.67\%
\]

Figure 3 shows typical buck region waveforms. If V<sub>IN</sub> approaches V<sub>OUT</sub>, the buck-boost region is reached.

Buck-Boost Region (V<sub>IN</sub> = V<sub>OUT</sub>)

When V<sub>IN</sub> is close to V<sub>OUT</sub>, the controller enters buck-boost region. Figure 4 shows the typical waveforms in this region. At the beginning of a clock cycle, if the controller starts with B and D on, the controller first operates as a buck region. When I<sub>CMP</sub> trips, switch B is turned off, and switch A is turned on. At 120° clock phase, switch C is turned on. The LTC3789 starts to operate as a boost until I<sub>CMP</sub> trips. Then, switch D is turned on for the remainder of the clock period. If the controller starts with switches A and C on, the controller first operates as a boost, until I<sub>CMP</sub> trips and switch D is turned on. At 120°, switch B is turned on, making it operate as a buck. Then, I<sub>CMP</sub> trips, turning switch B off and switch A on for the remainder of the clock period.

Boost Region (V<sub>IN</sub>> V<sub>OUT</sub>)

Switch A is always on and synchronous switch B is always off in the boost region. In every cycle, switch C is turned on first. Inductor current is sensed when synchronous switch C is turned on. After the sensed inductor peak current exceeds what the reference voltage demands, which is proportional to V<sub>ITH</sub>, switch C is turned off and synchronous switch D is turned on for the remainder of the cycle. Switches C and D will alternate, behaving like a typical synchronous boost regulator.
The duty cycle of switch C decreases until the minimum duty cycle of the converter reaches \( D_{\text{MIN BOOST}} \), given by:

\[
D_{\text{MIN BOOST}} = \left( \frac{1}{12} \right) \cdot 100\% = 8.33\%
\]

Figure 5 shows typical boost region waveforms. If \( V_{\text{IN}} \) approaches \( V_{\text{OUT}} \), the buck-boost region is reached.

Light Load Current Operation

The LTC3789 can be enabled to enter pulse-skipping mode or forced continuous conduction mode. To select forced continuous operation, tie the MODE/PLLIN pin to a DC voltage below 0.8V (e.g., SGND). To select pulse-skipping mode of operation, tie the MODE/PLLIN pin to INTVCC.

When the LTC3789 enters pulse-skipping mode, in the boost region, synchronous switch D is held off whenever reverse current through switch A is detected. At very light loads, the current comparator, \( I_{\text{CMP}} \), may remain tripped for several cycles and force switch C to stay off for the same number of cycles (i.e., skipping pulses). In the buck region, the inductor current is not allowed to reverse. Synchronous switch B is held off whenever reverse current on the inductor is detected. At very light loads, the current comparator, \( I_{\text{CMP}} \), may remain untripped for several cycles, holding switch A off for the same number of cycles. Synchronous switch B also remains off for the skipped cycles. In the buck-boost region, the controller operates alternatively in boost and buck region in one clock cycle, as in continuous operation. A small amount of reverse current is allowed, to minimize ripple. For the same reason, a narrow band of continuous buck and boost operation is allowed on the high and low line ends of the buck-boost region.

Output Overvoltage

If the output voltage is higher than the value commanded by the \( V_{\text{FB}} \) resistor divider, the LTC3789 will respond according to the mode and region of operation. In continuous conduction mode, the LTC3789 will sink current into the input. If the input supply is capable of sinking current, the LTC3789 will allow up to about 160mV/R_{\text{SENSE}} to be sunk into the input. In pulse-skipping mode and in the buck or boost regions, switching will stop and the output will be allowed to remain high. In pulse-skipping mode, and in the buck/boost region as well as the narrow band of continuous boost operation that adjoins it, current sunk into the input through switch A is limited to approximately 40mV/R_{\text{DS(ON)}} of switch A. If this level is reached, switching will stop and the output will rise. In pulse-skipping mode, and in the narrow continuous buck region that adjoins the buck/boost region, current sunk into the input through \( R_{\text{SENSE}} \) is limited to approximately 40mV/R_{\text{SENSE}}.
OPERATION

Constant-Current Regulation

The LTC3789 provides a constant-current regulation loop for either input or output current. A sensing resistor close to the input or output capacitor will sense the input or output current. When the current exceeds the programmed current limit, the voltage on the \( I_{TH} \) pin will be pulled down to maintain the desired maximum input or output current. The input current limit function prevents overloading the DC input source, while the output current limit provides a building block for battery charger or LED driver applications. It can also serve as an extra current limit protection for a constant-voltage regulation application. The input/output current limit function has an operating voltage range of GND to the absolute maximum \( V_{OUT} \) (\( V_{IN} \)).

Frequency Selection and Phase-Locked Loop (FREQ and MODE/PLLIN Pins)

The selection of switching frequency is a trade-off between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger inductance and/or capacitance to maintain low output ripple voltage. The switching frequency of the LTC3789’s controllers can be selected using the FREQ pin. If the MODE/PLLIN pin is not being driven by an external clock source, the FREQ pin can be used to program the controller’s operating frequency from 200kHz to 600kHz.

Switching frequency is determined by the voltage on the FREQ pin. Since there is a precision 10µA current flowing out of the FREQ pin, the user can program the controller’s switching frequency with a single resistor to SGND. A curve is provided in the Applications Information section to show the relationship between the voltage on the FREQ pin and the switching frequency.

A phase-locked loop (PLL) is integrated on the LTC3789 to synchronize the internal oscillator to an external clock source driving the MODE/PLLIN pin. The controller operates in forced continuous mode when it is synchronized. The PLL filter network is integrated inside the LTC3789. The PLL is capable of locking to any frequency within the range of 200kHz to 600kHz. The frequency setting resistor should always be present to set the controller’s initial switching frequency before locking to the external clock.

Power Good (PGOOD) Pins

The PGOOD pin is connected to the open drain of an internal N-channel MOSFET. When \( V_{FB} \) is not within ±10% of the 0.8V reference voltage, the PGOOD pin is pulled low. The PGOOD pin is also pulled low when \( V_{RUN} \) is below 1.22V or when the LTC3789 is in the soft-start phase. There is an internal 20µs power good or bad mask when \( V_{FB} \) goes in or out of the ±10% window. The PGOOD pin is allowed to be pulled up by an external resistor to INT\( V_{CC} \) or an external source of up to 6V.

Short-Circuit Protection, Current Limit and Current Limit Foldback

The maximum current threshold of the controller is limited by a voltage clamp on the \( I_{TH} \) pin. In every boost cycle, the sensed maximum peak voltage is limited to 140mV. In every buck cycle, the sensed maximum valley voltage is limited to 90mV. In the buck-boost region, only peak sensed voltage is limited by the same threshold as in the boost region.

The LTC3789 includes current foldback to help limit load current when the output is shorted to ground. If the output falls below 50% of its nominal output level, then the maximum sense voltage is progressively lowered from its maximum value to one-third of the maximum value. Foldback current limiting is disabled during the soft-start. Under short-circuit conditions, the LTC3789 will limit the current by operating as a buck with very low duty cycles, and by skipping cycles. In this situation, synchronous switch B will dissipate most of the power (but less than in normal operation).
The Typical Application on the first page is a basic LTC3789 application circuit. External component selection is driven by the load requirement, and begins with the selection of RSENSE and the inductor value. Next, the power MOSFETs are selected. Finally, C_IN and C_OUT are selected. This circuit can be configured for operation up to an input voltage of 38V.

RSENSE Selection and Maximum Output Current

RSENSE is chosen based on the required output current. The current comparator threshold sets the peak of the inductor current in the boost region and the maximum inductor valley current in the buck region. In the boost region, the maximum average load current at V_IN(MIN) is:

\[ I_{OUT(MAX,BOOST)} = \left( \frac{140mV}{R_{SENSE}} - \frac{\Delta I_L}{2} \right) \cdot \frac{V_{IN(MIN)}}{V_{OUT}} \]

where \( \Delta I_L \) is peak-to-peak inductor ripple current. In the buck region, the maximum average load current is:

\[ I_{OUT(MAX,BUCK)} = \frac{90mV}{R_{SENSE}} + \frac{\Delta I_L}{2} \]

Figure 6 shows how \( I_{LOAD(MAX)} \cdot R_{SENSE} \) varies with input and output voltage.

The maximum current sensing RSENSE value for the boost region is:

\[ R_{SENSE(MAX)} = \frac{2 \cdot 140mV \cdot V_{IN(MIN)}}{2 \cdot I_{OUT(MAX,BOOST)} \cdot V_{OUT} + \Delta I_{BOOST} \cdot V_{IN(MIN)}} \]

The maximum current sensing RSENSE value for the buck region is:

\[ R_{SENSE(MAX)} = \frac{2 \cdot 90mV}{2 \cdot I_{OUT(MAX,BUCK)} - \Delta I_{BUCK}} \]

The final RSENSE value should be lower than the calculated RSENSE(MAX) in both the boost and buck regions. A 20% to 30% margin is usually recommended.

Programming Input/Output Current Limit

As shown in Figures 7 and 8, input/output current sense resistor RSENSE2 should be placed between the bulk capacitor for V_IN/V_OUT and the decoupling capacitor. A lowpass filter formed by R_F and C_F is recommended to reduce the switching noise and stabilize the current loop. The input/output current limit is set by the I_LIM pin for 50mV, 100mV or 140mV with I_LIM pulled to the GND, floating, or tied to INTVCC, respectively. If input/output current limit is not desired, the IOSENSE+ and IOSENSE− pins should be shorted to either V_OUT or V_IN.

![Figure 6. Load Current vs V_IN/V_OUT](image)

![Figure 7. Programming Output Current Limit](image)

![Figure 8. Programming Input Current Limit](image)
APPLICATIONS INFORMATION

With the typical 100Ω resistors shown here, the value of capacitor C_F should be 1µF to 2.2µF. The current loop’s transfer function should approximate that of the voltage loop. Crossover frequency should be one-tenth the switching frequency, and gain should decrease by 20dB/decade. Similar current and voltage loop transfer functions will ensure overall system stability.

When the I_OSENSE common mode voltage is above ~3.2V, the I_OSENSE- pin sources 10µA. The I_OSENSE+ pin, however, sources 18.3µA, 26.6µA and 35µA when the I_LIM pin is low, floating, and high, respectively, and when a constant current is being regulated. The error introduced by this mismatch can be offset to a first order by scaling the I_OSENSE+ and I_OSENSE- resistors accordingly. For example, if the I_OSENSE+ branch has a 100Ω resistor, the 1.83mV across it can be replicated in the I_OSENSE- branch by using a 182Ω resistor.

When the I_OSENSE common mode voltage falls below ~3.2V by a diode drop, the I_OSENSE current decreases linearly; it reaches approximately −300µA at zero volts. The values of the diode drop and maximum current sinking can vary by 20% to 30% due to process variation. Ensure that I_OSENSE common mode voltage never exceeds its absolute maximum of 0.3V below ground. Pay special attention to short-circuit conditions in high power applications.

Slope Compensation

Slope compensation provides stability in constant-frequency architectures by preventing subharmonic oscillations at high duty cycles in boost operation and at low duty cycles in buck operation. This is accomplished internally by adding a compensating ramp to the inductor current signal at duty cycles in excess of 40% in the boost region, or subtracting a ramp from the inductor current signal at lower than 40% duty cycles in the buck region. Normally, this results in a reduction of maximum inductor peak current for duty cycles >40% in the boost region, or an increase of maximum inductor current for duty cycles <40% in the buck region. However, the LTC3789 uses a scheme that counteracts this compensating ramp, which allows the maximum inductor current to remain unaffected throughout all duty cycles.

Phase-Locked Loop and Frequency Synchronization

The LTC3789 has a phase-locked loop (PLL) comprised of an internal voltage-controlled oscillator (VCO) and a phase detector. This allows the turn-on of the top MOSFET of the controller to be locked to the rising edge of an external clock signal applied to the MODE/PLLIN pin. The phase detector is an edge sensitive digital type that provides zero degrees phase shift between the external and internal oscillators. This type of phase detector does not exhibit false locking to harmonics of the external clock.

The output of the phase detector is a pair of complementary current sources that charge or discharge the internal filter network. There is a precision 10µA of current flowing out of the FREQ pin. This allows a single resistor to SGND to set the switching frequency when no external clock is applied to the MODE/PLLIN pin. The internal switch between FREQ and the integrated PLL filter network is on, allowing the filter network to be at the same voltage on the FREQ pin. Operating frequency is shown in Figure 9 and specified in the Electrical Characteristics table. If an external clock is detected on the MODE/PLLIN pin, the internal switch previously mentioned will turn off and isolate the influence of the FREQ pin. Note that the LTC3789 can only be synchronized to an external

![Figure 9. Relationship Between Oscillator Frequency and Voltage at the FREQ Pin](image-url)
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clock whose frequency is within range of the LTC3789’s internal VCO. This is guaranteed to be between 200kHz and 600kHz. A simplified block diagram is shown in Figure 10.

For a given ripple the inductance terms in continuous mode are as follows:

\[
L_{\text{BOOST}} > \frac{V_{\text{IN(MIN)}}^2 \cdot (V_{\text{OUT}} - V_{\text{IN(MIN)}}) \cdot 100}{f \cdot I_{\text{OUT(MAX)}} \cdot \% \text{Ripple} \cdot V_{\text{OUT}}^2} \text{ H},
\]

\[
L_{\text{BUCK}} > \frac{V_{\text{OUT}} \cdot (V_{\text{IN(MAX)}} - V_{\text{OUT}}) \cdot 100}{f \cdot I_{\text{OUT(MAX)}} \cdot \% \text{Ripple} \cdot V_{\text{IN(MAX)}}} \text{ H}
\]

where:

- \(f\) is operating frequency, Hz
- \% Rippled is allowable inductor current ripple
- \(V_{\text{IN(MIN)}}\) is minimum input voltage, V
- \(V_{\text{IN(MAX)}}\) is maximum input voltage, V
- \(V_{\text{OUT}}\) is output voltage, V
- \(I_{\text{OUT(MAX)}}\) is maximum output load current, A

For high efficiency, choose an inductor with low core loss, such as ferrite. Also, the inductor should have low DC resistance to reduce the \(I^2R\) losses, and must be able to handle the peak inductor current without saturating. To minimize radiated noise, use a toroid, pot core or shielded bobbin inductor.

\(C_{\text{IN}}\) and \(C_{\text{OUT}}\) Selection

In the boost region, input current is continuous. In the buck region, input current is discontinuous. In the buck region, the selection of input capacitor \(C_{\text{IN}}\) is driven by the need to filter the input square wave current. Use a low ESR capacitor sized to handle the maximum RMS current. For buck operation, the input RMS current is given by:

\[
I_{\text{RMS}} \approx I_{\text{OUT(MAX)}} \cdot \frac{V_{\text{OUT}}}{V_{\text{IN}}} \cdot \sqrt{\frac{V_{\text{IN}}}{V_{\text{OUT}}} - 1}
\]

This formula has a maximum at \(V_{\text{IN}} = 2V_{\text{OUT}}\), where \(I_{\text{RMS}} = I_{\text{OUT(MAX)}}/2\). This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to derate the capacitor.
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In the boost region, the discontinuous current shifts from the input to the output, so C\textsubscript{OUT} must be capable of reducing the output voltage ripple. The effects of ESR (equivalent series resistance) and the bulk capacitance must be considered when choosing the right capacitor for a given output ripple voltage. The steady ripple due to charging and discharging the bulk capacitance is given by:

\[
\text{Ripple (Boost, Cap)} = \frac{I_{\text{OUT (MAX)}} \cdot (V_{\text{OUT}} - V_{\text{IN (MIN)}})}{C_{\text{OUT}} \cdot V_{\text{OUT}} \cdot f}
\]

where C\textsubscript{OUT} is the output filter capacitor.

The steady ripple due to the voltage drop across the ESR is given by:

\[
\Delta V_{\text{BOOST, ESR}} = I_{\text{OUT (MAX, BOOST)}} \cdot \text{ESR}
\]

In buck mode, V\textsubscript{OUT} ripple is given by:

\[
\Delta V_{\text{OUT}} \leq \Delta I_L \cdot (\text{ESR} + 1 / (8 \cdot f \cdot C_{\text{OUT}}))
\]

Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient. Capacitors are now available with low ESR and high ripple current ratings, such as OS-CON and POSCAP.

Power MOSFET Selection and Efficiency Considerations

The LTC3789 requires four external N-channel power MOSFETs, two for the top switches (switches A and D, shown in Figure 1) and two for the bottom switches (switches B and C, shown in Figure 1). Important parameters for the power MOSFETs are the breakdown voltage V\textsubscript{BR, DSS}, threshold voltage V\textsubscript{GS, TH}, on-resistance R\textsubscript{DS(ON)}, reverse transfer capacitance C\textsubscript{RSS} and maximum current I\textsubscript{DS(MAX)}.

The drive voltage is set by the 5.5V INTVCC supply. Consequently, logic-level threshold MOSFETs must be used in LTC3789 applications.

In order to select the power MOSFETs, the power dissipated by the device must be known. For switch A, the maximum power dissipation happens in the boost region, when it remains on all the time. Its maximum power dissipation at maximum output current is given by:

\[
P_{A, BOOST} = \left( \frac{V_{\text{OUT}}}{V_{\text{IN}}} \cdot I_{\text{OUT (MAX)}} \right)^2 \cdot \rho_T \cdot R_{\text{DS(ON)}}
\]

where \(\rho_T\) is a normalization factor (unity at 25°C) accounting for the significant variation in on-resistance with temperature, typically about 0.4%/°C, as shown in Figure 11. For a maximum junction temperature of 125°C, using a value \(\rho_T = 1.5\) is reasonable.

\[\text{Figure 11. Normalized R}_{\text{DS(ON)}} \text{ vs Temperature}\]

Switch B operates in the buck region as the synchronous rectifier. Its power dissipation at maximum output current is given by:

\[
P_{B, BUCK} = \frac{V_{\text{IN}} - V_{\text{OUT}}}{V_{\text{IN}}} \cdot I_{\text{OUT (MAX)}}^2 \cdot \rho_T \cdot R_{\text{DS(ON)}}
\]

Switch C operates in the boost region as the control switch. Its power dissipation at maximum current is given by:

\[
P_{C, BOOST} = \frac{(V_{\text{OUT}} - V_{\text{IN}}) V_{\text{OUT}}}{V_{\text{IN}}^2} \cdot I_{\text{OUT (MAX)}}^2 \cdot \rho_T
\]

\[
\cdot R_{\text{DS(ON)}} + k \cdot \frac{V_{\text{OUT}}^3}{V_{\text{IN}}} \cdot I_{\text{OUT (MAX)}} \cdot C_{\text{RSS}} \cdot f
\]
where $C_{RSS}$ is usually specified by the MOSFET manufacturers. The constant $k$, which accounts for the loss caused by reverse recovery current, is inversely proportional to the gate drive current and has an empirical value of 1.7.

For switch D, the maximum power dissipation happens in the boost region, when its duty cycle is higher than 50%. Its maximum power dissipation at maximum output current is given by:

$$P_{D,BOOST} = \frac{V_{IN}}{V_{OUT}} \cdot \left( \frac{V_{OUT}}{V_{IN}} \cdot I_{OUT(MAX)} \right)^2 \cdot \rho_t \cdot R_{DS(ON)}$$

For the same output voltage and current, switch A has the highest power dissipation and switch B has the lowest power dissipation unless a short occurs at the output.

From a known power dissipated in the power MOSFET, its junction temperature can be obtained using the following formula:

$$T_J = T_A + P \cdot R_{TH(JA)}$$

The $R_{TH(JA)}$ to be used in the equation normally includes the $R_{TH(JC)}$ for the device plus the thermal resistance from the case to the ambient temperature ($R_{TH(JC)}$). This value of $T_J$ can then be compared to the original, assumed value used in the iterative calculation process.

Schottky Diode (D1, D2) Selection

The Schottky diodes, D1 and D2, shown in Figure 13, conduct during the dead time between the conduction of the power MOSFET switches. They are intended to prevent the body diode of synchronous switches B and D from turning on and storing charge during the dead time. In particular, D2 significantly reduces reverse recovery current between switch D turn-off and switch C turn-on, which improves converter efficiency and reduces switch C voltage stress. In order for the diode to be effective, the inductance between it and the synchronous switch must be as small as possible, mandating that these components be placed adjacently.

INTVCC Regulators and EXTVCC

The LTC3789 features a true PMOS LDO that supplies power to INTVCC from the $V_{IN}$ supply. INTVCC powers the gate drivers and much of the LTC3789's internal circuitry. The linear regulator regulates the voltage at the INTVCC pin to 5.5V when $V_{IN}$ is greater than 6.5V. EXTVCC can supply the needed power when its voltage is higher than 4.8V through another on-chip PMOS LDO. Each of these can supply a peak current of 100mA and must be bypassed to ground with a minimum of 1µF ceramic capacitor or low ESR electrolytic capacitor. No matter what type of bulk capacitor is used, an additional 0.1µF ceramic capacitor placed directly adjacent to the INTVCC and PGND pins is highly recommended. Good bypassing is needed to supply the high transient current required by the MOSFET gate drivers and to prevent interaction between the channels.

High input voltage applications in which large MOSFETs are being driven at high frequencies may cause the maximum junction temperature rating for the LTC3789 to be exceeded. The INTVCC current, which is dominated by the gate charge current, may be supplied by either the 5.5V linear regulator from $V_{IN}$ or the 5.5V LDO from EXTVCC. When the voltage on the EXTVCC pin is less than 4.5V, the linear regulator from $V_{IN}$ is enabled. Power dissipation for the IC in this case is highest and is equal to $V_{IN} \cdot I_{INTVCC}$. The gate charge current is dependent on operating frequency, as discussed in the Efficiency Considerations section. The junction temperature can be estimated by using the equations given in Note 3 of the Electrical Characteristics. For example, the LTC3789 INTVCC current is limited to less than 24mA from a 24V supply in the SSOP package and not using the EXTVCC supply:

$$T_J = 70°C + (28mA)(24V)(80°C/W) = 125°C$$

To prevent the maximum junction temperature from being exceeded, the input supply current must be checked while operating in continuous conduction mode (MODE.PLLIN = SGND) at maximum $V_{IN}$. When the voltage applied to EXTVCC rises above 4.8V, the INTVCC linear regulator from $V_{IN}$ is turned off and the linear regulator from EXTVCC is turned on and remains on as long as the voltage applied to EXTVCC remains above 4.5V. Using EXTVCC allows the MOSFET driver and control power to be derived from the LTC3789's switching regulator output during normal operation and from the $V_{IN}$ when the output is out of regulation (e.g., start-up, short-circuit). Do not apply more than 14V to EXTVCC.
APPLICATIONS INFORMATION

Significant efficiency and thermal gains can be realized by powering EXTVCC from the output, since the VIN current resulting from the driver and control currents will be scaled by a factor of (Duty Cycle)/(Switcher Efficiency).

Tying the EXTVCC pin to a 12V output reduces the junction temperature in the previous example from 125°C to 97°C:

\[ T_J = 70°C + (28mA)(12V)(80°C/W) = 97°C \]

Powering EXTVCC from the output can also provide enough gate drive when VIN drops below 5V. This allows a wider operating range for VIN after the controller start into regulation.

The following list summarizes the three possible connections for EXTVCC:

1. EXTVCC left open (or grounded). This will cause INTVCC to be powered from the internal 5.5V regulator at the cost of a small efficiency penalty.

2. EXTVCC connected directly to VOUT (4.7V < VOUT < 14V). This is the normal connection for the 5.5V regulator and provides the highest efficiency.

3. EXTVCC connected to an external supply. If an external supply is available in the 4.7V to 14V range, it may be used to power EXTVCC provided it is compatible with the MOSFET gate drive requirements.

Note that there is an internal body diode from INTVCC to VIN. When INTVCC is powered from EXTVCC and VIN drops lower than 4.5V, the diode will create a back-feeding path from EXTVCC to VIN. To limit this back-feeding current, a 10Ω ~ 15Ω resistor is recommended between the system VIN voltage and the chip VIN pin. To truly eliminate this back-feeding current, a blocking Schottky diode should be connected between the system VIN and the chip VIN.

Output Voltage

The LTC3789 output voltage is set by an external feed-back resistive divider carefully placed across the output capacitor. The resultant feedback signal is compared with the internal precision 0.8V voltage reference by the error amplifier. The output voltage is given by the equation:

\[ V_{OUT} = 0.8V \cdot \left(1 + \frac{R2}{R1}\right) \]

where R1 and R2 are defined in Figure 13.

Topside MOSFET Driver Supply (CA, DA, CB, DB)

Referring to Figure 13, the external bootstrap capacitors CA and CB connected to the BOOST1 and BOOST2 pins supply the gate drive voltage for the topside MOSFET switches A and D. When the top switch A turns on, the switch node SW1 rises to VIN and the BOOST1 pin rises to approximately VIN + INTVCC. When the bottom switch B turns on, the switch node SW1 drops to low and the boost capacitor CA is charged through DA from INTVCC. When the top switch D turns on, the switch node SW2 rises to VOUT and the BOOST2 pin rises to approximately VOUT + INTVCC. When the bottom switch C turns on, the switch node SW2 drops to low and the boost capacitor CB is charged through DA from INTVCC. The boost capacitors CA and CB need to store about 100 times the gate charge required by the top switches A and D. In most applications, a 0.1µF to 0.47µF, X5R or X7R dielectric capacitor is adequate.

Undervoltage Lockout

The LTC3789 has two functions that help protect the controller in case of undervoltage conditions. A precision UVLO comparator constantly monitors the INTVCC voltage to ensure that an adequate gate-drive voltage is present. It locks out the switching action when INTVCC is below 3.4V. To prevent oscillation when there is a disturbance on the INTVCC, the UVLO comparator has 400mV of precision hysteresis.

Another way to detect an undervoltage condition is to monitor the VIN supply. Because the RUN pin has a precision turn-on reference of 1.22V, one can use a resistor divider to VIN to turn on the IC when VIN is high enough. An extra 5µA of current flows out of the RUN pin once its voltage passes 1.22V. One can program the hysteresis of the run comparator by adjusting the values of the resistive divider.
Soft-Start Function

When a capacitor is connected to the SS pin, a soft-start current of 3µA starts to charge the capacitor. A soft-start function is achieved by controlling the output ramp voltage according to the ramp rate on the SS pin. Current foldback is disabled during this phase to ensure smooth soft-start. When the chip is in the shutdown state with its RUN pin voltage below 1.22V, the SS pin is actively pulled to ground. The soft-start range is defined to be the voltage range from 0V to 0.8V on the SS pin. The total soft-start time can be calculated as:

$$t_{SOFTSTART} = \frac{0.8 \cdot C_{SS}}{3\mu A}$$

Regardless of the mode selected by the MODE/PLLIN pin, the regulator will always start in pulse-skipping mode up to SS = 0.8V.

Fault Conditions: Current Limit and Current Foldback

The maximum inductor current is inherently limited in a current mode controller by the maximum sense voltage. In the boost region, maximum sense voltage and the sense resistance determine the maximum allowed inductor peak current, which is:

$$I_{L(MAX,BOOST)} = \frac{140mV}{R_{SENSE}}$$

In the buck region, maximum sense voltage and the sense resistance determine the maximum allowed inductor valley current, which is:

$$I_{L(MAX,BUCK)} = \frac{90mV}{R_{SENSE}}$$

To further limit current in the event of a short circuit to ground, the LTC3789 includes foldback current limiting. If the output falls by more than 50%, then the maximum sense voltage is progressively lowered to about one-third of its full value.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Although all dissipative elements in circuit produce losses, four main sources account for most of the losses in LTC3789 circuits:

1. DC I²R losses. These arise from the resistances of the MOSFETs, sensing resistor, inductor and PC board traces and cause the efficiency to drop at high output currents.

2. MOSFET Transition loss. This loss arises from the brief amount of time switch A or switch C spends in the saturated region during switch node transitions. It depends upon the input voltage, load current, driver strength and MOSFET capacitance, among other factors.

3. INTV CC current. This is the sum of the MOSFET driver and control currents. This loss can be reduced by supplying INTV CC current through the EXTV CC pin from a high efficiency source, such as the output (if 4.7V < VOUT < 14V) or alternate supply if available.

4. C IN and C OUT loss. The input capacitor has the difficult job of filtering the large RMS input current to the regulator in buck mode. The output capacitor has the more difficult job of filtering the large RMS output current in boost mode. Both C IN and C OUT are required to have low ESR to minimize the AC I²R loss and sufficient capacitance to prevent the RMS current from causing additional upstream losses in fuses or batteries.

5. Other losses. Schottky diodes D1 and D2 are responsible for conduction losses during dead time and light load conduction periods. Inductor core loss should also be considered. Switch C causes reverse recovery current loss in boost mode.

When making adjustments to improve efficiency, the input current is the best indicator of changes in efficiency. If one makes a change and the input current decreases, then the efficiency has increased. If there is no change in input current, then there is no change in efficiency.
Design Example

\( V_{\text{IN}} = 5\text{V} \) to \( 18\text{V} \)

\( V_{\text{OUT}} = 12\text{V} \)

\( I_{\text{OUT(\text{MAX})}} = 5\text{A} \)

\( f = 400\text{kHz} \)

Maximum ambient temperature = \( 60^\circ\text{C} \)

Set the frequency at 400kHz by applying 1.2V on the FREQ pin (see Figure 7). The 10\( \mu\text{A} \) current flowing out of the FREQ pin will give 1.2V across a 120k resistor to GND. The inductance value is chosen first based on a 30% ripple current assumption. In the buck region, the ripple current is:

\[
\Delta I_{L,\text{BUCK}} = \frac{V_{\text{OUT}}}{f \cdot L} \cdot \left(1 - \frac{V_{\text{OUT}}}{V_{\text{IN}}}\right)
\]

\( I_{\text{RIPPLE,BUCK}} = \frac{\Delta I_{L,\text{BUCK}} \cdot 100}{I_{\text{OUT}}} \% \)

The highest value of ripple current occurs at the maximum input voltage. In the boost region, the ripple current is:

\[
\Delta I_{L,\text{BOOST}} = \frac{V_{\text{IN}}}{f \cdot L} \cdot \left(1 - \frac{V_{\text{IN}}}{V_{\text{OUT}}}\right)
\]

\( I_{\text{RIPPLE,BOOST}} = \frac{\Delta I_{L,\text{BOOST}} \cdot 100}{I_{\text{IN}}} \% \)

The highest value of ripple current occurs at \( V_{\text{IN}} = V_{\text{OUT}}/2 \).

A 6.8\( \mu\text{H} \) inductor will produce 11% ripple in the boost region (\( V_{\text{IN}} = 6\text{V} \)) and 29% ripple in the buck region (\( V_{\text{IN}} = 18\text{V} \)).

The \( R_{\text{SENSE}} \) resistor value can be calculated by using the maximum current sense voltage specification with some accommodation for tolerances.

\[
R_{\text{SENSE}} = 2 \cdot 140\text{mV} \cdot \frac{V_{\text{IN(MIN)}}}{2 \cdot I_{\text{OUT(\text{MAX,BUCC})}} \cdot V_{\text{OUT}} + \Delta I_{L,\text{BOOST}} \cdot V_{\text{IN(MIN)}}}
\]

Select an \( R_{\text{SENSE}} \) of 10mΩ.

Output voltage is 12V. Select R1 as 20k. R2 is:

\[
R_2 = \frac{V_{\text{OUT}} \cdot R_1}{0.8} - R_1
\]

Select R2 as 280k. Both R1 and R2 should have a tolerance of no more than 1%.

Selecting MOSFET Switches

The MOSFETs are selected based on voltage rating and \( R_{\text{DS(ON)}} \) value. It is important to ensure that the part is specified for operation with the available gate voltage amplitude. In this case, the amplitude is 5.5V and MOSFETs with an \( R_{\text{DS(ON)}} \) value specified at \( V_{\text{GS}} = 4.5\text{V} \) can be used.

Select QA and QB. With 18V maximum input voltage MOSFETs with a rating of at least 30V are used. As we do not yet know the actual thermal resistance (circuit board design and airflow have a major impact) we assume that the MOSFET thermal resistance from junction to ambient is \( 50^\circ\text{C/W} \).

If we design for a maximum junction temperature, \( T_{J(\text{MAX})} = 125^\circ\text{C} \), the maximum \( R_{\text{DS(ON)}} \) value can be calculated. First, calculate the maximum power dissipation:

\[
P_{\text{D(MAX)}} = \left(\frac{T_{J(\text{MAX})} - T_{A(\text{MAX})}}{R_{(j-a)}}\right)
\]

\[
P_{\text{D(MAX)}} = \frac{(125 - 60)}{50} = 1.3\text{W}
\]

The maximum dissipation in QA occurs at minimum input voltage when the circuit operates in the boost region and QA is on continuously. The input current is then:

\[
\frac{V_{\text{OUT}} \cdot I_{\text{OUT(MAX)}}}{V_{\text{IN(MIN)}}}, \text{ OR } 12\text{A}
\]

We calculate a maximum value for \( R_{\text{DS(ON)}} \):

\[
R_{\text{DS(ON)}} \left(125^\circ\text{C}\right) < \frac{P_{D(MAX)}}{I_{\text{IN(MAX)}}^2}
\]

\[
R_{\text{DS(ON)}} \left(125^\circ\text{C}\right) < \frac{1.3\text{W}}{(12\text{A})^2} = 0.009\Omega
\]
The Vishay SiR422DP has a typical $R_{DS(ON)}$ of 0.010Ω at $T_J = 125°C$ and $V_{GS} = 4.5V$.

The maximum dissipation in QB occurs at maximum input voltage when the circuit is operating in the buck region. The dissipation is:

$$P_{B,BUCK} = \frac{V_{IN} - V_{OUT}}{V_{IN}} \cdot I_{OUT(MAX)}^2 \cdot \rho_t \cdot R_{DS(ON)}$$

$$R_{DS(ON)}(125°C) < \frac{1.3W}{\frac{18V}{10} - \frac{12V}{18}} \cdot (5A)^2 = 0.156Ω$$

This seems to indicate that a quite small MOSFET can be used for QB if we only look at power loss. However, with 5A current the voltage drop across 0.156Ω is 0.78V, which means the MOSFET body diode is conducting. To avoid body diode current flow we should keep the maximum voltage drop well below 0.5V, using, for example, Vishay Si4840BDY in the SO-8 package ($R_{DSON(MAX)} = 0.012Ω$).

Select QC and QD. With 12V output voltage we need MOSFETs with 20V or higher rating.

The highest dissipation occurs at minimum input voltage when the inductor current is highest. For switch QC the dissipation is:

$$P_{C,BUCK} = \frac{V_{OUT} - V_{IN}}{V_{IN}} \cdot \frac{I_{OUT(MAX)}}{V_{OUT}} \cdot \rho_t \cdot R_{DS(ON)}$$

$$R_{DS(ON)}(125°C) < \frac{1.3W}{\frac{18V}{10} - \frac{12V}{18}} \cdot (5A)^2$$

Vishay SiR4840Y is a possible choice for QC and QD. The calculated power loss at 5V input voltage is then 1.3W for QC and 0.84W for QD.

$C_{IN}$ is chosen to filter the square current in the buck region. In this mode, the maximum input current peak is:

$$I_{IN,PEAK(MAX,BUCK)} = 5A \cdot \left(1 + \frac{29%}{2}\right) = 5.7A$$

A low ESR (10mΩ) capacitor is selected. Input voltage ripple is 57mV (assuming ESR dominates the ripple).

$C_{OUT}$ is chosen to filter the square current in the boost region. In this mode, the maximum output current peak is:

$$I_{OUT,PEAK(MAX,BUCK)} = \frac{12}{5} \cdot \frac{5}{5} \cdot \left(1 + \frac{11%}{2}\right) = 10.6A$$

A low ESR (5mΩ) capacitor is suggested. This capacitor will limit output voltage ripple to 53mV (assuming ESR dominates the ripple).

PC Board Layout Checklist

The basic PC board layout requires a dedicated ground plane layer. Also, for high current, a multilayer board provides heat sinking for power components.

- The ground plane layer should not have any traces and should be as close as possible to the layer with power MOSFETs.
- Place $C_{IN}$, switch A, switch B and D1 in one compact area. Place $C_{OUT}$, switch C, switch D and D2 in one compact area. One layout example is shown in Figure 12.
- Use immediate vias to connect the components (including the LTC3789’s SGND and PGND pins) to the ground plane. Use several large vias for each power component.
APPLICATIONS INFORMATION

• Use planes for $V_{IN}$ and $V_{OUT}$ to maintain good voltage filtering and to keep power losses low.

• Flood all unused areas on all layers with copper. Flood- ing with copper will reduce the temperature rise of power components. Connect the copper areas to any DC net ($V_{IN}$ or GND). When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3789. These items are also illustrated in Figure 13.

• Segregate the signal and power grounds. All small-signal components should return to the SGND pin at one point, which is then tied to the PGND pin close to the inductor current sense resistor $R_{SENSE}$.

• Place switch B and switch C as close to the controller as possible, keeping the PGND, BG and SW traces short.

• Keep the high dV/dt SW1, SW2, BOOST1, BOOST2, TG1 and TG2 nodes away from sensitive small-signal nodes.

• The path formed by switch A, switch B, D1 and the $C_{IN}$ capacitor should have short leads and PC trace lengths. The path formed by switch C, switch D, D2 and the $C_{OUT}$ capacitor also should have short leads and PC trace lengths.

• The output capacitor (–) terminals should be connected as closely as possible to the (–) terminals of the input capacitor.

• Connect the top driver boost capacitor $C_A$ closely to the BOOST1 and SW1 pins. Connect the top driver boost capacitor $C_B$ closely to the BOOST2 and SW2 pins.

• Connect the output capacitors $C_{IN}$ and output capacitors $C_{OUT}$ closely to the power MOSFETs. These capacitors carry the MOSFET AC current in the boost and buck region.

• Connect $V_{FB}$ pin resistive dividers to the (+) terminals of $C_{OUT}$ and signal ground. A small $V_{FB}$ bypass capacitor may be connected closely to the LTC3789 SGND pin. The R2 connection should not be along the high current or noise paths, such as the input capacitors.

• Route $SENSE^-$ and $SENSE^+$ leads together with minimum PC trace spacing. Avoid having sense lines pass through noisy areas, such as switch nodes. The filter capacitor between $SENSE^+$ and $SENSE^-$ should be as close as possible to the IC. Ensure accurate current sensing with Kelvin connections at the sense resistor. One layout example is shown in Figure 14.

• Connect the $I_{TH}$ pin compensation network closely to the IC, between $I_{TH}$ and the signal ground pins. The capacitor helps to filter the effects of PCB noise and output voltage ripple voltage from the compensation loop.

• Connect the $INTV_{CC}$ bypass capacitor, $C_{VCC}$, closely to the IC, between the $INTV_{CC}$ and the power ground pins. This capacitor carries the MOSFET drivers’ current peaks. An additional 1µF ceramic capacitor placed immediately next to the $INTV_{CC}$ and PGND pins can help improve noise performance substantially.

Figure 12. Switches Layout
Figure 13. LTC3789 12V/5A, Buck-Boost Regulator

Figure 14. Sense Lines Layout
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

GN Package
28-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)

RECOMMENDED SOLDER PAD LAYOUT

NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN INCHES
3. DRAWING NOT TO SCALE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006” (0.152mm) PER SIDE
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010” (0.254mm) PER SIDE
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UFD Package
28-Lead Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1712 Rev B)

NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WXXX-X).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON THE TOP AND BOTTOM OF PACKAGE
## Revision History

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**Related Parts**

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<td>High Efficiency (Up to 98%) Synchronous, 4-Switch Buck-Boost DC/DC Controller</td>
<td>4V ≤ VIN ≤ 36V, 0.8V ≤ VOUT ≤ 30V, 5mm × 5mm QFN-32 and SSOP-24 Packages</td>
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<td>LTC3785</td>
<td>High Efficiency (Up to 98%) Synchronous, 4-Switch Buck-Boost DC/DC Controller</td>
<td>2.7V ≤ VIN ≤ 10V, 2.7V ≤ VOUT ≤ 10V, 4mm × 4mm QFN-24 Package</td>
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<td>High Efficiency Buck-Boost DC/DC µModule™ Regulator Complete Power Supply</td>
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<td>High Efficiency Buck-Boost DC/DC µModule Regulator Complete Power Supply</td>
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<td>High Efficiency Buck-Boost DC/DC µModule Regulator Complete Power Supply</td>
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<td>2A Synchronous Buck-Boost Monolithic DC/DC Converter</td>
<td>1.8V ≤ VIN ≤ 5.5V, 1.8V ≤ VOUT ≤ 5.25V, IQ = 40µA, ISD &lt; 1µA, 3mm × 4mm DFN-14 Package</td>
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