The LT®3782 is a current mode two phase step-up DC/DC converter controller. Its high switching frequency (up to 500kHz) and 2-phase operation reduce system filtering capacitance and inductance requirements.

With 10V gate drive (VCC ≥13V) and 4A peak drive current, the LT3782 can drive most industrial grade high power MOSFETs with high efficiency. For synchronous applications, the LT3782 provides synchronous gate signals with programmable falling edge delay to avoid cross conduction when using external MOSFET drivers. Other features include programmable undervoltage lockout, soft-start, current limit, duty cycle clamp (50% or higher) and slope compensation.

The LT3782 is available in thermally enhanced 28-lead TSSOP and 4mm × 5mm QFN packages.

For new designs use the LT3782A which has improved phase matching.
**ABSOLUTE MAXIMUM RATINGS**

(Note 1)

V\textsubscript{CC} Supply Voltage ........................................... 40V
GBIAS, GBIAS1, GBIAS2 Pin (Externally Forced) ......................... 14V
SYNC, RUN Pin .......................................................... 30V
Operating Junction Temperature Range (Notes 2, 3) .............. –40°C to 125°C

Storage Temperature Range ....................... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ...................... 300°C
SS .............................................................. –0.3V to 6V
SENSE\textsuperscript{1+}, SENSE\textsuperscript{2+}, SENSE\textsuperscript{1–}, SENSE\textsuperscript{2–} .......... –0.3V to 2V

**ORDER INFORMATION**

<table>
<thead>
<tr>
<th>LEAD FREE FINISH</th>
<th>TAPE AND REEL</th>
<th>PART MARKING</th>
<th>PACKAGE DESCRIPTION</th>
<th>TEMPERATURE RANGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>LT3782EFE#PBF</td>
<td>LT3782EFE#TRPBF</td>
<td>LT3782EFE</td>
<td>28-Lead Plastic TSSOP</td>
<td>–40°C to 85°C</td>
</tr>
<tr>
<td>LT3782IFE#PBF</td>
<td>LT3782IFE#TRPBF</td>
<td>LT3782IFE</td>
<td>28-Lead Plastic TSSOP</td>
<td>–40°C to 125°C</td>
</tr>
<tr>
<td>LT3782EUFD#PBF</td>
<td>LT3782EUFD#TRPBF</td>
<td>3782</td>
<td>28-Lead (4mm x 5mm) Plastic QFN</td>
<td>–40°C to 85°C</td>
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<tr>
<th>LEAD BASED FINISH</th>
<th>TAPE AND REEL</th>
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<th>PACKAGE DESCRIPTION</th>
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<td>LT3782EFE#TR</td>
<td>LT3782EFE</td>
<td>28-Lead Plastic SSOP</td>
<td>–40°C to 85°C</td>
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<td>LT3782IFE</td>
<td>LT3782IFE#TR</td>
<td>LT3782IFE</td>
<td>28-Lead Plastic SSOP</td>
<td>–40°C to 125°C</td>
</tr>
<tr>
<td>LT3782EUFD</td>
<td>LT3782EUFD#TR</td>
<td>3782</td>
<td>28-Lead (4mm x 5mm) Plastic QFN</td>
<td>–40°C to 85°C</td>
</tr>
</tbody>
</table>

Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: [http://www.linear.com/leadfree/](http://www.linear.com/leadfree/)
For more information on tape and reel specifications, go to: [http://www.linear.com/tapeandreel/](http://www.linear.com/tapeandreel/)
## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at \( T_A = 25^\circ C \). \( V_{CC} = 13V \), \( R_{SET} = 80k \), no load on any outputs, unless otherwise noted.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Overall Supply Voltage (( V_{CC} ))</td>
<td>●</td>
<td>6</td>
<td>40</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Supply Current (( I_{VCC} ))</td>
<td>( V_C \leq 0.5V ) (Switching Off), ( V_{CC} \leq 40V )</td>
<td>11</td>
<td>16</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Shutdown</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RUN Threshold</td>
<td>●</td>
<td>2.3</td>
<td>2.45</td>
<td>2.6</td>
<td>V</td>
</tr>
<tr>
<td>RUN Threshold Hysteresis</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>80</td>
</tr>
<tr>
<td>Supply Current in Shutdown</td>
<td>( 1V \leq RUN \leq V_{REF}, V_{CC} \leq 30V )</td>
<td>0.4</td>
<td>0.65</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>( RUN \leq 0.3V, V_{CC} \leq 30V )</td>
<td>40</td>
<td>90</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>RUN Pin Input Current</td>
<td>( V_{RUN} = 2.3V )</td>
<td>●</td>
<td>−0.5</td>
<td>−2</td>
<td>μA</td>
</tr>
<tr>
<td>Voltage Amplifier ( g_m )</td>
<td>Reference Voltage (( V_{REF} ))</td>
<td></td>
<td>2.42</td>
<td>2.44</td>
<td>2.464</td>
</tr>
<tr>
<td></td>
<td></td>
<td>●</td>
<td>2.4</td>
<td>2.488</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Transconductance</td>
<td>( V_{VC} = 1V, \Delta I_{VC} = \pm 2\mu A )</td>
<td>●</td>
<td>200</td>
<td>260</td>
</tr>
<tr>
<td></td>
<td>Input Current ( I_{FB} )</td>
<td>( V_{FB} = V_{REF} )</td>
<td>●</td>
<td>0.2</td>
<td>0.6</td>
</tr>
<tr>
<td></td>
<td>( V_C ) High</td>
<td>( I_{VC} = 0 )</td>
<td></td>
<td>1.5</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>( V_C ) Low</td>
<td>( I_{VC} = 0 )</td>
<td></td>
<td>0.35</td>
<td>0.4</td>
</tr>
<tr>
<td></td>
<td>Source Current ( I_{VC} )</td>
<td>( V_{VC} = 0.7V – 1V, V_{FB} = V_{REF} – 100mV )</td>
<td>8</td>
<td>11</td>
<td>14</td>
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<tr>
<td></td>
<td>Sink Current ( I_{VC} )</td>
<td>( V_{VC} = 0.7V – 1V, V_{FB} = V_{REF} + 100mV )</td>
<td>13</td>
<td>20</td>
<td>28</td>
</tr>
<tr>
<td></td>
<td>( V_C ) Threshold for Switching Off (BGATE1, BGATE2 Low)</td>
<td></td>
<td>0.3</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Soft-Start Current ( I_{SS} )</td>
<td>( V_{SS} = 0.1V – 2.8V )</td>
<td>6</td>
<td>10</td>
<td>15</td>
</tr>
<tr>
<td>Current Amplifier CA1, CA2</td>
<td>Voltage Gain ( \Delta V_C/\Delta V_{SENSE} )</td>
<td></td>
<td>4</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Current Limit ( (V_{SENSE1^+} – V_{SENSE1^-}) (V_{SENSE2^+} – V_{SENSE2^-}) )</td>
<td></td>
<td>50</td>
<td>62</td>
<td>80</td>
</tr>
<tr>
<td></td>
<td>Input Current ( (I_{SENSE1^+}, I_{SENSE1^-}, I_{SENSE2^+}, I_{SENSE2^-}) ) ( \Delta V_{SENSE} = 0V )</td>
<td></td>
<td>60</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>Oscillator</td>
<td>Switching Frequency</td>
<td>( R_{SET} = 130k )</td>
<td></td>
<td>130</td>
<td>154</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( R_{SET} = 80k )</td>
<td></td>
<td>212</td>
<td>250</td>
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<tr>
<td></td>
<td></td>
<td>( R_{SET} = 40k )</td>
<td></td>
<td>386</td>
<td>465</td>
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<tr>
<td></td>
<td>Synchronization Pulse Threshold on SYNC Pin</td>
<td>Rising Edge ( V_{SYNC} )</td>
<td></td>
<td>0.8</td>
<td>1.2</td>
</tr>
<tr>
<td></td>
<td>Synchronization Frequency Range</td>
<td>( R_{SET} = 130k )</td>
<td></td>
<td>180</td>
<td>240</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( R_{SET} = 80k )</td>
<td></td>
<td>290</td>
<td>392</td>
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<tr>
<td></td>
<td></td>
<td>( R_{SET} = 40k )</td>
<td></td>
<td>550</td>
<td>715</td>
</tr>
<tr>
<td></td>
<td>( V_{RSET} )</td>
<td>( R_{SET} = 80k )</td>
<td></td>
<td>2.3</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Maximum Duty Cycle</td>
<td>( V_{FB} = V_{REF} – 25mV, R_{SET} &gt; 80k )</td>
<td></td>
<td>90</td>
<td>94</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( R_{SET} = 40k )</td>
<td></td>
<td>83</td>
<td>90</td>
</tr>
<tr>
<td></td>
<td>Duty Cycle Limit</td>
<td>( R_{SET} = 80k, V_{DCL} \leq 0.3V )</td>
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<td>50</td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>( V_{DCL} = 1.2V )</td>
<td></td>
<td>75</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{DCL} = V_{RSET} )</td>
<td></td>
<td>Max Duty Cycle</td>
<td></td>
</tr>
<tr>
<td></td>
<td>DCL Pin Input Current</td>
<td>( V_{DCL} \leq 0.3V )</td>
<td>●</td>
<td>−0.1</td>
<td>−0.3</td>
</tr>
</tbody>
</table>
**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at $T_A = 25^°C$. $V_{CC} = 13V$, $R_{SET} = 80k$, no load on any outputs, unless otherwise noted.

<table>
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<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate Driver</td>
<td>$V_{GBIAS}$</td>
<td>$I_{GBIAS} &lt; 70mA$</td>
<td>●</td>
<td>10.2</td>
<td>11</td>
</tr>
<tr>
<td></td>
<td>$BGATE1$, $BGATE2$ High Voltage</td>
<td>$13V \leq V_{CC} \leq 24V$, $I_{BGATE} = -100mA$</td>
<td>●</td>
<td>7.8</td>
<td>9.2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{CC} = 8V$, $I_{BGATE} = -100mA$</td>
<td>●</td>
<td>3.8</td>
<td>5</td>
</tr>
<tr>
<td></td>
<td>$BGATE1$, $BGATE2$ Source Current (Peak)</td>
<td>Capacitive Load $&gt;22\mu F$</td>
<td>3</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Capacitive Load $&gt;50\mu F$</td>
<td>4</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$BGATE1$, $BGATE2$ Low Voltage</td>
<td>$8V \leq V_{CC} \leq 24V$, $I_{BGATE} = 100mA$</td>
<td>●</td>
<td>0.5</td>
<td>0.7</td>
</tr>
<tr>
<td></td>
<td>$BGATE1$, $BGATE2$ Sink Current (Peak)</td>
<td>Capacitive Load $&gt;22\mu F$</td>
<td>3</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Capacitive Load $&gt;50\mu F$</td>
<td>4</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$SGATE1$, $SGATE2$ High Voltage</td>
<td>$8V \leq V_{CC} \leq 24V$, $I_{SGATE} = -20mA$</td>
<td>●</td>
<td>4.5</td>
<td>5.5</td>
</tr>
<tr>
<td></td>
<td>$SGATE1$, $SGATE2$ Low Voltage</td>
<td>$8V \leq V_{CC} \leq 24V$, $I_{SGATE} = 20mA$</td>
<td>0.5</td>
<td>0.7</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$SGATE1$, $SGATE2$ Peak Current</td>
<td>500pF Load</td>
<td>100</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Delay of $BGATE$ High</td>
<td>DELAY Pin and $R_{SET}$ Pin Shorted</td>
<td>$V_{DELAY} = 1V$</td>
<td>100</td>
<td></td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>$V_{DELAY} = 0.5V$</td>
<td>150</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DELAY} = 0.25V$</td>
<td>250</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>500</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Delay Pin Input Current</td>
<td>$V_{DELAY} = 0.25V$</td>
<td>●</td>
<td>−0.1</td>
<td>−0.3</td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LT3782E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the −40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3782I is guaranteed to meet performance specifications over the full −40°C to 125°C operating junction temperature range.

**Note 3:** This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.
PIN FUNCTIONS (FE/UFD)

SGATE2 (Pin 1/Pin 26): Second Phase Synchronous Drive Signal. An external driver buffer is needed to drive the top synchronous power FET.

SGATE1 (Pin 2/Pin 27): First Phase Synchronous Drive Signal. An external driver buffer is needed to drive the top synchronous power FET.

GND (Pin 4/Pin 28): Chip Ground.

SYNC (Pin 5/Pin 1): Synchronization Input. The pulse width can range from 10% to 70%. Note that the operating frequency is half of the sync frequency.

DELAY (Pin 6/Pin 2): When synchronous drivers are used, the programmable delay that delays BGATE turns on after SGATE turns off.

DCL (Pin 7/Pin 3): This pin programs the limit of the maximum duty cycle. When connected to VRSET, it operates at natural maximum duty cycle, approximately 90%.

SENSE1+ (Pin 8/Pin 4): First Phase Current Sense Amplifier Positive Input. An RC filter is required across the current sense resistor. Current limit threshold is set at 60mV.

SENSE1− (Pin 9/Pin 5): First Phase Current Sense Amplifier Negative Input. An RC filter is required across the current sense resistor.

SLOPE (Pin 10/Pin 6): A resistor from SLOPE to GND increases the internal current mode PWM slope compensation.

RSET (Pin 11/Pin 7): A resistor from RSET to GND sets the oscillator charging current and the operating frequency.

SENSE2− (Pin 12/Pin 8): Second Phase Current Sense Amplifier Negative Input. An RC filter is required across the current sense resistor.

SENSE2+ (Pin 13/Pin 10): Second Phase Current Sense Amplifier Positive Input. An RC filter is required across the current sense resistor. Current limit threshold is set at 60mV.

SS (Pin 14/Pin 11): Soft-Start. A capacitor on this pin sets the output ramp up rate. The typical time for SS to reach the programmed level is (C • 2.44V)/10μA.

VC (Pin 15/Pin 12): The output of the gm error amplifier and the control signal of the current loop of the current-mode PWM. Switching starts at 0.7V, and higher VC voltages corresponds to higher inductor current.

FB (Pin 16/Pin 13): Error Amplifier Inverting Input. A resistor divider to this pin sets the output voltage.

RUN (Pin 17/Pin 14): LT3782 goes into shutdown mode when VRUN is below 2.2V and goes to low bias current shutdown mode when VRUN is below 0.3V.

VEE2 (Pin 19/Pin 16): Gate Driver BGATE2 Ground. This pin should be connected to the ground side of the second current sense resistor.

BGATE2 (Pin 20/Pin 17): Second Phase MOSFET Driver.

GBIAS2 (Pin 21/Pin 18): Bias for Gate Driver BGATE2. Should be connected to GBIAS or an external power supply between 12V to 14V. A bypass low ESR capacitor of 2μF or larger is needed and should be connected directly to the pin to minimize parasitic impedance.

GBIAS1 (Pin 22/Pin 21): Bias for Gate Driver BGATE1. Should be connected to GBIAS2.

BGATE1 (Pin 23/Pin 22): First Phase MOSFET Driver.

VEE1 (Pin 24/Pin 23): Gate Driver BGATE1 Ground. This pin should be connected to the ground side of the second current sense resistor.

VCC (Pin 27/Pin 24): Chip Power Supply. Good supply bypassing is required.

GBIAS (Pin 28/Pin 25): Internal 11V regulator output for biasing internal circuitry. Should be connected to GBIAS1 and GBIAS2.

Exposed Pad (Pin 29/Pin 29): The exposed package pad is fused to internal ground and is for heat sinking. Solder the bottom metal plate onto expanded ground plane for optimum thermal performance.

NC (Pins 3, 18, 25, 26/Pins 9, 15, 19, 20): Not Connected. Can be connected to GND.
Operation

The LT3782 is a two phase constant frequency current mode boost controller. Switching frequency can be programmed up to 500kHz. During normal switching cycles, the two channels are controlled by internal flip-flops and are 180 degrees out-of-phase.

Referring to the Block Diagram, the LT3782's basic functions include a transconductance amplifier ($g_m$) to regulate the output voltage and to control the current mode PWM current loop. It also includes the necessary logic and flip-flop to control the PWM switching cycles, two high speed gate drivers to drive high power N-Channel MOSFETs, and 2-phase control signals to drive external gate drivers for optional synchronous operation.

In normal operation, each switching cycle starts with a switch turn-on. The inductor current of each channel is sampled through the current sense resistor and amplified then compared to the error amplifier output $V_C$ to turn the switch off. The phase delay of the second channel is controlled by the divide-by-two D flip-flop and is exactly 180 degrees out-of-phase of the first channel. With a resistor divider connected to the FB pin, the output voltage is programmed to the desired value. The 10V gate drivers are sufficient to drive most high power N-channel MOSFETs in many industrial applications.

Additional important features include shutdown, current limit, soft-start, synchronization and programmable maximum duty cycle. Additional slope compensation can be added also.

Output Voltage Programming

With a 2.44V feedback reference voltage $V_{REF}$ the output $V_{OUT}$ is programmed by a resistor divider as shown in the Block Diagram.

$$V_{OUT} = 2.44 \left(1 + \frac{R_{F1}}{R_{F2}}\right)$$

Soft-Start and Shutdown

During soft-start, the voltage on the SS pin ($V_{SS}$) controls the output voltage. The output voltage thus ramps up following $V_{SS}$. The effective range of $V_{SS}$ is from 0V to 2.44V. The typical time for the output to reach the programmed level is

$$t = \frac{C \cdot 2.44V}{10\mu A}$$

C is the capacitor connected from the SS pin to Gnd.

Undervoltage Lockout and Shutdown

Only when $V_{RUN}$ is higher than 2.45V $V_{GBIAS}$ will be active and the switching enabled. The LT3782 goes into low current shutdown when $V_{RUN}$ is below 0.3V. A resistor divider can be used on RUN pin to set the desired $V_{CC}$ undervoltage lockout voltage. 80mV of hysteresis is built in on RUN pin thresholds.

Oscillation Frequency Setting and Synchronization

The switching frequency of LT3782 can be set up to 500kHz by a resistor $R_{FREQ}$ from pin $R_{SET}$ to ground.

For $f_{SET} = 250kHz$, $R_{FREQ} = 80k$

Once the switching frequency $f_{SET}$ is chosen, $R_{FREQ}$ can be found from the Switching Frequency vs $R_{FREQ}$ graph found under the Typical Performance Characteristics section.

Note that because of the 2-phase operation, the internal oscillator is running at twice the switching frequency. To synchronize the LT3782 to the system frequency $f_{SYSTEM}$, the synchronizing frequency $f_{SYNC}$ should be two times $f_{SYSTEM}$, and the LT3782 switching frequency $f_{SET}$ should be set below 80% of $f_{SYSTEM}$.

$$f_{SYNC} = 2f_{SYSTEM} \text{ and } f_{SET} < (f_{SYSTEM} \cdot 0.8)$$

For example, to synchronize the LT3782 to 200kHz system frequency $f_{SYSTEM}$, $f_{SYNC}$ needs to be set at 400kHz and $f_{SET}$ needs to be set at 160kHz. From the Switching Frequency vs $R_{FREQ}$ graph found under the Typical Performance Characteristics section, $R_{FREQ} = 130k$. 
APPLICATIONS INFORMATION

With a 200ns one-shot timer on chip, the LT3782 provides flexibility on the external sync pulse width. The sync pulse threshold is about 1.2V (Figure 1).

Current Limit

Current limit is set by the 60mV threshold across SEN1P, SEN1N for channel one and SEN2P, SEN2N for channel two. By connecting an external resistor $R_S$ (see Block Diagram), the current limit is set for $60\text{mV}/R_S$. $R_S$ should be placed very close to the power switch with very short traces. A low pass $R_C$ filter is needed across $R_S$ to filter out the switching spikes. Good Kelvin sensing is required for accurate current limit. The input bypass capacitor ground should be at the same ground point of the current sense resistor to minimize the ground current path.

Synchronous Rectifier Switches

For high output voltage applications, the power loss of the catch diodes are relatively small because of high duty cycle. If diodes power loss or heat is a concern, the LT3782 provides PWM signals through SGATE1 and SGATE2 pins to drive external MOSFET drivers for synchronous rectifier operation. Note that SGATE drives the top switch and BGATE drives the bottom switch. To avoid cross conduction between top and bottom switches, the BGATE turn-on is delayed 100ns (when DELAY pin is tied to $R_{SET}$ pin) from SGATE turn-off (see Figure 2). If a longer delay is needed to compensate for the propagation delay of external gate driver, a resistor divider can be used from $R_{SET}$ to ground to program $V_{DELAY}$ for the longer delay needed. For example, for a switching frequency of 250kHz and delay of 150ns,
then $R_{FREQ1} + R_{FREQ2}$ should be 80k and $V_{DELAY}$ should be 1V, with $V_{RSET} = 2.3V$ then $R_{FREQ1} = 47.5k$ and $R_{FREQ2} = 32.5k$ (see Figure 3).

**Duty Cycle Limit**

When DCL pin is shorted to $R_{SET}$ pin and switching frequency is less than 250kHz ($R_{FREQ} > 80k$), the maximum duty cycle of LT3782 will be at least 90%. The maximum duty cycle can be clamped to 50% by grounding the DCL pin or to 75% by forcing the $V_{DCL}$ voltage to 1.2V with a resistor divider from $R_{SET}$ pin to ground. The typical DCL pin input current is 0.2μA.

**Slope Compensation**

The LT3782 is designed for high voltage and/or high current applications, and very often these applications generate noise spikes that can be picked up by the current sensing amplifier and cause switching jitter. To avoid switching jitter, careful layout is absolutely necessary to minimize the current sensing noise pickup. Sometimes increasing slope compensation to overcome the noise can help to reduce jitter. The built-in slope compensation can be increased by adding a resistor $R_{SLOPE}$ from SLOPE pin to ground. Note that smaller $R_{SLOPE}$ increases slope compensation and the minimum $R_{SLOPE}$ allowed is $R_{FREQ}/2$.

**Layout Considerations**

To prevent EMI, the power MOSFETs and input bypass capacitor leads should be kept as short as possible. A ground plane should be used under the switching circuitry to prevent interplane coupling and to act as a thermal spreading path. Note that the bottom pad of the package is the heat sink, as well as the IC signal ground, and must be soldered to the ground plane.

In a boost converter, the conversion gain (assuming 100% efficiency) is calculated as (ignoring the forward voltage drop of the boost diode):

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{1-D}$$

where $D$ is the duty ratio of the main switch. $D$ can then be estimated from the input and output voltages:

$$D = 1 - \frac{V_{IN}}{V_{OUT}}; D_{MAX} = 1 - \frac{V_{IN(MAX)}}{V_{OUT}}$$

![Figure 3. Increase Delay Time](image-url)
The Peak and Average Input Currents

The control circuit in the LT3782 measures the input current by using a sense resistor in each MOSFET source, so the output current needs to be reflected back to the input in order to dimension the power MOSFET properly. Based on the fact that, ideally, the output power is equal to the input power, the maximum average input current is:

$$I_{IN\,(MAX)} = \frac{I_{O\,(MAX)}}{1-D_{MAX}}.$$  

The peak current is:

$$I_{IN\,(PEAK)} = 1.2 \cdot \frac{I_{O\,(MAX)}}{1-D_{MAX}}.$$  

The maximum duty cycle, $D_{MAX}$, should be calculated at minimum $V_{IN}$.

Power Inductor Selection

In a boost circuit, a power inductor should be designed to carry the maximum input DC current. The inductance should be small enough to generate enough ripple current to provide adequate signal to noise ratio to the LT3782. An empirical starting of the inductor ripple current (per phase) is about 40% of maximum DC current, which is half of the input DC current in a 2-phase circuit:

$$\Delta I_L \approx 40\% \cdot \frac{I_{OUT\,(MAX)} \cdot V_{OUT}}{2V_{IN}} = 20\% \cdot \frac{I_{OUT\,(MAX)} \cdot V_{OUT}}{V_{IN}}.$$  

where $V_{IN}$, $V_{OUT}$ and $I_{OUT}$ are the DC input voltage, output voltage and output current, respectively.

And the inductance is estimated to be:

$$L = \frac{V_{IN} \cdot D}{f_s \cdot \Delta I_L}$$  

where $f_s$ is the switching frequency per phase.

The saturation current level of inductor is estimated to be:

$$I_{SAT} \geq \frac{\Delta I_L}{2} + \frac{I_{IN}}{2} = 70\% \cdot \frac{I_{OUT\,(MAX)} \cdot V_{OUT}}{V_{IN\,(MIN)}}.$$  

Sense Resistor Selection

During the switch on-time, the control circuit limits the maximum voltage drop across the sense resistor to about 60mV. The peak inductor current is therefore limited to 60mV/R. The relationship between the maximum load current, duty cycle and the sense resistor $R_{SENSE}$ is:

$$R \leq \frac{V_{SENSE\,(MAX)} \cdot (1-D_{MAX})}{1.2 \cdot \frac{I_{O\,(MAX)}}{2}}.$$  

Power MOSFET Selection

Important parameters for the power MOSFET include the drain-to-source breakdown voltage ($V_{BVDSS}$), the threshold voltage ($V_{GS\,(TH)}$), the on-resistance ($R_{DS\,(ON)}$) versus gate-to-source voltage, the gate-to-source and gate-to-drain charges ($Q_{GS}$ and $Q_{GD}$, respectively), the maximum drain current ($I_{D\,(MAX)}$) and the MOSFET's thermal resistances ($R_{TH\,(JC)}$ and $R_{TH\,(JA)}$).
The gate drive voltage is set by the 10V GBIAS regulator. Consequently, 10V rated MOSFETs are required in most high voltage LT3782 applications.

Pay close attention to the BV_{DSS} specifications for the MOSFETs relative to the maximum actual switch voltage in the application. The switch node can ring during the turn-off of the MOSFET due to layout parasitics. Check the switching waveforms of the MOSFET directly across the drain and source terminals using the actual PC board layout (not just on a lab breadboard!) for excessive ringing.

Calculating Power MOSFET Switching and Conduction Losses and Junction Temperatures

In order to calculate the junction temperature of the power MOSFET, the power dissipated by the device must be known. This power dissipation is a function of the duty cycle, the load current and the junction temperature itself (due to the positive temperature coefficient of its R_{DS(ON)}). As a result, some iterative calculation is normally required to determine a reasonably accurate value. Care should be taken to ensure that the converter is capable of delivering the required load current over all operating conditions (line voltage and temperature), and for the worst-case specifications for V_{SENSE(MAX)} and the R_{DS(ON)} of the MOSFET listed in the manufacturer’s data sheet.

The power dissipated by the MOSFET in a 2-phase boost converter is:

\[ P_{\text{FET}} = \frac{1}{2} \frac{I_{\text{O(MAX)}}^2}{(1-D)} \cdot R_{\text{DS(ON)}} \cdot D \cdot \rho_T + k \cdot V_0^2 \cdot \frac{1}{(1-D)} \cdot C_{\text{RSS}} \cdot f \]

The first term in the equation above represents the I^2R losses in the device, and the second term, the switching losses. The constant, k = 1.7, is an empirical factor inversely related to the gate drive current and has the dimension of 1/current. The \( \rho_T \) term accounts for the temperature coefficient of the R_{DS(ON)} of the MOSFET, which is typically 0.4%/°C. Figure 4 illustrates the variation of normalized R_{DS(ON)} over temperature for a typical power MOSFET.

![Figure 4. Normalized R_{DS(ON)} vs Temperature](image)
APPLICATIONS INFORMATION

From a known power dissipated in the power MOSFET, its junction temperature can be obtained using the following formula:

\[ T_J = T_A + P_{FET} \times R_{TH(JA)} \]

The \( R_{TH(JA)} \) to be used in this equation normally includes the \( R_{TH(JC)} \) for the device plus the thermal resistance from the case to the ambient temperature \( (R_{TH(CA)}) \). This value of \( T_J \) can then be compared to the original, assumed value used in the iterative calculation process.

Input Capacitor Choice

The input capacitor must have high enough voltage and ripple current ratings to handle the maximum input voltage and RMS ripple current rating. The input ripple current in a boost circuit is very small because the input current is continuous. With 2-phase operation, the ripple cancellation will further reduce the input capacitor ripple current rating. The ripple current is plotted in Figure 5. Please note that the ripple current is normalized against

\[ I_{\text{norm}} = \frac{V_{IN}}{L \cdot f_s} \]

Output Capacitor Selection

The voltage rating of the output capacitor must be greater than the maximum output voltage with sufficient derating. Because the ripple current in output capacitor is a pulsating square wave in a boost circuit, it is important that the ripple current rating of the output capacitor be high enough to deal with this large ripple current. Figure 6 shows the output ripple current in the 1- and 2-phase designs. As we can see, the output ripple current of a 2-phase boost circuit reaches almost zero when the duty cycle equals 50% or the output voltage is twice as much as the input voltage. Thus the 2-phase technique significantly reduces the output capacitor size.

Figure 5. Normalized Input Peak-to-Peak Ripple Current

Figure 6. Normalized Output RMS Ripple Currents in Boost Converter: 1-Phase and 2-Phase. \( I_{\text{OUT}} \) is the DC Output Current.
APPLICATIONS INFORMATION

For a given $V_{IN}$ and $V_{OUT}$, we can calculate the duty cycle $D$ and then derive the output RMS ripple current from Figure 6. After choosing output capacitors with sufficient RMS ripple current rating, we also need to consider the ESR requirement if electrolytic caps, tantalum caps, POSCAPs or SP CAPs are selected. Given the required output ripple voltage spec $\Delta V_{OUT}$ (in RMS value) and the calculated RMS ripple current $\Delta I_{OUT}$, one can estimate the ESR value of the output capacitor to be

$$ESR \leq \frac{\Delta V_{OUT}}{\Delta I_{OUT}}.$$

External Regulator to Bias Gate Drivers

For applications with $V_{IN}$ higher than 24V, the IC temperature may get too high. To reduce heat, an external regulator between 12V to 14V should be used to override the internal $V_{GBIAS}$ regulator to supply the current needed for BGATE1 and BGATE2 (see Figure 7).

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power (≥100%). Percent efficiency can be expressed as:

$$\text{% Efficiency} = 100% - (L1 + L2 + L3 + \ldots),$$

where $L1$, $L2$, etc. are the individual loss components as a percentage of the input power. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Although all dissipative elements in the circuit produce losses, four main sources usually account for the majority of the losses in LT3782 application circuits:

1. The supply current into $V_{IN}$. The $V_{IN}$ current is the sum of the DC supply current $I_Q$ (given in the Electrical Characteristics) and the MOSFET driver and control currents. The DC supply current into the $V_{IN}$ pin is typically about 7mA and represents a small power loss (much less than 1%) that increases with $V_{IN}$. The driver current results from switching the gate capacitance of the power MOSFET; this current is typically much larger than the DC current. Each time the MOSFET is switched on and then off, a packet of gate charge $Q_G$ is transferred from GBIAS to ground. The resulting $\frac{dQ}{dt}$ is a current that must be supplied to the GBIAS capacitor through the $V_{IN}$ pin by an external supply. In normal operation:

$$I_{Q(TOT)} \approx I_Q = f \cdot Q_G$$

$$P_{IC} = V_{IN} \cdot (I_Q + f \cdot Q_G)$$

Figure 7
2. Power MOSFET switching and conduction losses:

\[
P_{\text{FET}} = \left( \frac{I_{O(\text{MAX})}}{2-1-D_{\text{MAX}}} \right)^2 \cdot R_{DS(\text{ON})} \cdot D_{\text{MAX}} \cdot P_T
\]

\[
+ k \cdot V_o^2 \cdot \frac{2}{1-D_{\text{MAX}}} \cdot C_{\text{RSS}} \cdot f
\]

3. The \(i^2R\) losses in the sense resistor can be calculated almost by inspection.

\[
P_{R(\text{SENSE})} = \left( \frac{I_{O(\text{MAX})}}{2-1-D_{\text{MAX}}} \right)^2 \cdot R \cdot D_{\text{MAX}}
\]

4. The losses in the inductor are simply the DC input current squared times the winding resistance. Expressing this loss as a function of the output current yields:

\[
P_{R(\text{WINDING})} = \left( \frac{I_{O(\text{MAX})}}{2-1-D_{\text{MAX}}} \right)^2 \cdot R_W
\]

5. Losses in the boost diode. The power dissipation in the boost diode is:

\[
P_{\text{DIODE}} = \frac{I_{O(\text{MAX})}}{2} \cdot V_D
\]

The boost diode can be a major source of power loss in a boost converter. For 13.2V input, 42V output at 3A, a Schottky diode with a 0.4V forward voltage would dissipate 600mW, which represents about 1% of the input power. Diode losses can become significant at low output voltages where the forward voltage is a significant percentage of the output voltage.

6. Other losses, including \(C_{\text{IN}}\) and \(C_{\text{O}}\) ESR dissipation and inductor core losses, generally account for less than 2% of the total losses.

**PCB Layout Considerations**

To achieve best performance from an LT3782 circuit, the PC board layout must be carefully done. For lower power applications, a two-layer PC board is sufficient. However, at higher power levels, a multiplayer PC board is recommended. Using a solid ground plane under the circuit is the easiest way to ensure that switching noise does not affect the operation.

In order to help dissipate the power from MOSFETs and diodes, keep the ground plane on the layers closest to the layers where power components are mounted. Use power planes for MOSFETs and diodes in order to improve the spreading of the heat from these components into the PCB.
For best electrical performance, the LT3782 circuit should be laid out as follows:

Place all power components in a tight area. This will minimize the size of high current loops. Orient the input and output capacitors and current sense resistors in a way that minimizes the distance between the pads connected to ground plane.

Place the LT3782 and associated components tightly together and next to the section with power components.

Use a local via to ground plane for all pads that connect to ground. Use multiple vias for power components.

Connect the current sense inputs of LT3782 directly to the current sense resistor pads. Connect the current sense traces on the opposite sides of pads from the traces carrying the MOSFETs source currents to ground. This technique is referred to as Kelvin sensing.
10V to 24V Input to 24V, 8A Output Boost Converter

Efficiency

10V TO 24V INPUT

OUTPUT 24V 8A

LT3782

TYPICAL APPLICATIONS
FE Package
28-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663)
Exposed Pad Variation EB

NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN MILLIMETERS (INCHES)
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE
   FOR EXPOSED PAD ATTACHMENT
   *DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH
   SHALL NOT EXCEED 0.150mm (.006") PER SIDE
UFD Package
28-Lead Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1712 Rev B)

NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WXXX-X).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED
TYPICAL APPLICATIONS

28V Output Base Station Power Converter with Redundant Input

RELATED PARTS

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
<th>COMMENTS</th>
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<tbody>
<tr>
<td>LT®1619</td>
<td>Current Mode PWM Controller</td>
<td>300kHz Fixed Frequency, Boost, SEPIC, Flyback Topology</td>
</tr>
<tr>
<td>LTC1624</td>
<td>Current Mode DC/DC Controller</td>
<td>SO-8; 300kHz Operating Frequency; Buck, Boost, SEPIC Design; VIN Up to 36V</td>
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<tr>
<td>LTC1696</td>
<td>Overvoltage Protection Controller</td>
<td>0.8V ≤ VIN ≤ 24V, ±2% Overvoltage Threshold Accuracy, ThinSOT™ Package</td>
</tr>
<tr>
<td>LTC1700</td>
<td>No RSENSE™ Synchronous Step-Up Controller</td>
<td>Up to 95% Efficiency, Operation as Low as 0.9V Input</td>
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<tr>
<td>LTC1871/LTC1871-7</td>
<td>Wide Input Range Controller</td>
<td>No RSENSE; 7V Gate Drive, Current Mode Control</td>
</tr>
<tr>
<td>LT1930</td>
<td>1.2MHz, SOT-23 Boost Converter</td>
<td>Up to 34V Output, 2.6V ≤ VIN ≤ 16V, Miniature Design</td>
</tr>
<tr>
<td>LT1952</td>
<td>Single Switch Synchronous Forward Controller</td>
<td>High Efficiency, 25W to 500W, Wide Input Range, Adaptive Duty Cycle Clamp</td>
</tr>
<tr>
<td>LTC3425</td>
<td>5A, 8MHz 4-Phase Monolithic Step-Up DC/DC Converter</td>
<td>0.5V ≤ VIN ≤ 4.5V, 2.4V ≤ VOUT ≤ 5.25V, Very Low Output Ripple</td>
</tr>
<tr>
<td>LTC3703/LTC3703-5</td>
<td>100V and 60V, Step-Down and Step-Up DC/DC Synchronous Controller</td>
<td>High Efficiency Synchronous Operation, High Voltage Operation, No Transformer Required</td>
</tr>
<tr>
<td>LTC3728</td>
<td>Dual, 550kHz, 2-Phase Synchronous Step-Down Controller</td>
<td>Dual 180° Phased Controllers, VIN: 3.5V to 35V, 99% Duty Cycle, 5mm × 5mm QFN, SSOP-28 Packages</td>
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<tr>
<td>LTC3729</td>
<td>20A to 200A, 550kHz PolyPhase™ Synchronous Controller</td>
<td>Expandable from 2-Phase to 12-Phase, Uses All Surface Mount Components, VIN Up to 36V</td>
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<tr>
<td>LTC3731</td>
<td>3- to 12-Phase Step-Down Synchronous Controller</td>
<td>60A to 240A Output Current, 0.6V ≤ VOUT ≤ 6V, 4.5V ≤ VIN ≤ 32V</td>
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<tr>
<td>LTC3803</td>
<td>SOT-23 Flyback Controller</td>
<td>Adjustable Slope Compensation, Internal Soft-Start, Current Mode 200kHz Operation</td>
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<tr>
<td>LTC3806</td>
<td>Synchronous Flyback Controller</td>
<td>High Efficiency, Improves Cross Regulation in Multiple Output Designs, Current Mode, 3mm × 4mm 12-Pin DFN Package</td>
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