FEATURES
- Very Low $V_{IN\text{(MIN)}}$: 1.5V
- Ultrafast Transient Response
- True Current Mode Control
- 5V Drive for N-Channel MOSFETs Eliminates Auxiliary 5V Supply
- No Sense Resistor Required
- Uses Standard 5V Logic-Level N-Channel MOSFETs
- $V_{OUT\text{(MIN)}}$: 0.4V
- $V_{OUT}$ Tracks 1/2 $V_{IN}$ or External $V_{REF}$
- Symmetrical Source and Sink Output Current Limit
- Adjustable Switching Frequency
- $t_{ON\text{(MIN)}}$ <100ns
- Power Good Output Voltage Monitor
- Programmable Soft-Start
- Output Overvoltage Protection
- Optional Short-Circuit Shutdown Timer
- Small 24-Lead SSOP Package

APPLICATIONS
- Bus Termination: DDR/QDR Memory, SSTL, HSTL, ...
- Servers, RAID Systems
- Distributed Power Systems
- Synchronous Buck with General Purpose Boost

DESCRIPTION
The LTC3718 is a high current, high efficiency synchronous switching regulator controller for DDR and QDR™ memory termination. It operates from an input as low as 1.5V and provides a regulated output voltage equal to (0.5)$V_{IN}$. The controller uses a valley current control architecture to enable high frequency operation with very low on-times without requiring a sense resistor. Operating frequency is selected by an external resistor and is compensated for variations in $V_{IN}$ and $V_{OUT}$. The LTC3718 uses a pair of standard 5V logic level N-channel external MOSFETs, eliminating the need for expensive P-channel or low threshold devices.

Forced continuous operation reduces noise and RF interference. Fault protection is provided by internal foldback current limiting, an output overvoltage comparator and an optional short-circuit timer. Soft-start capability for supply sequencing can be accomplished using an external timing capacitor. OPTI-LOOP® compensation allows the transient response to be optimized over a wide range of loads and output capacitors.

Efficiency vs Load Current

Figure 1. High Efficiency Bus Termination Supply without Auxiliary 5V Supply
**LTC3718**

**ABSOLUTE MAXIMUM RATINGS**
(Note 1)

- Input Supply Voltage (Vin2) .................................. 10V to –0.3V
- Boosted Topside Driver Supply Voltage (BOOST) .................. 42V to –0.3V
- VIN1, ION, SW1 Voltage ........................................ 36V to –0.3V
- RUN/SS, PGOOD Voltages ........................................ 7V to –0.3V
- VON, VREF, VRNG Voltages ...................................... 2.7V to –0.3V
- SW2 Voltage ........................................................ 36V to –0.4V
- VFB2 Voltage ..................................................... VIN2 + 0.3V
- SHDN Voltage ....................................................... 10V
- TG, BG, INTVCC Peak Currents ................................. 2A
- TG, BG, INTVCC RMS Currents .................................. 50mA

Operating Ambient Temperature Range (Note 4) ................... –40 °C to 85 °C

Junction Temperature (Note 2) ................................... 125 °C

Storage Temperature Range ........................................ –65 °C to 150 °C

Lead Temperature (Soldering, 10 sec) ............................... 300 °C

*Consult LTC Marketing for parts specified with wider operating temperature ranges.*

**PACKAGE/ORDER INFORMATION**

<table>
<thead>
<tr>
<th>ORDER PART NUMBER</th>
</tr>
</thead>
<tbody>
<tr>
<td>LTC3718EG</td>
</tr>
</tbody>
</table>

**ELECTRICAL CHARACTERISTICS**

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are TA = 25 °C. VIN1 = 15V, VIN2 = 1.5V unless otherwise noted.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
</table>

**Buck Regulator**

- I_Q(VIN1) Input DC Supply Current (VIN1)
  - Normal
  - Shutdown Supply Current
  - V_RUN/SS = 0V

- V_FB1 Feedback Voltage Accuracy
  - I_TH = 1.2V (Note 3)
  - ● –0.65, 0.1, 0.65 %

- ΔV_FB1(Line) Feedback Voltage Line Regulation
  - VIN1 = 4V to 36V, I_TH = 1.2V (Note 3)
  - –0.002 %/V

- ΔV_FB1(LOAD) Feedback Voltage Load Regulation
  - I_TH = 0.5V to 1.9V (Note 3)
  - –0.05, –0.3 %

- g_m(EA) Error Amplifier Transconductance
  - I_TH = 1.2V (Note 3)
  - 0.93, 1.13, 1.33 mS

- I_ON On-Time
  - I_ON = 60μA, V_ON = 1.5V
  - –200, –250, –300 ns
  - I_ON = 30μA, V_ON = 1.5V
  - –400, –500, –600 ns

- I_ON(MIN) Minimum On-Time
  - I_ON = 180μA
  - 50 ns

- ΔV_FB1(UV) Output Undervoltage Fault Threshold
  - ● –25 %

- VRUN/SS(ON) RUN Pin Start Threshold
  - ● 0.8, 1.5, 2 V

- VRUN/SS(LE) RUN Pin Latchoff Enable
  - RUN/SS Pin Rising
  - 4, 4.5 V
### ELECTRICAL CHARACTERISTICS

The • denotes specifications which apply over the full operating temperature range, otherwise specifications are $T_A = 25°C$. $V_{IN1} = 15V$, $V_{IN2} = 1.5V$ unless otherwise noted.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{RUN/SS(LT)}$</td>
<td>RUN Pin Latchoff Threshold</td>
<td>RUN/SS Pin Falling</td>
<td>3.5</td>
<td>4.2</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{RUN/SS(C)}$</td>
<td>Soft-Start Charge Current</td>
<td>$V_{RUN/SS} = 0V$</td>
<td>$-0.5$</td>
<td>1.2</td>
<td>3</td>
<td>$\mu$A</td>
</tr>
<tr>
<td>$I_{RUN/SS(D)}$</td>
<td>Soft-Start Discharge Current</td>
<td>$V_{RUN/SS} = 4.5V$, $V_{FB} = 0V$</td>
<td>0.8</td>
<td>1.8</td>
<td>3</td>
<td>$\mu$A</td>
</tr>
<tr>
<td>$V_{IN(UVLO)}$</td>
<td>VIN Undervoltage Lockout</td>
<td>$V_{IN}$ Falling</td>
<td>$3.4$</td>
<td>3.9</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{IN}$ Rising</td>
<td>$3.5$</td>
<td>4.0</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$R_{UP}$</td>
<td>TG Driver Pull-Up On Resistance</td>
<td>TG High</td>
<td>2</td>
<td>3</td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>$R_{DOWN}$</td>
<td>TG Driver Pull-Down On Resistance</td>
<td>TG Low</td>
<td>2</td>
<td>3</td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>$R_{UP}$</td>
<td>BG Driver Pull-Up On Resistance</td>
<td>BG High</td>
<td>3</td>
<td>4</td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>$R_{DOWN}$</td>
<td>BG Driver Pull-Down On Resistance</td>
<td>BG Low</td>
<td>1</td>
<td>2</td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>$r_T$</td>
<td>TG Rise Time</td>
<td>$C_{LOAD} = 3300pF$</td>
<td>20</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$r_T$</td>
<td>TG Fall Time</td>
<td>$C_{LOAD} = 3300pF$</td>
<td>20</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$i_T$</td>
<td>BG Rise Time</td>
<td>$C_{LOAD} = 3300pF$</td>
<td>20</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$i_T$</td>
<td>BG Fall Time</td>
<td>$C_{LOAD} = 3300pF$</td>
<td>20</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$V_{INTVCC}$</td>
<td>Internal VCC Voltage</td>
<td>$6V &lt; V_{IN1} &lt; 30V$</td>
<td>4.7</td>
<td>5</td>
<td>5.3</td>
<td>V</td>
</tr>
<tr>
<td>$\Delta V_{DDO(LOAD)}$</td>
<td>Internal VCC Load Regulation</td>
<td>$I_{CC} = 0mA$ to $20mA$</td>
<td>$-0.1$</td>
<td>±2</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>$\Delta V_{FB1H}$</td>
<td>PGOOD Upper Threshold</td>
<td>$V_{FB1} = $ Rising</td>
<td>8</td>
<td>10</td>
<td>12</td>
<td>%</td>
</tr>
<tr>
<td>$\Delta V_{FB1L}$</td>
<td>PGOOD Lower Threshold</td>
<td>$V_{FB1} = $ Falling</td>
<td>$-8$</td>
<td>$-10$</td>
<td>$-12$</td>
<td>%</td>
</tr>
<tr>
<td>$\Delta V_{FB1(HYS)}$</td>
<td>PGOOD Hysterisis</td>
<td>$V_{FB1} = $ Returning</td>
<td>1</td>
<td>2</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>$V_{PGL}$</td>
<td>PGOOD Low Voltage</td>
<td>$I_{PGOOD} = 5mA$</td>
<td>0.15</td>
<td>0.4</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

### Internal VCC Regulator

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{FB2}$</td>
<td>Feedback Voltage</td>
<td>$0°C &lt; T &lt; 70°C$</td>
<td>1.205</td>
<td>1.23</td>
<td>1.255</td>
</tr>
<tr>
<td>$I_{FB2}$</td>
<td>Pin Bias Current</td>
<td>$0°C &lt; T &lt; 70°C$</td>
<td>1.20</td>
<td>1.23</td>
<td>1.26</td>
</tr>
<tr>
<td>$\Delta V_{FB2(LINE)}$</td>
<td>Boost Reference Line Regulation</td>
<td>$1.5V &lt; V_{IN2} &lt; 10V$</td>
<td>0.02</td>
<td>0.2</td>
<td>%/V</td>
</tr>
<tr>
<td>$f_{BOOST}$</td>
<td>Switching Frequency</td>
<td>$0°C &lt; T &lt; 70°C$</td>
<td>1.0</td>
<td>1.4</td>
<td>1.8</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0.9</td>
<td>1.4</td>
<td>1.9</td>
</tr>
<tr>
<td>$DC_{BOOST(MAX)}$</td>
<td>Maximum Duty Cycle</td>
<td>82</td>
<td>86</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>$I_{LIM(BOOST)}$</td>
<td>Switch Current Limit</td>
<td>(Note 5)</td>
<td>500</td>
<td>800</td>
<td>mA</td>
</tr>
<tr>
<td>$V_{CESAT(BOOST)}$</td>
<td>Switch $V_{CESAT}$</td>
<td>$I_{SW} = 300mA$</td>
<td>300</td>
<td>350</td>
<td>mV</td>
</tr>
<tr>
<td>$I_{SWLKG(BOOST)}$</td>
<td>Switch Leakage Current</td>
<td>$V_{SW} = 5V$</td>
<td>0.01</td>
<td>1</td>
<td>µA</td>
</tr>
<tr>
<td>$V_{SHDN(HIGH)}$</td>
<td>SHDN Input Voltage High</td>
<td>1</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{SHDN(LOW)}$</td>
<td>SHDN Input Voltage Low</td>
<td>0.3</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{SHDN}$</td>
<td>SHDN Pin Bias Current</td>
<td>$V_{SHDN} = 3V$</td>
<td>25</td>
<td>50</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{SHDN} = 0V$</td>
<td>0.01</td>
<td>0.1</td>
<td>µA</td>
</tr>
</tbody>
</table>
**ELECTRICAL CHARACTERISTICS**

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

**Note 2:** $T_J$ is calculated from the ambient temperature $T_A$ and power dissipation $P_D$ as follows:

$LTC3718EG$: $T_J = T_A + (P_D \cdot 130 \degree C/W)$

**Note 3:** The LTC3718 is tested in a feedback loop that adjusts $V_{FB1}$ to achieve a specified error amplifier output voltage ($V_{TH}$).

**Note 4:** The LTC3718 is guaranteed to meet performance specifications from $0 \degree C$ to $70 \degree C$. Specifications over the $-40 \degree C$ to $85 \degree C$ operating temperature range are assured by design, characterization and correlation with statistical process controls.

**Note 5:** Current limit guaranteed by design and/or correlation to static test.

**TYPICAL PERFORMANCE CHARACTERISTICS**

**Boost Converter Oscillator Frequency vs Temperature**

**SHDN Pin Current vs $V_{SHDN}$**

**Boost Converter Current Limit vs Duty Cycle**

**$V_{FB2}$, Feedback Pin Voltage**

**Efficiency vs Load Current**

**$V_{OUT}/V_{IN}$ Tracking Ratio vs Input Voltage**
TYPICAL PERFORMANCE CHARACTERISTICS

Frequency vs Input Voltage

Load Regulation

Load-Step Transient

Start-Up Response

On-Time vs \( V_{ON} \) Voltage

On-Time vs Temperature

On-Time vs \( I_{ON} \) Current
TYPICAL PERFORMANCE CHARACTERISTICS

**INTVCC Load Regulation**

**RUN/SS Latchoff Thresholds vs Temperature**

**RUN/SS Latchoff Thresholds vs Temperature**

**Undervoltage Lockout Threshold vs Temperature**

**Maximum Current Sense Threshold vs VRNG Voltage**

**Maximum Current Sense Threshold vs RUN/SS Voltage, VRNG = 1V**

**Maximum Current Sense Threshold vs Temperature, VRNG = 1V**

**Error Amplifier gm vs Temperature**
**PIN FUNCTIONS**

**RUN/SS (Pin 1):** Run Control and Soft-Start Input. A capacitor to ground at this pin sets the ramp time to full output current (approximately 3s/μF) and the time delay for overcurrent latchoff (see Applications Information). Forcing this pin below 0.8V shuts down the device.

**V_{ON} (Pin 2):** On-Time Voltage Input. Voltage trip point for the on-time comparator. Tying this pin to the output voltage makes the on-time proportional to V_{OUT}. The comparator input defaults to 0.7V when the pin is grounded, 2.4V when the pin is tied to INTVCC.

**PGOOD (Pin 3):** Power Good Output. Open-drain logic output that is pulled to ground when the output voltage of the buck section is not within ±10% of the regulation point.

**V_{RNG} (Pin 4):** Sense Voltage Range Input. The voltage at this pin is ten times the nominal sense voltage at maximum output current and can be set from 0.5V to 2V by a resistive divider from INTVCC. The nominal sense voltage defaults to 70mV when this pin is tied to ground, 140mV when tied to INTVCC.

**ITH (Pin 5):** Current Control Threshold and Error Amplifier Compensation Point. The current comparator threshold increases with this control voltage. The voltage ranges from 0V to 2.4V with 1.2V corresponding to zero sense voltage (zero current).

**SGND (Pins 6, 11):** Signal Ground. All small-signal components and compensation components should connect to this ground, which in turn connects to PGND at one point.

**ION (Pin 7):** On-Time Current Input. Tie a resistor from VIN to this pin to set the one-shot timer current and thereby set the switching frequency.

**V_{FB1} (Pin 8):** Error Amplifier Feedback Input. This pin connects the negative error amplifier input to V_{OUT}.

**V_{REF} (Pin 9):** Positive Input of Internal Error Amplifier. Reference voltage for output voltage, power good threshold, and short-circuit shutdown threshold. The output voltage is set to V_{REF}/2.

**SHDN (Pin 10):** Shutdown, Active Low. Tie to 1V or more to enable boost converter portion of the LTC3718. Ground to shut down.

**V_{FB2} (Pin 12):** Boost Converter Feedback. The V_{FB2} pin is connected to INTVCC through a resistor divider to set the voltage on INTVCC. Set INTVCC voltage according to:

\[ V_{INTVCC} = 1.23V(1 + RF2/RF1) \]

**SW2 (Pin 13):** Boost Converter Switch Pin. Connect inductor/diode for boost converter portion here. Minimize trace area at this pin to keep EMI down.

**PGND (Pins 14, 19):** Power Ground. Connect these pins closely to the source of the bottom N-channel MOSFET, the (–) terminal of C_{VC} and the (–) terminal of C_{IN}.

**V_{IN2} (Pin 15):** Input Supply Pin for Boost Converter Portion of LTC3718. Must be locally bypassed.

**V_{IN1} (Pin 16):** Main Input Supply. Decouple this pin to PGND with at least a 1μF ceramic capacitor.

**INTVCC (Pin 17):** Internal Regulator Output. The driver and control circuits are powered from this voltage when VIN is greater than 5V. Decouple this pin to power ground with a minimum of 4.7μF low ESR tantalum or ceramic capacitor.

**BG (Pin 18):** Bottom Gate Drive. Drives the gate of the bottom N-channel MOSFET between ground and INTVCC.

**SENSE^- (Pin 20):** Negative Current Sense Comparator Input. The (–) input to the current comparator is normally connected to power ground unless using a resistive divider from INTVCC (see Applications Information).

**SENSE^+ (Pin 21):** Positive Current Sense Comparator Input. The (+) input to the current comparator is normally connected to the SW node unless using a sense resistor (see Applications Information).

**SW1 (Pin 22):** Switch Node. The (–) terminal of the bootstrap capacitor C_B connects here. This pin swings from a diode voltage drop below ground up to V_{IN}.

**TG (Pin 23):** Top Gate Drive. Drives the top N-channel MOSFET with a voltage swing equal to INTVCC superimposed on the switch node voltage SW.

**BOOST (Pin 24):** Boosted Floating Driver Supply. The (+) terminal of the bootstrap capacitor C_B connects here. This pin swings from a diode voltage drop below INTVCC up to V_{IN} + INTVCC.
OPERATION

Main Control Loop

The LTC3718 is a current mode controller for DC/DC step-down converters designed to operate from low input voltages. It incorporates a boost converter with a buck regulator.

Buck Regulator Operation

In normal operation, the top MOSFET is turned on for a fixed interval determined by a one-shot timer OST. When the top MOSFET is turned off, the bottom MOSFET is turned on until the current comparator ICMP trips, restarting the one-shot timer and initiating the next cycle. Inductor current is determined by sensing the voltage between the SENSE+ and SENSE− pins using the bottom MOSFET on-resistance. The voltage on the ITH pin sets the comparator threshold corresponding to inductor valley current. The error amplifier EA adjusts this voltage by comparing the feedback signal VFB1 from the output voltage with an internal reference generated from one half of the voltage on VREF. If the load current increases, it causes a drop in the feedback voltage relative to the reference. The ITH voltage then rises until the average inductor current again matches the load current.

The operating frequency is determined implicitly by the top MOSFET on-time and the duty cycle required to maintain regulation. The one-shot timer generates an on-time that is proportional to the ideal duty cycle, thus holding frequency approximately constant with changes in VIN. The nominal frequency can be adjusted with an external resistor RON.

Overvoltage and undervoltage comparators OV and UV pull the PGOOD output low if the output feedback voltage exits a ±10% window around the regulation point. Furthermore, in an overvoltage condition, M1 is turned off and M2 is turned on and held on until the overvoltage condition clears.

Pulling the RUN/SS pin low forces the controller into its shutdown state, turning off both M1 and M2. Releasing the pin allows an internal 1.2μA current source to charge up an external soft-start capacitor CSS. When this voltage reaches 1.5V, the controller turns on and begins switching, but with the ITH voltage clamped at approximately 0.6V below the RUN/SS voltage. As CSS continues to charge, the soft-start current limit is removed.

INTVCC Power

Power for the top and bottom MOSFET drivers and most of the internal controller circuitry is derived from the INTVCC pin. The top MOSFET driver is powered from a floating bootstrap capacitor CB. This capacitor is recharged from INTVCC through an external Schottky diode DB when the top MOSFET is turned off.

Boost Regulator Operation

The 5V power source for INTVCC can be provided by a current mode, internally compensated fixed frequency step-up switching regulator that has been incorporated into the LTC3718.

Operation can be best understood by referring to the Functional Diagrams. Q1 and Q2 form a bandgap reference core whose loop is closed around the output of the regulator. The voltage drop across R5 and R6 is low enough such that Q1 and Q2 do not saturate, even when VIN2 is 1V. When there is no load, VFB2 rises slightly above 1.23V, causing VC (the error amplifier’s output) to decrease. Comparator A2’s output stays high, keeping switch Q3 in the off state. As increased output loading causes the VFB2 voltage to decrease, A1’s output increases. Switch current is regulated directly on a cycle-by-cycle basis by the VC node. The flip-flop is set at the beginning of each switch cycle, turning on the switch. When the summation of a signal representing switch current and a ramp generator (introduced to avoid subharmonic oscillations at duty factors greater than 50%) exceeds the VC signal, comparator A2 changes state, resetting the flip-flop and turning off the switch. More power is delivered to the output as switch current is increased. The output voltage, attenuated by external resistor divider R7 and R8, appears at the VFB2 pin, closing the overall loop. Frequency compensation is provided internally by RC and CC. Transient response can be optimized by the addition of a phase lead capacitor CPL in parallel with R7 in applications where large value or low ESR output capacitors are used.

As the load current is decreased, the switch turns on for a shorter period each cycle. If the load current is further decreased, the boost converter will skip cycles to maintain output voltage regulation. If the VFB2 pin voltage is increased significantly above 1.23V, the boost converter will enter a low power state.
A typical LTC3718 application circuit is shown in Figure 1. External component selection is primarily determined by the maximum load current and begins with the selection of the sense resistance and power MOSFET switches. The LTC3718 uses the on-resistance of the synchronous power MOSFET for determining the inductor current. The desired amount of ripple current and operating frequency largely determines the inductor value. Finally, $C_{IN}$ is selected for its ability to handle the large RMS current into the converter and $C_{OUT}$ is chosen with low enough ESR to meet the output voltage ripple and transient specification.

**Maximum Sense Voltage and VRNG Pin**

Inductor current is determined by measuring the voltage across a sense resistance that appears between the SENSE+ and SENSE– pins. The maximum sense voltage is set by the voltage applied to the VRNG pin and is equal to approximately $(0.13)V_{\text{VRNG}}$ for sourcing current and $(0.17)V_{\text{VRNG}}$ for sinking current. The current mode control loop will not allow the inductor current valleys to exceed $(0.13)V_{\text{VRNG}}/R_{\text{SENSE}}$ for sourcing current and $(0.17)V_{\text{VRNG}}$ for sinking current. In practice, one should allow some margin for variations in the LTC3718 and external component values and a good guide for selecting the sense resistance is:

$$R_{\text{SENSE}} = \frac{V_{\text{VRNG}}}{10 \times V_{\text{OUT(MAX)}}}$$

when $V_{\text{VRNG}} = 0.5 – 2V$.

An external resistive divider from INTVCC can be used to set the voltage of the VRNG pin between 0.5V and 2V resulting in nominal sense voltages of 50mV to 200mV. Additionally, the VRNG pin can be tied to SGND or INTVCC in which case the nominal sense voltage defaults to 70mV or 140mV, respectively. The maximum allowed sense voltage is about 1.3 times this nominal value for positive output current and 1.7 times the nominal value for negative output current.

**Connecting the SENSE+ and SENSE– Pins**

The LTC3718 can be used with or without a sense resistor. When using a sense resistor, it is placed between the source of the bottom MOSFET M2 and ground. Connect the SENSE+ and SENSE– pins as a Kelvin connection to the sense resistor with SENSE+ at the source of the bottom MOSFET and the SENSE– pin to PGND1. Using a sense resistor provides a well defined current limit, but adds cost and reduces efficiency. Alternatively, one can eliminate the sense resistor and use the bottom MOSFET as the current sense element by simply connecting the SENSE+ pin to the drain and the SENSE– pin to the source of the bottom MOSFET. This improves efficiency, but one must carefully choose the MOSFET on-resistance as discussed in a later section.

**Power MOSFET Selection**

The LTC3718 requires two external N-channel power MOSFETs, one for the top (main) switch and one for the bottom (synchronous) switch. Important parameters for the power MOSFETs are the breakdown voltage $V_{\text{BR}DSS}$, threshold voltage $V_{\text{GS}TH}$, on-resistance $R_{\text{DS(ON)}}$, reverse transfer capacitance $C_{RSS}$ and maximum current $I_{\text{DS(MAX)}}$. The gate drive voltage is set by the 5V INTVCC supply. Consequently, logic-level threshold MOSFETs must be used in LTC3718 applications.

When the bottom MOSFET is used as the current sense element, particular attention must be paid to its on-resistance. MOSFET on-resistance is typically specified with a maximum value $R_{\text{DS(ON)(MAX)}}$ at $25^\circ C$. In this case, additional margin is required to accommodate the rise in MOSFET on-resistance with temperature:

$$R_{\text{DS(ON)(MAX)}} = \frac{R_{\text{SENSE}}}{\rho T}$$

The $\rho T$ term is a normalization factor (unity at $25^\circ C$) accounting for the significant variation in on-resistance with temperature, typically about $0.4%/^\circ C$ as shown in Figure 2. For a maximum junction temperature of $100^\circ C$, using a value $\rho T = 1.3$ is reasonable.

The power dissipated by the top and bottom MOSFETs strongly depends upon their respective duty cycles and the load current. During normal operation, the duty cycles for the MOSFETs are:
Tying a resistor $R_{ON}$ from $V_{IN}$ to the $ION$ pin yields an on-time inversely proportional to $V_{IN}$. For a step-down converter, this results in approximately constant frequency operation as the input supply varies:

$$f = \frac{V_{OUT} \cdot R_{ON}(10pF)}{V_{IN} \cdot V_{ON}(10pF)} \text{ [Hz]}$$

To hold frequency constant during output voltage changes, tie the $V_{ON}$ pin to $V_{OUT}$. The $V_{ON}$ pin has internal clamps that limit its input to the one-shot timer. If the pin is tied below 0.7V, the input to the one-shot is clamped at 0.7V. Similarly, if the pin is tied above 2.4V, the input is clamped at 2.4V.

Because the voltage at the $ION$ pin is about 0.7V, the current into this pin is not exactly inversely proportional to $V_{IN}$, especially in applications with lower input voltages. To account for the 0.7V drop on the $ION$ pin, the following equation can be used to calculate frequency:

$$f = \frac{(V_{IN} - 0.7V) \cdot V_{OUT}}{V_{VON} \cdot V_{IN} \cdot R_{ON}(10pF)}$$

To correct for this error, an additional resistor $R_{ON2}$ connected from the $ION$ pin to the 5V INTVCC supply will further stabilize the frequency.

Changes in the load current magnitude will also cause frequency shift. Parasitic resistance in the MOSFET switches and inductor reduce the effective voltage across the inductance, resulting in increased duty cycle as the load current increases. By lengthening the on-time slightly as current increases, constant frequency operation can be maintained. This is accomplished with a resistive divider from the $I_{TH}$ pin to the $V_{ON}$ pin and $V_{OUT}$. The values required will depend on the parasitic resistances in the specific application. A good starting point is to feed about 25% of the voltage change at the $I_{TH}$ pin to the $V_{ON}$ pin as shown in Figure 3a. Place capacitance on the $V_{ON}$ pin to...
filter out the \( I_{TH} \) variations at the switching frequency. The resistor load on \( I_{TH} \) reduces the DC gain of the error amp and degrades load regulation, which can be avoided by using the PNP emitter follower of Figure 3b.

**Inductor L1 Selection**

Given the desired input and output voltages, the inductor value and operating frequency determine the ripple current:

\[
\Delta I_L = \left( \frac{V_{OUT}}{fL} \right) \left( 1 - \frac{V_{OUT}}{V_{IN}} \right)
\]

Lower ripple current reduces cores losses in the inductor, ESR losses in the output capacitors and output voltage ripple. Highest efficiency operation is obtained at low frequency with small ripple current. However, achieving this requires a large inductor. There is a tradeoff between component size, efficiency and operating frequency.

A reasonable starting point is to choose a ripple current that is about 40% of \( I_{OUT(MAX)} \). The largest ripple current occurs at the highest \( V_{IN} \). To guarantee that ripple current does not exceed a specified maximum, the inductance should be chosen according to:

\[
L = \left( \frac{V_{OUT}}{f\Delta I_{L(MAX)}} \right) \left( 1 - \frac{V_{OUT}}{V_{IN(MAX)}} \right)
\]

Once the value for \( L \) is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite, molypermalloy or Kool M\( \mu \) cores. A variety of inductors designed for high current, low voltage applications are available from manufacturers such as Sumida, Panasonic, Coiltronics, Coilcraft and Toko.

**Schottky Diode D1, D2 Selection**

The Schottky diodes, D1 and D2, shown in Figure 1 conduct during the dead time between the conduction of the power MOSFET switches. It is intended to prevent the body diodes of the top and bottom MOSFETs from turning on and storing charge during the dead time, which can cause a modest (about 1%) efficiency loss. The diodes can be rated for about one half to one fifth of the full load current since they are on for only a fraction of the duty cycle. In order for the diode to be effective, the inductance between it and the bottom MOSFET must be as small as possible, mandating that these components be placed adjacent. The diodes can be omitted if the efficiency loss is tolerable.

**C\( IN \) and C\( OUT \) Selection**

The input capacitance \( C_{IN} \) is required to filter the square wave current at the drain of the top MOSFET. Use a low ESR capacitor sized to handle the maximum RMS current.

\[
I_{RMS} = I_{OUT(MAX)} \sqrt{\frac{V_{IN}}{V_{OUT}}} \left( \frac{V_{IN}}{V_{OUT}} - 1 \right)
\]

This formula has a maximum at \( V_{IN} = 2V_{OUT} \), where \( I_{RMS} = I_{OUT(MAX)}/2 \). This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to derate the capacitor.

The selection of \( C_{OUT} \) is primarily determined by the ESR required to minimize voltage ripple and load step.
transients. The output ripple $\Delta V_{\text{OUT}}$ is approximately bounded by:

$$\Delta V_{\text{OUT}} \leq \Delta I_L \left( \text{ESR} + \frac{1}{8fC_{\text{OUT}}} \right)$$

Since $\Delta I_L$ increases with input voltage, the output ripple is highest at maximum input voltage. Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering and has the necessary RMS current rating.

Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR, but can be used in cost-sensitive applications providing that consideration is given to ripple current ratings and long term reliability. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing. When used as input capacitors, care must be taken to ensure that ringing from inrush currents and switching does not pose an overvoltage hazard to the power switches and controller. To dampen input voltage transients, add a small 5μF to 50μF aluminum electrolytic capacitor with an ESR in the range of 0.5Ω to 2Ω. High performance through-hole capacitors may also be used, but an additional ceramic capacitor in parallel is recommended to reduce the effect of their lead inductance.

**Top MOSFET Driver Supply ($C_B, D_B$)**

An external bootstrap capacitor $C_B$ connected to the BOOST pin supplies the gate drive voltage for the topside MOSFET. This capacitor is charged through diode $D_B$ from INTVcc when the switch node is low. When the top MOSFET turns on, the switch node rises to $V_{\text{IN}}$ and the BOOST pin rises to approximately $V_{\text{IN}} + \text{INTVcc}$. The boost capacitor needs to store about 100 times the gate charge required by the top MOSFET. In most applications a 0.1μF to 0.47μF X5R or X7R dielectric capacitor is adequate.

**Fault Condition: Current Limit**

The maximum inductor current is inherently limited in a current mode controller by the maximum sense voltage. In the LTC3718, the maximum sense voltage is controlled by the voltage on the VRNG pin. With valley current control, the maximum sense voltage and the sense resistance determine the maximum allowed inductor valley current. The corresponding output current limit is:

$$I_{\text{LIMITPOSITIVE}} = \frac{V_{\text{SNS(MAX)}}}{R_{\text{DS(ON)P}}} + \frac{1}{2} \Delta I_L$$

$$I_{\text{LIMITNEGATIVE}} = \frac{V_{\text{SNS(MIN)}}}{R_{\text{DS(ON)P}}} - \frac{1}{2} \Delta I_L$$

The current limit value should be checked to ensure that $I_{\text{LIMIT(MIN)}} > I_{\text{OUT(MAX)}}$. The minimum value of current limit generally occurs with the largest $V_{\text{IN}}$ at the highest ambient temperature, conditions that cause the largest power loss in the converter. Note that it is important to check for self-consistency between the assumed MOSFET junction temperature and the resulting value of $I_{\text{LIMIT}}$ which heats the MOSFET switches.

Caution should be used when setting the current limit based upon the $R_{\text{DS(ON)}}$ of the MOSFETs. The maximum current limit is determined by the minimum MOSFET on-resistance. Data sheets typically specify nominal and maximum values for $R_{\text{DS(ON)}}$, but not a minimum. A reasonable assumption is that the minimum $R_{\text{DS(ON)}}$ lies the same amount below the typical value as the maximum lies above it. Consult the MOSFET manufacturer for further guidelines.

**Minimum Off-time and Dropout Operation**

The minimum off-time $t_{\text{OFF(MIN)}}$ is the smallest amount of time that the LTC3718 is capable of turning on the bottom MOSFET, tripping the current comparator and turning the MOSFET back off. This time is generally about 250ns. The minimum off-time limit imposes a maximum duty cycle of $t_{\text{ON}}/(t_{\text{ON}} + t_{\text{OFF(MIN)}})$. If the maximum duty cycle is reached,
due to a dropping input voltage for example, then the output will drop out of regulation. The minimum input voltage to avoid dropout is:

\[ V_{IN(MIN)} = V_{OUT} \left( \frac{t_{ON} + t_{OFF(MIN)}}{t_{ON}} \right) \]

**Output Voltage Programming**

When \( V_{FB} \) is connected to \( V_{OUT} \), the output voltage is regulated to one half of the voltage at the \( V_{REF} \) pin. A resistor connected between \( V_{FB} \) and \( V_{OUT} \) can be used to further adjust the output voltage according to the following equation:

\[ V_{OUT} = V_{REF} \left( \frac{60k + R_{FB}}{120k} \right) \]

If \( V_{REF} \) exceeds 3V, resistors should be placed in series with the \( V_{REF} \) pin and the \( V_{FB} \) pin to avoid exceeding the input common mode range of the internal error amplifier. To maintain the \( V_{OUT} = V_{REF}/2 \) relationship, the resistor in series with the \( V_{REF} \) pin should be made twice as large as the resistor in series with the \( V_{FB} \) pin.

Alternately, the external buffer circuit shown in Figure 5 can be used. Note that the bipolar devices reduce the signal swing at the MOSFET gate.

**Soft-Start andLatchoff with the RUN/SS Pin**

The RUN/SS pin provides a means to shut down the LTC3718 as well as a timer for soft-start and overcurrent latchoff. Pulling the RUN/SS pin below 0.8V puts the LTC3718 into a low quiescent current shutdown (\( I_Q < 30\mu A \)). Releasing the pin allows an internal 1.2\( \mu A \) current source to charge up the external timing capacitor \( C_{SS} \). If RUN/SS has been pulled all the way to ground, there is a delay before starting of about:

\[ t_{DELAY} = \frac{1.5V}{1.2\mu A} C_{SS} = \left( \frac{1.3s\mu F}{C_{SS}} \right) \]

When the voltage on RUN/SS reaches 1.5V, the LTC3718 begins operating with a clamp on \( I_{TH} \) of approximately 0.9V. As the RUN/SS voltage rises to 3V, the clamp on \( I_{TH} \) is raised until its full 2.4V range is available. This takes an additional 1.3s/\( \mu F \), during which the load current is folded back. During start-up, the maximum load current is reduced until either the RUN/SS pin rises to 3V or the output reaches 75% of its final value. The pin can be driven from logic as shown in Figure 6. Diode D1 reduces the start delay while allowing \( C_{SS} \) to charge up slowly for the soft-start function.

**External Gate Drive Buffers**

The LTC3718 drivers are adequate for driving up to about 30nC into MOSFET switches with RMS currents of 50mA. Applications with larger MOSFET switches or operating at frequencies requiring greater RMS currents will benefit from using external gate drive buffers such as the LTC1693.
APPLICATIONS INFORMATION

persists until the RUN/SS pin drops to 3.5V, then the controller turns off both power MOSFETs, shutting down the converter permanently. The RUN/SS pin must be actively pulled down to ground in order to restart operation.

The overcurrent protection timer requires that the soft-start timing capacitor $C_{SS}$ be made large enough to guarantee that the output is in regulation by the time $C_{SS}$ has reached the 4V threshold. In general, this will depend upon the size of the output capacitance, output voltage and load current characteristic. A minimum soft-start capacitor can be estimated from:

$$C_{SS} > C_{OUT} \frac{V_{OUT}}{R_{SENSE}} (10^{-4} \text{[F/V s]})$$

Generally 0.1μF is more than sufficient.

Overcurrent latchoff operation is not always needed or desired. The feature can be overridden by adding a pull-up current greater than 5μA to the RUN/SS pin. The additional current prevents the discharge of $C_{SS}$ during a fault and also shortens the soft-start period. Connecting a resistor to $V_{IN}$ as shown in Figure 6a is simple, but slightly increases shutdown current. Connecting a resistor to $INTV_{CC}$ as shown in Figure 6b eliminates the additional shutdown current, but requires a diode to isolate $C_{SS}$. Any pull-up network must be able to pull RUN/SS above the 4.2V maximum threshold of the latchoff circuit and overcome the 4μA maximum discharge current.

$INTV_{CC}$ Supply

The 5V supply that powers the drivers and internal circuitry within the LTC3718 can be supplied by either an internal P-channel low dropout regulator if $V_{IN}$ is greater than 5V or the internal boost regulator if $V_{IN}$ is less than 5V. The $INTV_{CC}$ pin can supply up to 50mA RMS and must be bypassed to ground with a minimum of 4.7μF tantalum or other low ESR capacitor. Good bypassing is necessary to supply the high transient currents required by the MOSFET gate drivers. Applications using large MOSFETs with a high input voltage and high frequency of operation may cause the LTC3718 to exceed its maximum junction temperature rating or RMS current rating. In continuous mode operation, this current is $I_{GATECHG} \approx f(Q_{g(TOP)} + Q_{g(BOT)})$. The junction temperature can be estimated from the equations given in Note 2 of the Electrical Characteristics.

Inductor Selection for Boost Converter

For the boost converter, the inductance should be 4.7μH for input voltages less than 3.3V and 10μH for inputs above 3.3V. The inductor should have a saturation current rating of approximately 0.5A or greater. A guide for selecting an inductor for the boost converter is to choose a ripple current that is 40% of the current supplied by the boost converter. To ensure that the ripple current doesn’t exceed a specified amount, the inductance can be chosen according to the following equation:

$$L = \frac{V_{IN2(MIN)} (1 - \frac{V_{IN2(MAX)}}{V_{OUT(BOOST)}})}{\Delta I \cdot f}$$

Diode D3 Selection

A Schottky diode is recommended for use in the boost converter section. The Motorola MBR0520 is a very good choice.

Boost Converter Output Capacitor

Because the LTC3718’s boost converter is internally compensated, loop stability must be carefully considered when choosing its output capacitor. Small, low cost tantalum capacitors have some ESR, which aids stability. However, ceramic capacitors are becoming more popular, having attractive characteristics such as near-zero ESR, small size and reasonable cost. Simply replacing a tantalum output capacitor with a ceramic unit will decrease the phase margin, in some cases to unacceptable levels. With the addition of a phase-lead capacitor and isolating resistor, the boost converter portion of the LTC3718 can be used successfully with ceramic output capacitors.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Although all dissipative elements in the circuit produce losses, four main sources account for most of the losses in LTC3718 circuits:
APPLICATIONS INFORMATION

1. DC I^2R losses. These arise from the resistances of the MOSFETs, inductor and PC board traces and cause the efficiency to drop at high output currents. In continuous mode the average output current flows through L, but is chopped between the top and bottom MOSFETs. If the two MOSFETs have approximately the same R^DS(ON), then the resistance of one MOSFET can simply be summed with the resistances of L and the board traces to obtain the DC I^2R loss. For example, if R^DS(ON) = 0.01Ω and R_L = 0.005Ω, the loss will range from 1% up to 10% as the output current varies from 1A to 10A for a 1.5V output.

2. Transition loss. This loss arises from the brief amount of time the top MOSFET spends in the saturated region during switch node transitions. It depends upon the input voltage, load current, driver strength and MOSFET capacitance, among other factors. The loss is significant at input voltages above 20V and can be estimated from:

   Transition Loss \( \equiv (1.7A^{-1}) V^2 \) OUT \( \cdot \sum \) CRSS \( \cdot \) f

3. INTVCC current. This is the sum of the MOSFET driver and control currents.

4. C_IN loss. The input capacitor has the difficult job of filtering the large RMS input current to the regulator. It must have a very low ESR to minimize the AC I^2R loss and sufficient capacitance to prevent the RMS current from causing additional upstream losses in fuses or batteries.

Other losses, including C_OUT ESR loss, Schottky diode D1 conduction loss during dead time and inductor core loss generally account for less than 2% additional loss.

When making adjustments to improve efficiency, the input current is the best indicator of changes in efficiency. If you make a change and the input current decreases, then the efficiency has increased. If there is no change in input current, then there is no change in efficiency.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_OUT immediately shifts by an amount equal to \( \Delta I_{LOAD} \cdot (ESR) \), where ESR is the effective series resistance of C_OUT. \( \Delta I_{LOAD} \) also begins to charge or discharge C_OUT generating a feedback error signal used by the regulator to return V_OUT to its steady-state value. During this recovery time, V_OUT can be monitored for overshoot or ringing that would indicate a stability problem. The I_TH pin external components shown in Figure 1 will provide adequate compensation for most applications. For a detailed explanation of switching control loop theory see Application Note 76.

Design Example

As a design example, take a supply with the following specifications: VIN = 2.5V, V_OUT = 1.25V ±100mV, I_OUT(MAX) = ±6A, f = 300kHz. First, calculate the timing resistor with V_ON = V_OUT:

   \[ R_{ON} = \frac{2.5V - 0.7V}{(2.5V)(300kHz)(10pf)} = 240k \]

Next, use a standard value of 237k and choose the inductor for about 40% ripple current at the maximum VIN:

   \[ L = \frac{1.25V}{(300kHz)(0.4)(6A)} \cdot \left(1 - \frac{1.25V}{2.5V}\right) = 0.87\muH \]

Selecting a standard value of 1\muH results in a maximum ripple current of:

   \[ I_{L} = \frac{1.25V}{(300kHz)(1\muH)} \cdot \left(1 - \frac{1.25V}{2.5V}\right) = 2.1A \]

Next, choose the synchronous MOSFET switch. Choosing an IRF7811A (R^DS(ON) = 0.013Ω, C_RSS = 60pF, \( \theta_{JA} = 50^\circ C/W \)) yields a nominal sense voltage of:

   \[ V_{NSN}(NOM) = (6A)(1.3)(0.013\Omega) = 101.4mV \]

Tying VRNG to 1V will set the current sense voltage range for a nominal value of 100mV with current limit occurring at 133mV. To check if the current limit is acceptable, assume a junction temperature of about 10°C above a 50°C ambient with \( \rho_{60^\circ C} = 1.15 \):

   \[ I_{LIMIT} \geq \frac{133mV}{(1.15)(0.013\Omega)} + \frac{1}{2}(2.1A) = 9.9A \]
and double check the assumed $T_J$ in the MOSFET:

$$P_{BOT} = \frac{2.5V - 1.25V}{2.5V} \left( \frac{9.9A}{2} \right)^2 (1.15)(0.013\Omega)$$

$$= 0.18W$$

$$T_J = 50°C + (0.18W)(50°C/W) = 59°C$$

Now check the power dissipation of the top MOSFET at current limit with $\rho_{90°C} = 1.35$:

$$P_{TOP} = \frac{1.25V}{2.5V} \left( \frac{9.9A}{2} \right)^2 (1.35)(0.013\Omega)$$

$$+ \left(1.7\right)\left(2.5V\right)\left(9.9A\right)^2 (60\mu F)(300kHz)$$

$$= 0.87W$$

$$T_J = 50°C + (0.87W)(50°C/W) = 93.5°C$$

$C_{IN}$ is chosen for an RMS current rating of about 6A at temperature. The output capacitors are chosen for a low ESR of 0.005Ω to minimize output voltage changes due to inductor ripple current and load steps. The ripple voltage will be only:

$$\Delta V_{OUT(ripple)} = \Delta I_{L(MAX)} (ESR)$$

$$= (2.6A) (0.005\Omega) = 13mV$$

However, a 0A to 6A load step will cause an output change of up to:

$$\Delta V_{OUT(STEP)} = \Delta I_{LOAD} (ESR) = (6A) (0.005\Omega) = 30mV$$

The inductor for the boost converter is selected by first choosing an allowable ripple current. The boost converter will be operating in discontinuous mode. If we select a ripple current of 170mA for the boost converter, then:

$$L = \frac{3.3V \left(1 - \frac{3.3V}{5V}\right)}{(170mA)(1.4MHz)} = 4.7\mu H$$

The complete circuit is shown in Figure 7.

---

**Figure 7. Design Example: 1.25V±6A at 300kHz from 2.5V**
PC Board Layout Checklist

When laying out a PC board follow one of the two suggested approaches. The simple PC board layout requires a dedicated ground plane layer. Also, for higher currents, it is recommended to use a multilayer board to help with heat sinking power components.

- The ground plane layer should not have any traces and it should be as close as possible to the layer with power MOSFETs.

- Place C\textsubscript{IN}, C\textsubscript{OUT}, MOSFETs, D1 and inductor all in one compact area. It may help to have some components on the bottom side of the board.

- Place LTC3718 chip with Pins 13 to 24 facing the power components. Keep the components connected to Pins 1 to 12 close to LTC3718 (noise sensitive components).

- Use an immediate via to connect the components to ground plane including SGND and PGND of LTC3718. Use several bigger vias for power components.

- Use compact plane for switch node (SW) to improve cooling of the MOSFETs and to keep EMI down.

- Use planes for V\textsubscript{IN} and V\textsubscript{OUT} to maintain good voltage filtering and to keep power losses low.

- Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power component. You can connect the copper areas to any DC net (V\textsubscript{IN}, V\textsubscript{OUT}, GND or to any other DC rail in your system).

When laying out a printed circuit board, without a ground plane, use the following checklist to ensure proper operation of the controller. These items are also illustrated in Figure 8.

- Segregate the signal and power grounds. All small signal components should return to the SGND pin at one point which is then tied to the PGND pin close to the source of M2.

- Place M2 as close to the controller as possible, keeping the PGND, BG and SW traces short.

- Connect the input capacitor(s) C\textsubscript{IN} close to the power MOSFETs. This capacitor carries the MOSFET AC current.

- Keep the high dV/dt SW, BOOST and TG nodes away from sensitive small-signal nodes.

- Connect the INTV\textsubscript{CC} decoupling capacitor CV\textsubscript{CC} closely to the INTV\textsubscript{CC} and PGND pins.

- Connect the top driver boost capacitor C\textsubscript{B} closely to the BOOST and SW pins.

---

**Figure 8. LTC3718 Layout Diagram**
TYPICAL APPLICATION

One Half $V_{IN}$, ±10A Bus Terminator

PACKAGE DESCRIPTION

G Package
24-Lead Plastic SSOP (5.3mm)
(Reference LTC DWG # 05-08-1640)

NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN MILLIMETERS (INCHES)
3. DRAWING NOT TO SCALE

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.152mm (.006") PER SIDE
**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.254mm (.010") PER SIDE

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.
LTC3718

**TYPICAL APPLICATION**

Dual Output 2.5V, ±10A Buck Converter and 5V to 12V/130mA Boost Converter

**RELATED PARTS**

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>LT®1613</td>
<td>ThinSOT™ Step-Up DC/DC Converter</td>
<td>1.4MHz, 1.1V &lt; V_IN &lt; 10V</td>
</tr>
<tr>
<td>LTC1735</td>
<td>High Efficiency Synchronous Switching Regulator</td>
<td>4V ≤ V_IN ≤ 36V, 0.8V ≤ V_OUT ≤ 6V, SSOP-16</td>
</tr>
<tr>
<td>LTC1772</td>
<td>ThinSOT Current Mode Step-Down Controller</td>
<td>Small Solution, 2.5V ≤ V_IN ≤ 9.8V, 0.8V ≤ V_OUT ≤ V_IN</td>
</tr>
<tr>
<td>LTC1773</td>
<td>Synchronous Current Mode Step-Down Controller</td>
<td>2.65V ≤ V_IN ≤ 8.5V, 0.8V ≤ V_OUT ≤ V_IN, 550kHz Operation, &gt;90% Efficiency</td>
</tr>
<tr>
<td>LTC1778</td>
<td>No RSENSE™ Synchronous Step-Down Controller</td>
<td>No Sense Resistor Required, 4V ≤ V_IN ≤ 36V, 0.8V ≤ V_OUT ≤ V_IN</td>
</tr>
<tr>
<td>LTC1876</td>
<td>2-Phase, Dual Synchronous Step-Down Controller with Step-Up Regulator</td>
<td>2.6V ≤ V_IN ≤ 36V, Dual Output: 0.8V ≤ V_OUT ≤ (0.9)V_IN</td>
</tr>
<tr>
<td>LTC3413</td>
<td>3A Monolithic DDR Memory Termination Regulator</td>
<td>±3A Output Current, 2.25V ≤ V_IN ≤ 5.5V</td>
</tr>
<tr>
<td>LTC3711</td>
<td>5-Bit, Adjustable, No RSENSE Synchronous Step-Down Controller</td>
<td>0.925V ≤ V_OUT ≤ 2V, 4V ≤ V_IN ≤ 36V</td>
</tr>
<tr>
<td>LTC3713</td>
<td>Low Input Voltage, High Power, No RSENSE Synchronous Controller</td>
<td>No Sense Resistor Required, V_IN(MIN) = 1.5V</td>
</tr>
<tr>
<td>LTC3717</td>
<td>High Power DDR Memory Termination Regulator</td>
<td>4V ≤ V_IN ≤ 36V, V_OUT Tracks V_IN or V_REF, I_OUT from 1A to 20A</td>
</tr>
<tr>
<td>LTC3778</td>
<td>No RSENSE Synchronous Step-Down Controller</td>
<td>Optional Sense Resistor, 4V ≤ V_IN ≤ 36V, 0.6V ≤ V_OUT ≤ V_IN</td>
</tr>
<tr>
<td>LTC3831</td>
<td>High Power DDR Memory Termination Regulator</td>
<td>V_OUT Tracks 1/2 V_IN or V_REF, 3V ≤ V_IN ≤ 8V, I_OUT from 1A to 20A</td>
</tr>
</tbody>
</table>

No RSENSE and ThinSOT are trademarks of Linear Technology Corporation.