The LTC®3716 is a 2-phase, VID programmable, synchronous step-down switching regulator controller that drives two N-channel external power MOSFET stages in a fixed frequency architecture. The 2-phase controller drives its two output stages out of phase at frequencies up to 300kHz to minimize the RMS ripple currents in both input and output capacitors. The 2-phase technique effectively multiplies the fundamental frequency by two, improving transient response while operating each channel at an optimum frequency for efficiency. Thermal design is also simplified.

An operating mode select pin (FCB) can be used to regulate a secondary winding or select among three modes including Burst Mode™ operation for highest efficiency. An internal differential amplifier provides true remote sensing of the regulated supply’s positive and negative output terminals as required in high current applications.

The RUN/SS pin provides soft-start and optional timed, short-circuit shutdown. Current foldback limits MOSFET dissipation during short-circuit conditions when the overcurrent latchoff is disabled. OPTI-LOOP compensation allows the transient response to be optimized for a wide range of output capacitors and ESR values.

**FEATURES**
- Output Stages Operate Antiphase Reducing Input and Output Capacitance Requirements and Power Supply Induced Noise
- Dual Input Supply Capability for Load Sharing
- 5-Bit Mobile VID Code: $V_{OUT} = 0.6V$ to $1.75V$
- $\pm 1\%$ Output Voltage Accuracy
- True Remote Sensing Differential Amplifier
- Power Good Output Voltage Monitor
- Supports Active Voltage Positioning
- Current Mode Control Ensures Current Sharing
- OPTI-LOOP™ Compensation Minimizes $C_{OUT}$
- Three Operational Modes: PWM, Burst and Cycle Skip
- Programmable Fixed Frequency: 150kHz to 300kHz
- Wide $V_{IN}$ Range: 4V to 36V Operation
- Adjustable Soft-Start Current Ramping
- Internal Current Foldback and Short-Circuit Shutdown
- Overvoltage Soft Latch Eliminates Nuisance Trips
- Available in 36-Lead Narrow SSOP Package

**APPLICATIONS**
- Mobile Computer CPU Supply

---

Linear Technology Corporation

LTC and LT are registered trademarks of Linear Technology Corporation.

OPTI-LOOP and Burst Mode are trademarks of Linear Technology Corporation.

TYPICAL APPLICATION

Figure 1. High Current Dual Phase Step-Down Converter
**ABSOLUTE MAXIMUM RATINGS**

(Note 1)
- Input Supply Voltage ($V_{IN}$)...........36V to –0.3V
- Topside Driver Voltages (BOOST1, 2).........42V to –0.3V
- Switch Voltage (SW1, 2).........................36V to –5V
- $SENSE1^+, SENSE2^+, SENSE1^–, SENSE2^–$ Voltages ...........$–0.3V$ to $–0.3V$
- $EAIN, V\text{OS}^+, V\text{OS}^–, EXT\text{VCC}, INT\text{VCC}, RUN/SS,$
- $V_{BIAS,\, ATTE\text{NIN, ATTE\text{NOUT, PGOOD, AMPMD,}}}$
- $VIDO–VID4,$ Voltages .........................$7V$ to $–0.3V$
- Boosted Driver Voltage (BOOST-SW)..............$7V$ to $–0.3V$
- PLLFLTR, PLLIN, $V_{DIFFOUT},$
- $I_{TH}$ Voltage .................................................$–2.7V$ to $–0.3V$
- Peak Output Current <$1\mu A$(TG1, 2, BG1, 2)..............$3A$
- $INT\text{VCC}$ RMS Output Current......................$50mA$
- Operating Ambient Temperature Range
  (Note 2) .............................................$–40^\circ C$ to $85^\circ C$
- Junction Temperature (Note 3)..................$125^\circ C$
- Storage Temperature Range ......................$–65^\circ C$ to $150^\circ C$
- Lead Temperature (Soldering, 10 sec)...........$300^\circ C$
- $T_{JMAX} = 125^\circ C, \theta_{JA} = 85^\circ C/W$

Consult factory for parts specified with wider operating temperature ranges.

**ELECTRICAL CHARACTERISTICS**

- The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ C, V_{IN} = 15V, V_{BIAS} = 5V, V_{RUN/SS} = 5V$ unless otherwise noted.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{EAIN}$</td>
<td>Regulated Feedback Voltage</td>
<td>$I_{TH}$ Voltage = $1.2V$; Measured at $V_{EAIN}$ (Note 4)</td>
<td>●</td>
<td>0.594</td>
<td>0.600</td>
<td>0.606</td>
</tr>
<tr>
<td>$V_{SENSEMAX}$</td>
<td>Maximum Current Sense Threshold</td>
<td></td>
<td>●</td>
<td>62</td>
<td>75</td>
<td>88</td>
</tr>
<tr>
<td>$I_{INEAIN}$</td>
<td>Feedback Current</td>
<td></td>
<td>●</td>
<td>–5</td>
<td>–50</td>
<td>nA</td>
</tr>
<tr>
<td>$V_{LOADREG}$</td>
<td>Output Voltage Load Regulation</td>
<td>(Note 4)</td>
<td>●</td>
<td>0.1</td>
<td>0.5</td>
<td>%</td>
</tr>
<tr>
<td>$V_{REFLNREG}$</td>
<td>Reference Voltage Line Regulation</td>
<td>$M = 3.6V$ to $30V$ (Note 4)</td>
<td></td>
<td>0.002</td>
<td>0.02</td>
<td>%/V</td>
</tr>
<tr>
<td>$V_{FCB}$</td>
<td>Forced Continuous Threshold</td>
<td></td>
<td>●</td>
<td>0.57</td>
<td>0.6</td>
<td>0.63</td>
</tr>
<tr>
<td>$I_{FCB}$</td>
<td>Forced Continuous Current</td>
<td></td>
<td>●</td>
<td>–0.17</td>
<td>–1</td>
<td>μA</td>
</tr>
<tr>
<td>$V_{BINHIBIT}$</td>
<td>Burst Inhibit (Constant Frequency)</td>
<td>$\text{Threshold}$</td>
<td>●</td>
<td>4.3</td>
<td>4.8</td>
<td>V</td>
</tr>
<tr>
<td>$V_{OVL}$</td>
<td>Output Overvoltage Threshold</td>
<td>Measured at $V_{EAIN}$</td>
<td>●</td>
<td>0.64</td>
<td>0.66</td>
<td>0.68</td>
</tr>
<tr>
<td>$UVLO$</td>
<td>Undervoltage Lockout</td>
<td>$V_{R}$ Ramping Down</td>
<td>3</td>
<td>3.33</td>
<td>4</td>
<td>V</td>
</tr>
<tr>
<td>$g_m$</td>
<td>Transconductance Amplifier $g_m$</td>
<td>$I_{TH} = 1.2V, SINK/Source 5\mu A$ (Note 4)</td>
<td>●</td>
<td>3</td>
<td></td>
<td>mmho</td>
</tr>
<tr>
<td>$g_{mol}$</td>
<td>Transconductance Amplifier Gain</td>
<td>$I_{TH} = 1.2V, (g_m \cdot Z_l; No Ext Load)$ (Note 4)</td>
<td>●</td>
<td>1.5</td>
<td></td>
<td>V/mV</td>
</tr>
</tbody>
</table>
**ELECTRICAL CHARACTERISTICS**

The **●** denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. $V_{IN} = 15V$, $V_{BIAS} = 5V$, $V_{RUN/SS} = 5V$ unless otherwise noted.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_D$</td>
<td>Input DC Supply Current Normal Mode Shutdown</td>
<td>$V_{RUN/SS} = 0V$</td>
<td>1.2</td>
<td>20</td>
<td>40</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{RUN/SS}$</td>
<td>Soft-Start Charge Current</td>
<td>$V_{RUN/SS} = 1.9V$</td>
<td>$-0.5$</td>
<td>$-1.2$</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>$I_{V_{RUN/SS}}$</td>
<td>RUN/SS Pin ON Threshold $V_{RUN/SS} = 1.9V$</td>
<td></td>
<td>1.0</td>
<td>1.5</td>
<td>1.9</td>
<td>V</td>
</tr>
<tr>
<td>$I_{V_{RUN/SS}}$</td>
<td>RUN/SS Pin Latchoff Arming $V_{RUN/SS} = 3V$</td>
<td></td>
<td>4.1</td>
<td>4.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{SC}_{\text{L}}$</td>
<td>RUN/SS Discharge Current Soft Short Condition $V_{EAIN} = 0.5V$, $V_{RUN/SS} = 4.5V$</td>
<td></td>
<td>0.5</td>
<td>2</td>
<td>4</td>
<td>µA</td>
</tr>
<tr>
<td>$I_{S_{DLH}}$</td>
<td>Shutdown Latch Disable Current</td>
<td></td>
<td>1.6</td>
<td>5</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>$I_{SH}$</td>
<td>Total Sense Pins Source Current Each Channel: $V_{SENSE1–, 2–} = V_{SENSE1+, 2+} = 0V$</td>
<td>$-85$</td>
<td>$-60$</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>$D_{P_{\text{MAX}}}$</td>
<td>Maximum Duty Factor</td>
<td>In Dropout</td>
<td>98</td>
<td>99.5</td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>$T_{G1, 2}$</td>
<td>Top Gate Transition Time: Rise Time $C_{LOAD} = 3300pF$</td>
<td></td>
<td>30</td>
<td>90</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$T_{G1, 2}$</td>
<td>Fall Time $C_{LOAD} = 3300pF$</td>
<td></td>
<td>40</td>
<td>90</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$B_{G1, 2}$</td>
<td>Bottom Gate Transition Time: Rise Time $C_{LOAD} = 3300pF$</td>
<td></td>
<td>30</td>
<td>90</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$B_{G1, 2}$</td>
<td>Fall Time $C_{LOAD} = 3300pF$</td>
<td></td>
<td>20</td>
<td>90</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$T_{G/BG_{1D}}$</td>
<td>Top Gate Off to Bottom Gate On Delay Synchronous Switch-On Delay Time $C_{LOAD} = 3300pF$ Each Driver (Note 6)</td>
<td></td>
<td>90</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$B_{G/TG_{1D}}$</td>
<td>Bottom Gate Off to Top Gate On Delay Top Switch-On Delay Time $C_{LOAD} = 3300pF$ Each Driver (Note 6)</td>
<td></td>
<td>90</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$I_{ON(MIN)}$</td>
<td>Minimum On-Time Tested with a Square Wave (Note 7)</td>
<td></td>
<td>180</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

**Internal $V_{CC}$ Regulator**

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{INTVCC}$</td>
<td>Internal $V_{CC}$ Voltage $6V &lt; V_{IN} &lt; 30V$, $V_{EXTVCC} = 4V$</td>
<td></td>
<td>4.8</td>
<td>5.0</td>
<td>5.2</td>
<td>V</td>
</tr>
<tr>
<td>$V_{LDO INT}$</td>
<td>INT$CC$ Load Regulation $I_{CC} = 0$ to $20mA$, $V_{EXTVCC} = 4V$</td>
<td></td>
<td>0.2</td>
<td>1.0</td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>$V_{LDO EXT}$</td>
<td>EXTVCC Voltage Drop $I_{CC} = 20mA$, $V_{EXTVCC} = 5V$</td>
<td></td>
<td>80</td>
<td>160</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>$V_{EXTVCC}$</td>
<td>EXTVCC Switchover Voltage $I_{CC} = 20mA$, EXTVCC Ramping Positive</td>
<td></td>
<td>4.5</td>
<td>4.7</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{LDOHYS}$</td>
<td>EXTVCC Switchover Hysteresis $I_{CC} = 20mA$, EXTVCC Ramping Negative</td>
<td></td>
<td>0.2</td>
<td></td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

**VID Parameters**

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{BIAS}$</td>
<td>Operating Supply Voltage Range</td>
<td></td>
<td>2.7</td>
<td>5.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$R_{ATTEN}$</td>
<td>Resistance Between ATTENIN and ATTENOUT Pins</td>
<td></td>
<td>10</td>
<td></td>
<td></td>
<td>kΩ</td>
</tr>
<tr>
<td>$R_{ATTENERR}$</td>
<td>Resistive Divider Error</td>
<td>$-0.25$</td>
<td>0.25</td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>$R_{PULLUP}$</td>
<td>VID0 to VID4 Pull-Up Resistance (Note 8)</td>
<td></td>
<td>40</td>
<td></td>
<td></td>
<td>kΩ</td>
</tr>
<tr>
<td>$V_{THLOW}$</td>
<td>VID0 to VID4 Logic Threshold Low</td>
<td></td>
<td>0.4</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{THHIGH}$</td>
<td>VID0 to VID4 Logic Threshold High</td>
<td></td>
<td>1.6</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{LEAK}$</td>
<td>VID0 to VID4 Leakage $V_{BIAS} &lt; VID0–VID4 &lt; 7V$</td>
<td></td>
<td>±1</td>
<td></td>
<td></td>
<td>μA</td>
</tr>
</tbody>
</table>

**Oscillator and Phase-Locked Loop**

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{NOM}$</td>
<td>Nominal Frequency $V_{PLLFLTR} = 1.2V$</td>
<td></td>
<td>190</td>
<td>220</td>
<td>250</td>
<td>kHz</td>
</tr>
<tr>
<td>$f_{LOW}$</td>
<td>Lowest Frequency $V_{PLLFLTR} = 0V$</td>
<td></td>
<td>120</td>
<td>140</td>
<td>160</td>
<td>kHz</td>
</tr>
<tr>
<td>$f_{HIGH}$</td>
<td>Highest Frequency $V_{PLLFLTR} &gt; 2.4V$</td>
<td></td>
<td>280</td>
<td>310</td>
<td>360</td>
<td>kHz</td>
</tr>
<tr>
<td>$R_{PLLIN}$</td>
<td>PLLIN Input Resistance</td>
<td></td>
<td>50</td>
<td></td>
<td></td>
<td>kΩ</td>
</tr>
<tr>
<td>$I_{PLLFLTR}$</td>
<td>Phase Detector Output Current Sinking Capability $f_{PLLIN} &lt; f_{OSC}$</td>
<td></td>
<td>$-15$</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>$I_{PLLFLTR}$</td>
<td>Phase Detector Output Current Sourcing Capability $f_{PLLIN} &gt; f_{OSC}$</td>
<td></td>
<td>15</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>$R_{RELPHS}$</td>
<td>Controller 2-Controller 1 Phase</td>
<td></td>
<td>180</td>
<td></td>
<td></td>
<td>Deg</td>
</tr>
</tbody>
</table>
ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at \( T_A = 25^°C \). \( V_{IN} = 15V \), \( V_{BIAS} = 5V \), \( V_{RUN/SS} = 5V \) unless otherwise noted.

### SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS
--- | --- | --- | --- | --- | --- | ---
PGOOD Output

| V\(_{PGL}\) | PGOOD Voltage Low | \( I_{PGOOD} = 2mA \) | 0.1 | 0.3 | V |
| I\(_{PGOOD}\) | PGOOD Leakage Current | \( V_{PGOOD} = 5V \) | ±1 | | \( \mu A \) |
| \( V_{PG} \) | PGOOD Trip Level, Either Controller | \( V_{EAIN} \) with Respect to Set Output Voltage | –8 | –10 | –12 | % |
| | | \( V_{EAIN} \) Ramping Negative | 8 | 10 | 12 | % |

### Differential Amplifier/Op Amp Gain Block

| \( A_{D\text{A}} \) | Differential Amplifier Gain | \( V_{\text{AMPMD}} = 0V \) | 0.995 | 1 | 1.005 | V/V |
| CMRR\(_{D\text{A}}\) | Common Mode Rejection Ratio | \( 0V < V_{CM} < 5V ; V_{\text{AMPMD}} = 0V \) | 46 | 55 | | dB |
| \( R_{IN} \) | Input Resistance | Measured at \( V_{OS+} \) Input; \( V_{\text{AMPMD}} = 0V \) | 80 | | kΩ |
| \( V_{DS} \) | Input Offset Voltage | Op Amp Mode; \( V_{CM} = 2.5V ; V_{\text{AMPMD}} = 5V \) | 6 | | mV |
| \( I_{B} \) | Input Bias Current | Op Amp Mode; \( V_{\text{AMPMD}} = 5V \) | 30 | 200 | nA |
| \( A_{OL} \) | Open-Loop DC Gain | Op Amp Mode; \( 0.7V \leq V_{\text{DIFFOUT}} < 10V ; V_{\text{AMPMD}} = 5V \) | 5000 | | V/mV |
| \( V_{CM} \) | Common Mode Input Voltage Range | Op Amp Mode; \( V_{\text{AMPMD}} = 5V \) | 0 | 3 | | V |
| CMRR\(_{O\text{A}}\) | Common Mode Rejection Ratio | Op Amp Mode; \( 0V < V_{CM} < 3V ; V_{\text{AMPMD}} = 5V \) | 70 | 90 | | dB |
| PSRR\(_{D\text{A}}\) | Power Supply Rejection Ratio | Op Amp Mode; \( 6V < V_{IN} < 30V ; V_{\text{AMPMD}} = 5V \) | 70 | 90 | | dB |
| \( I_{CL} \) | Maximum Output Current | Op Amp Mode; \( V_{\text{DIFFOUT}} = 0V ; V_{\text{AMPMD}} = 5V \) | 10 | 35 | | mA |
| \( V_{DMAX} \) | Maximum Output Voltage | Op Amp Mode; \( I_{\text{DIFFOUT}} = 1mA ; V_{\text{AMPMD}} = 5V \) | 10 | 11 | | V |
| GBW | Gain-Bandwidth Product | Op Amp Mode; \( I_{\text{DIFFOUT}} = 1mA ; V_{\text{AMPMD}} = 5V \) | 2 | | MHz |
| SR | Slew Rate | Op Amp Mode; \( R_{L} = 2k ; V_{\text{AMPMD}} = 5V \) | 5 | | V/μs |

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

**Note 2:** The LTC3716 is guaranteed to meet performance specifications from \( 0°C \) to \( 70°C \). Specifications over the \( -40°C \) to \( 85°C \) operating temperature range are assured by design, characterization and correlation with statistical process controls.

**Note 3:** \( T_J \) is calculated from the ambient temperature \( T_A \) and power dissipation \( P_D \) according to the following formula:

\[
T_J = T_A + (P_D \cdot 85°C/W)
\]

**Note 4:** The LTC3716 is tested in a feedback loop that servos \( V_{ITH} \) to a specified voltage and measures the resultant \( V_{EAIN} \).

**Note 5:** Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Applications Information.

**Note 6:** Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels.

**Note 7:** The minimum on-time condition corresponds to the on inductor peak-to-peak ripple current \( \geq 40\% I_{MAX} \) (see Minimum On-Time Considerations in the Applications Information section).

**Note 8:** Each built-in pull-up resistor attached to the VID inputs also has a series diode to allow input voltages higher than the \( V_{VIDVCC} \) supply without damage or clamping (see the Applications Information section).
TYPICAL PERFORMANCE CHARACTERISTICS

**Efficiency vs Load Current**
(3 Operating Modes) (Figure 13)

**Efficiency vs Load Current**
(Figure 13)

**Efficiency vs Input Voltage**
(Figure 13)

**Supply Current vs Input Voltage and Mode**

**EXTVCC Voltage Drop**

**INTVCC and EXTVCC Switch Voltage vs Temperature**

**Internal 5V LDO Line Reg**

**Maximum Current Sense Threshold vs Duty Factor**

**Maximum Current Sense Threshold vs Percent of Nominal Output Voltage (Foldback)**
**TYPICAL PERFORMANCE CHARACTERISTICS**

**Maximum Current Sense Threshold vs VRUN/SS (Soft-Start)**

![Graph showing maximum current sense threshold vs VRUN/SS.](image1)

**Load Regulation**

![Graph showing load regulation.](image2)

**VITH vs VRUN/SS (Soft-Start)**

![Graph showing VITH vs VRUN/SS.](image3)

**SENSE Pins Total Source Current**

![Graph showing sense pins total source current.](image4)

**Maximum Current Sense Threshold vs Temperature**

![Graph showing maximum current sense threshold vs temperature.](image5)

**RUN/SS Current vs Temperature**

![Graph showing run/SS current vs temperature.](image6)

**Soft-Start Up (Figure 13)**

![Graph showing soft-start up.](image7)
TYPICAL PERFORMANCE CHARACTERISTICS

Load Step (Figure 13)

Current Sense Pin Input Current vs Temperature

EXTVCC Switch Resistance vs Temperature

Oscillator Frequency vs Temperature

Undervoltage Lockout vs Temperature

VRUN/SS Shutdown Latch Thresholds vs Temperature
**PIN FUNCTIONS**

**RUN/SS (Pin 1):** Combination of Soft-Start, Run Control Input and Short-Circuit Detection Timer. A capacitor to ground at this pin sets the ramp time to full current output. Forcing this pin below 0.8V causes the IC to shut down all internal circuitry. All functions are disabled in shutdown.

**SENSE+, SENSE2+ (Pins 2, 14):** The (+) Input to Each Differential Current Comparator. The $I_T$ pin voltage and built-in offsets between SENSE– and SENSE+ pins in conjunction with $R_{SENSE}$ set the current trip threshold.

**SENSE1–, SENSE2– (Pins 3, 13):** The (–) Input to the Differential Current Comparators.

**EAIN (Pin 4):** Input to the error amplifier that compares the feedback voltage to the internal 0.6V reference voltage. This pin is normally connected to a resistive divider from the output of the differential amplifier (DIFFOUT).

**PLLFLTR (Pin 5):** The phase-locked loop’s lowpass filter is tied to this pin. Alternatively, this pin can be driven with an AC or DC voltage source to vary the frequency of the internal oscillator. Do not apply voltage to this pin prior to application of $V_{IN}$.

**PLLIN (Pin 6):** External Synchronization Input to Phase Detector. This pin is internally terminated to SGND with 50kΩ. The phase-locked loop will force the rising top gate signal of controller 1 to be synchronized with the rising edge of the PLLIN signal.

**FCB (Pin 7):** Forced Continuous Control Input. This input acts on both output stages and can be used to regulate a secondary winding. Pulling this pin below 0.6V will force continuous synchronous operation. Do not leave this pin floating without a decoupling capacitor.

**I_TH (Pin 8):** Error Amplifier Output and Switching Regulator Compensation Point. Both current comparator’s thresholds increase with this control voltage. The normal voltage range of this pin is from 0V to 2.4V

**SGND (Pin 9):** Signal Ground. This pin is common to both controllers. Route separately to the PGND pin.

**V_DIFFOUT (Pin 10):** Output of a Differential Amplifier. This pin provides true remote output voltage sensing. $V_{DIFFOUT}$ normally drives an external resistive divider that sets the output voltage.

**V_OS–, V_OS+ (Pins 11, 12):** Inputs to an Operational Amplifier. Internal precision resistors configure it as a differential amplifier whose output is $V_{DIFFOUT}$.

**ATTENOUT (Pin 15):** Voltage Feedback Signal Resistively Divided According to the VID Programming Code.

**ATTENIN (Pin 16):** The Input to the VID Controlled Resistive Divider.

**VID0–VID4 (Pins 17, 18, 19, 20, 21):** VID Control Logic Input Pins.

**V_BIAS (Pin 22):** Supply Pin for the VID Control Circuit.

**AMPMD (Pin 23):** This Logic Input pin controls the connections of internal precision resistors that configure the operational amplifier as a unity-gain differential amplifier.

**TG2, TG1 (Pins 24, 35):** High Current Gate Drives for Top N-Channel MOSFETS. These are the outputs of floating drivers with a voltage swing equal to INTVCC superimposed on the switch node voltage SW.

**SW2, SW1 (Pins 25, 34):** Switch Node Connections to Inductors. Voltage swing at these pins is from a Schottky diode (external) voltage drop below ground to $V_{IN}$.

**BOOST2, BOOST1 (Pins 26, 33):** Bootstrapped Supplies to the Topside Floating Drivers. External capacitors are connected between the BOOST and SW pins, and Schottky diodes are connected between the BOOST and INTVCC pins.

**BG2, BG1 (Pins 27, 31):** High Current Gate Drives for Bottom N-Channel MOSFETS. Voltage swing at these pins is from ground to INTVCC.

**PGND (Pin 28):** Driver Power Ground. Connect to sources of bottom N-channel MOSFETS and the (–) terminals of $C_{IN}$.

**INTVCC (Pin 29):** Output of the Internal 5V Linear Low Dropout Regulator and the EXTVCC Switch. The driver and control circuits are powered from this voltage source. Decouple to power ground with a 1μF ceramic capacitor placed directly adjacent to the IC and minimum of 4.7μF additional tantalum or other low ESR capacitor.

**EXTVCC (Pin 30):** External Power Input to an Internal Switch. This switch closes and supplies INTVCC, bypassing the internal low dropout regulator whenever $V_{EXTVCC}$ is higher than 4.7V. See EXTVCC Connection in the Applications Information section. Do not exceed 7V on this pin and ensure $V_{EXTVCC} \leq V_{INTVCC}$.
**PIN FUNCTIONS**

**V_{IN}** (Pin 32): Main Supply Pin. Should be closely decoupled to the IC’s signal ground pin.

**PGOOD** (Pin 36): Open-Drain Logic Output. PGOOD is pulled to ground when the voltage on the EAIN pin is not within ±10% of its set point.
**OPERATION**  (Refer to Functional Diagram)

**Main Control Loop**

The LTC3716 uses a constant frequency, current mode step-down architecture with the two output stages operating 180 degrees out of phase. During normal operation, each top MOSFET is turned on when the clock for that channel sets the RS latch, and turned off when the main current comparator, \( I_1 \), resets the RS latch. The peak inductor current at which \( I_1 \) resets the RS latch is controlled by the voltage on the \( I_{TH} \) pin, which is the output of error amplifier EA. The EAIN pin receives the voltage feedback signal, which is compared to the internal reference voltage by the EA. When the load current increases, it causes a slight decrease in \( V_{EAIN} \) relative to the 0.6V reference, which in turn causes the \( I_{TH} \) voltage to increase until the average inductor current matches the new load current. After the top MOSFET has turned off, the bottom MOSFET is turned on until either the inductor current starts to reverse, as indicated by current comparator \( I_2 \), or the beginning of the next cycle.

The top MOSFET drivers are biased from floating bootstrap capacitor \( C_B \), which normally is recharged during each off cycle through an external diode when the top MOSFET turns off. As \( V_{IN} \) decreases to a voltage close to \( V_{OUT} \), the loop may enter dropout and attempt to turn on the top MOSFET continuously. The dropout detector detects this and forces the top MOSFET off for about 500ns every tenth cycle to allow \( C_B \) to recharge.

The main control loop is shut down by pulling the RUN/SS pin low. Releasing RUN/SS allows an internal 1.2\( \mu \)A current source to charge soft-start capacitor \( C_{SS} \). When \( C_{SS} \) reaches 1.5V, the main control loop is enabled with the \( I_{TH} \) voltage clamped at approximately 30% of its maximum value. As \( C_{SS} \) continues to charge, the \( I_{TH} \) pin voltage is gradually released allowing normal, full-current operation.

**Low Current Operation**

The FCB pin is a multifunction pin providing two functions: 1) to provide regulation for a secondary winding by temporarily forcing continuous PWM operation on both controllers; and 2) select between two modes of low current operation. When the FCB pin voltage is below 0.6V, the controller forces continuous PWM current mode operation. In this mode, the top and bottom MOSFETs are alternately turned on to maintain the output voltage independent of direction of inductor current. When the FCB pin is below \( V_{INTVCC} - 2V \) but greater than 0.6V, the controller enters Burst Mode operation. Burst Mode operation sets a minimum output current level before inhibiting the top switch and turns off the synchronous MOSFET(s) when the inductor current goes negative. This combination of requirements will, at low currents, force the \( I_{TH} \) pin below a voltage threshold that will temporarily inhibit turn-on of both output MOSFETs until the output voltage drops. There is 60mV of hysteresis in the burst comparator B tied to the \( I_{TH} \) pin. This hysteresis produces output signals to the MOSFETs that turn them on for several cycles, followed by a variable “sleep” interval depending upon the load current. The resultant output voltage ripple is held to a very small value by having the hysteretic comparator after the error amplifier gain block.

**Constant Frequency Operation**

When the FCB pin is tied to INTVCC, Burst Mode operation is disabled and a forced minimum peak output current requirement is removed. This provides constant frequency, discontinuous (preventing reverse inductor current) current operation over the widest possible output current range. This constant frequency operation is not as efficient as Burst Mode operation, but does provide a lower noise, constant frequency operating mode down to approximately 1% of designed maximum output current.

**Continuous Current (PWM) Operation**

Tying the FCB pin to ground will force continuous current operation. This is the least efficient operating mode, but may be desirable in certain applications. The output can source or sink current in this mode. When sinking current while in forced continuous operation, current will be forced back into the main power supply potentially boosting the input supply to dangerous voltage levels—BEWARE!
**OPERATION**  
*(Refer to Functional Diagram)*

**Frequency Synchronization**

The phase-locked loop allows the internal oscillator to be synchronized to an external source via the PLLIN pin. The output of the phase detector at the PLLFLTR pin is also the DC frequency control input of the oscillator that operates over a 140kHz to 310kHz range corresponding to a DC voltage input from 0V to 2.4V. When locked, the PLL aligns the turn on of the top MOSFET to the rising edge of the synchronizing signal. When PLLIN is left open, the PLLFLTR pin goes low, forcing the oscillator to minimum frequency.

Input capacitance ESR requirements and efficiency losses are substantially reduced because the peak current drawn from the input capacitor is effectively divided by two and power loss is proportional to the RMS current squared. A two stage, single output voltage implementation can reduce input path power loss by 75% and radically reduce the required RMS current rating of the input capacitor(s).

**INTVCC/EXTVCC Power**

Power for the top and bottom MOSFET drivers and most of the IC circuitry is derived from INTVCC. When the EXTVCC pin is left open, an internal 5V low dropout regulator supplies INTVCC power. If the EXTVCC pin is taken above 4.8V, the 5V regulator is turned off and an internal switch is turned on connecting EXTVCC to INTVCC. This allows the INTVCC power to be derived from a high efficiency external source such as the output of the regulator itself or a secondary winding, as described in the Applications Information section. An external Schottky diode can be used to minimize the voltage drop from EXTVCC to INTVCC in applications requiring greater than the specified INTVCC current. Voltages up to 7V can be applied to EXTVCC for additional gate drive capability.

**Differential Amplifier**

This amplifier provides true differential output voltage sensing. Sensing both $V_{OUT}^+$ and $V_{OUT}^-$ benefits regulation in high current applications and/or applications having electrical interconnection losses. The AMPMD pin allows selection of internal precision feedback resistors for high common mode rejection differencing applications, or direct access to the actual amplifier inputs without these internal feedback resistors for other applications.

The AMPMD pin is grounded to connect the internal precision resistors in a unity-gain differencing application or tied to the INTVCC pin to bypass the internal resistors and make the amplifier inputs directly available. The amplifier is a unity-gain stable, 2MHz gain-bandwidth, >120dB open-loop gain design. The amplifier has an output slew rate of 5V/μs and is capable of driving capacitive loads with an output RMS current typically up to 25mA. The amplifier is not capable of sinking current and therefore must be resistively loaded to do so.

**Output Overvoltage Protection**

An overvoltage comparator, 0V, guards against transient overshoots (>10%) as well as other more serious conditions that may overvoltage the output. In this case, the top MOSFET is turned off and the bottom MOSFET is turned on until the overvoltage condition is cleared.

**Power Good (PGOOD)**

The PGOOD pin is connected to the drain of an internal MOSFET. The MOSFET turns on when the output voltage is not within ±10% of its nominal output level as determined by the feedback divider. When the output is within ±10% of its nominal value, the MOSFET is turned off within 10μs and the PGOOD pin should be pulled up by an external resistor to a source of up to 7V.

**Short-Circuit Detection**

The RUN/SS capacitor is used initially to limit the inrush current from the input power source. Once the controllers have been given time, as determined by the capacitor on the RUN/SS pin, to charge up the output capacitors and provide full-load current, the RUN/SS capacitor is then used as a short-circuit timeout circuit. If the output voltage falls to less than 70% of its nominal output voltage the RUN/SS capacitor begins discharging assuming that the output is in a severe overcurrent and/or short-circuit condition. If the condition lasts for a long enough period as determined by the size of the RUN/SS capacitor, the controller will be shut down until the RUN/SS pin voltage is recycled. This built-in latchoff can be overridden by providing a current >5μA at a compliance of 5V to the RUN/SS pin. This current shortens the
The basic LTC3716 application circuit is shown in Figure 1 on the first page. External component selection begins with the selection of the inductors based on ripple current requirements and continues with the current sensing resistors using the calculated peak inductor current and/or maximum current limit. Next, the power MOSFETs, D1 and D2 are selected. The operating frequency and the inductor are chosen based mainly on the amount of ripple current. Finally, $C_{\text{IN}}$ is selected for its ability to handle the input ripple current (that PolyPhase™ operation minimizes) and $C_{\text{OUT}}$ is chosen with low enough ESR to meet the output ripple voltage and load step specifications (also minimized with PolyPhase). Current mode architecture provides inherent current sharing between output stages. The circuit shown in Figure 1 can be configured for operation up to an input voltage of 28V (limited by the external MOSFETs). Current mode control allows the ability to connect the two output stages to two different input power supply rails. A heavy output load can take some power from each input supply according to the selection of the $R_{\text{SENSE}}$ resistors.

$R_{\text{SENSE}}$ Selection For Output Current

$R_{\text{SENSE}}_{1,2}$ are chosen based on the required peak output current. The LTC3716 current comparator has a maximum threshold of 75mV/$R_{\text{SENSE}}$ and an input common mode range of SGND to 1.1(INTV$_{CC}$). The current comparator threshold sets the peak inductor current, yielding a maximum average output current $I_{\text{MAX}}$ equal to the peak value less half the peak-to-peak ripple current, $\Delta I_{L}$.

Assuming a common input power source for each output stage and allowing a margin for variations in the LTC3716 and external component values yields:

$$R_{\text{SENSE}} = 2(50\text{mV}/I_{\text{MAX}})$$

Operating Frequency

The LTC3716 uses a constant frequency, phase-lockable architecture with the frequency determined by an internal capacitor. This capacitor is charged by a fixed current plus an additional current which is proportional to the voltage applied to the PLLFLTR pin. Refer to Phase-Locked Loop and Frequency Synchronization for additional information.

A graph for the voltage applied to the PLLFLTR pin vs frequency is given in Figure 2. As the operating frequency is increased the gate charge losses will be higher, reducing efficiency (see Efficiency Considerations). The maximum switching frequency is approximately 310kHz.

Inductor Value Calculation and Output Ripple Current

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. So why would anyone ever choose to operate at lower frequencies with larger components? The answer is efficiency. A higher frequency generally results in lower efficiency because MOSFET gate charge and transition losses increase.
directly with frequency. In addition to this basic tradeoff, the effect of inductor value on ripple current and low current operation must also be considered. The PolyPhase approach reduces both input and output ripple currents while optimizing individual output stages to run at a lower fundamental frequency, enhancing efficiency.

The inductor value has a direct effect on ripple current. The inductor ripple current $\Delta I_L$ per individual section, $N$, decreases with higher inductance or frequency and increases with higher $V_{IN}$ or $V_{OUT}$:

$$\Delta I_L = \frac{V_{OUT}}{fL} \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where $f$ is the individual output stage operating frequency.

In a 2-phase converter, the net ripple current seen by the output capacitor is much smaller than the individual inductor ripple currents due to ripple cancellation. The details on how to calculate the net output ripple current can be found in Application Note 77.

Figure 3 shows the net ripple current seen by the output capacitors for 1- and 2-phase configurations. The output ripple current is plotted for a fixed output voltage as the duty factor is varied between 10% and 90% on the x-axis. The output ripple current is normalized against the inductor ripple current at zero duty factor. The graph can be used in place of tedious calculations, simplifying the design process.

Accepting larger values of $\Delta I_L$ allows the use of low inductances, but can result in higher output voltage ripple. A reasonable starting point for setting ripple current is $\Delta I_L = 0.4(I_{OUT})/2$, where $I_{OUT}$ is the total load current. Remember, the maximum $\Delta I_L$ occurs at the maximum input voltage. The individual inductor ripple currents are determined by the inductor, input and output voltages.

**Inductor Core Selection**

Once the values for L1 and L2 are known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite, molypermalloy, or Kool Mu cores. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on inductor type selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates “hard,” which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Molypermalloy (from Magnetics, Inc.) is a very good, low loss core material for toroids, but it is more expensive than ferrite. A reasonable compromise from the same manufacturer is Kool Mu. Toroids are very space efficient, especially when you can use several layers of wire. Because they lack a bobbin, mounting is more difficult. However, designs for surface mount are available which do not increase the height significantly.

**Power MOSFET, D1 and D2 Selection**

Two external power MOSFETs must be selected for each output stage with the LTC3716: one N-channel MOSFET for the top (main) switch, and one N-channel MOSFET for the bottom (synchronous) switch.

The peak-to-peak drive levels are set by the INTVCC voltage. This voltage is typically 5V during start-up.
APPLICATIONS INFORMATION

(see EXTVCC Pin Connection). Consequently, logic-level threshold MOSFETs must be used in most applications. The only exception is if low input voltage is expected (V_IN < 5V); then, sublogic-level threshold MOSFETs (V_GS(TH) < 1V) should be used. Pay close attention to the BV_DSS specification for the MOSFETs as well; most of the logic-level MOSFETs are limited to 30V or less.

Selection criteria for the power MOSFETs include the “ON” resistance R_DS(ON), reverse transfer capacitance C_RSS, input voltage and maximum output current. When the LTC3716 is operating in continuous mode the duty factors for the top and bottom MOSFETs of each output stage are given by:

Main Switch Duty Cycle \[ \frac{V_{OUT}}{V_{IN}} \]

Synchronous Switch Duty Cycle \[ \left( \frac{V_{IN} - V_{OUT}}{V_{IN}} \right) \]

The MOSFET power dissipations at maximum output current are given by:

\[ \begin{align*}
R_{MAIN} &= \frac{V_{OUT}}{V_{IN}} \left( \frac{I_{MAX}}{2} \right)^2 \left( 1 + \delta \right) R_{DS(ON)} + k \left( \frac{V_{IN}}{2} \right)^2 \left( \frac{I_{MAX}}{2} \right) C_{RSS}(f) \\
R_{SYNC} &= \frac{V_{IN} - V_{OUT}}{V_{IN}} \left( \frac{I_{MAX}}{2} \right)^2 \left( 1 + \delta \right) R_{DS(ON)}
\end{align*} \]

where \( \delta \) is the temperature dependency of R_DS(ON) and \( k \) is a constant inversely related to the gate drive current.

Both MOSFETs have \( i^2R \) losses but the topside N-channel equation includes an additional term for transition losses, which peak at the highest input voltage. For \( V_{IN} < 20V \) the high current efficiency generally improves with larger MOSFETs, while for \( V_{IN} > 20V \) the transition losses rapidly increase to the point that the use of a higher R_DS(ON) device with lower C_RSS actual provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage when the top switch duty factor is low or during a short-circuit when the synchronous switch is on close to 100% of the period.

The term \( (1 + \delta) \) is generally given for a MOSFET in the form of a normalized R_DS(ON) vs temperature curve, but \( \delta = 0.005/°C \) can be used as an approximation for low voltage MOSFETs. C_RSS is usually specified in the MOSFET characteristics. The constant \( k = 1.7 \) can be used to estimate the contributions of the two terms in the main switch dissipation equation.

The Schottky diodes, D1 and D2 shown in Figure 1 conduct during the dead-time between the conduction of the two large power MOSFETs. This helps prevent the body diode of the bottom MOSFET from turning on, storing charge during the dead-time, and requiring a reverse recovery period which would reduce efficiency. A 1A to 3A Schottky (depending on output current) diode is generally a good compromise for both regions of operation due to the relatively small average current. Larger diodes result in additional transition losses due to their larger junction capacitance.

C_IN and C_OUT Selection

In continuous mode, the source current of each top N-channel MOSFET is a square wave of duty cycle \( \frac{V_{OUT}}{V_{IN}} \). A low ESR input capacitor sized for the maximum RMS current must be used. The details of a closed form equation can be found in Application Note 77. Figure 4 shows the input capacitor ripple current for a 2-phase configuration with the output voltage fixed and input voltage varied. The input ripple current is normalized against the DC output current. The graph can be used in place of tedious calculations. The minimum input ripple current can be achieved when the input voltage is twice the output voltage.

In the graph of Figure 4, the 2-phase local maximum input RMS capacitor currents are reached when:

\[ \frac{V_{OUT}}{V_{IN}} = \frac{2k - 1}{4} \]

where \( k = 1, 2 \)

These worst-case conditions are commonly used for design because even significant deviations do not offer...
much relief. Note that capacitor manufacturer’s ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. Always consult the capacitor manufacturer if there is any question.

The output ripple varies with input voltage since $\Delta I_l$ is a function of input voltage. The output ripple will be less than 50mV at max $V_{IN}$ with $\Delta I_l = 0.4I_{OUT(MAX)}/2$ assuming:

- $C_{OUT}$ required $\text{ESR} < 4(R_{SENSE})$ and
- $C_{OUT} > 1/(16f)(R_{SENSE})$

The emergence of very low ESR capacitors in small, surface mount packages makes very physically small implementations possible. The ability to externally compensate the switching regulator loop using the $I_{TH}$ pin (OPTI-LOOP compensation) allows a much wider selection of output capacitor types. OPTI-LOOP compensation effectively removes constraints on output capacitor ESR. The impedance characteristics of each capacitor type are significantly different than an ideal capacitor and therefore require accurate modeling or bench evaluation during design.

Manufacturers such as Nichicon, United Chemicon and Sanyo should be considered for high performance through-hole capacitors. The OS-CON semiconductor dielectric capacitor available from Sanyo and the Panasonic SP surface mount types have the lowest (ESR)(size) product of any aluminum electrolytic at a somewhat higher price. An additional ceramic capacitor in parallel with OS-CON type capacitors is recommended to reduce the inductance effects.

In surface mount applications, multiple capacitors may have to be paralleled to meet the ESR or RMS current handling requirements of the application. Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. New special polymer surface mount capacitors offer very low ESR also but have much lower capacitive density per unit volume. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. Several excellent choices are the AVX TPS, AVX TPSV or the KEMET T510 series of surface mount tantalums, available in case heights ranging from 2mm to 4mm. Other capacitor types include Sanyo OS-CON, POSCAPs, Panasonic SP caps, Nichicon PL series and Sprague 595D series. Consult the manufacturer for other specific recommendations. A combination of capacitors will often result in maximizing performance and minimizing overall cost and size.
INTV\textsubscript{CC} Regulator

An internal P-channel low dropout regulator produces 5V at the INTV\textsubscript{CC} pin from the V\textsubscript{IN} supply pin. The INTV\textsubscript{CC} regulator powers the drivers and internal circuitry of the LTC3716. The INTV\textsubscript{CC} pin regulator can supply up to 50mA peak and must be bypassed to power ground with a minimum of 4.7\mu F tantalum or electrolytic capacitor. An additional 1\mu F ceramic capacitor placed very close to the IC is recommended due to the extremely high instantaneous currents required by the MOSFET gate drivers.

High input voltage applications in which large MOSFETs are being driven at high frequencies may cause the maximum junction temperature rating for the LTC3716 to be exceeded. The supply current is dominated by the gate charge supply current, in addition to the current drawn from the differential amplifier output. The gate charge is dependent on operating frequency as discussed in the Efficiency Considerations section. The supply current can either be supplied by the internal 5V regulator or via the EXTV\textsubscript{CC} pin. When the voltage applied to the EXTV\textsubscript{CC} pin is less than 4.7V, all of the INTV\textsubscript{CC} load current is supplied by the internal 5V linear regulator. Power dissipation for the IC is higher in this case by (I\textsubscript{IN})(V\textsubscript{IN} – INTV\textsubscript{CC}) and efficiency is lowered. The junction temperature can be estimated by using the equations given in Note 1 of the Electrical Characteristics. For example, the LTC3716 V\textsubscript{IN} current is limited to less than 24mA from a 24V supply:

\[
T_J = 70^\circ \text{C} + (24\text{mA})(24\text{V})(85^\circ \text{C/W}) = 119^\circ \text{C}
\]

Use of the EXTV\textsubscript{CC} pin reduces the junction temperature to:

\[
T_J = 70^\circ \text{C} + (24\text{mA})(5\text{V})(85^\circ \text{C/W}) = 80.2^\circ \text{C}
\]

The input supply current should be measured while the controller is operating in continuous mode at maximum V\textsubscript{IN} and the power dissipation calculated in order to prevent the maximum junction temperature from being exceeded.

EXTV\textsubscript{CC} Connection

The LTC3716 contains an internal P-channel MOSFET switch connected between the EXTV\textsubscript{CC} and INTV\textsubscript{CC} pins. When the voltage applied to EXTV\textsubscript{CC} rises above 4.7V, the internal regulator is turned off and an internal switch closes, connecting the EXTV\textsubscript{CC} pin to the INTV\textsubscript{CC} pin thereby supplying internal and MOSFET gate driving power to the IC. The switch remains closed as long as the voltage applied to EXTV\textsubscript{CC} remains above 4.5V. This allows the MOSFET driver and control power to be derived from the output during normal operation (4.7V < V\textsubscript{EXTVCC} < 7V) and from the internal regulator when the output is out of regulation (start-up, short-circuit). Do not apply greater than 7V to the EXTV\textsubscript{CC} pin and ensure that EXTV\textsubscript{CC} < V\textsubscript{IN} + 0.3V when using the application circuits shown. If an external voltage source is applied to the EXTV\textsubscript{CC} pin when the V\textsubscript{IN} supply is not present, a diode can be placed in series with the LTC3716’s V\textsubscript{IN} pin and a Schottky diode between the EXTV\textsubscript{CC} and the V\textsubscript{IN} pin, to prevent current from backfeeding V\textsubscript{IN}.

Significant efficiency gains can be realized by powering INTV\textsubscript{CC} from the output, since the V\textsubscript{IN} current resulting from the driver and control currents will be scaled by the ratio: (Duty Factor)/(Efficiency). For 5V regulators this means connecting the EXTV\textsubscript{CC} pin directly to V\textsubscript{OUT}. However, for 3.3V and other lower voltage regulators, additional supply circuitry is required to derive INTV\textsubscript{CC} power from the output.

The following list summarizes the four possible connections for EXTV\textsubscript{CC}:

1. EXTV\textsubscript{CC} left open (or grounded). This will cause INTV\textsubscript{CC} to be powered from the internal 5V regulator resulting in a significant efficiency penalty at high input voltages.
2. EXTV\textsubscript{CC} connected directly to V\textsubscript{OUT}. This is the normal connection for a 5V regulator and provides the highest efficiency.
3. EXTV\textsubscript{CC} connected to an external supply. If an external supply is available in the 5V to 7V range, it may be used to power EXTV\textsubscript{CC} providing it is compatible with the MOSFET gate drive requirements.
4. EXTV\textsubscript{CC} connected to an output-derived boost network. For 3.3V and other low voltage regulators, efficiency gains can still be realized by connecting EXTV\textsubscript{CC} to an output-derived voltage which has been boosted to greater than 4.7V but less than 7V. This can be done with either the inductive boost winding as shown in Figure 5a or the capacitive charge pump shown in Figure 5b. The charge pump has the advantage of simple magnetics.
Topside MOSFET Driver Supply (C_B, D_B) (Refer to Functional Diagram)

External bootstrap capacitors C_B1 and C_B2 connected to the BOOST1 and BOOST2 pins supply the gate drive voltages for the topside MOSFETs. Capacitor C_B in the Functional Diagram is charged through diode D_B from INTV_CC when the SW pin is low. When the topside MOSFET turns on, the driver places the C_B voltage across the gate-source of the desired MOSFET. This enhances the MOSFET and turns on the topside switch. The switch node voltage, SW, rises to V_IN and the BOOST pin rises to V_IN + V_INTVCC. The value of the boost capacitor C_B needs to be 30 to 100 times that of the total input capacitance of the topside MOSFET(s). The reverse breakdown of D_B must be greater than V_IN(MAX).

The final arbiter when defining the best gate drive amplitude level will be the input supply current. If a change is made that decreases input current, the efficiency has improved. If the input current does not change then the efficiency has not changed either.

Output Voltage

The LTC3716 has a true remote voltage sense capability. The sensing connections should be returned from the load back to the differential amplifier’s inputs through a common, tightly coupled pair of PC traces. The differential amplifier corrects for DC drops in both the power and ground paths. The differential amplifier output signal is divided down and compared with the internal precision 0.6V voltage reference by the error amplifier.

Output Voltage Programming

The output voltage is digitally programmed as defined in Table 1 using the VID0 to VID4 logic input pins. The VID logic inputs program a precision, 0.25% internal feedback resistive divider. The LTC3716 has an output voltage range of 0.6V to 1.75V in 25mV and 50mV steps.

Between the ATTENOUT pin and ground is a variable resistor, R1, whose value is controlled by the five VID input pins (VID0 to VID4). Another resistor, R2, between the ATTENIN and the ATTENOUT pins completes the resistive divider. The output voltage is thus set by the ratio of (R1 + R2) to R1.

Each VID digital input is pulled up by a 40k resistor in series with a diode from V_BIAS. Therefore, it must be grounded to get a digital low input, and can be either floated or connected to V_BIAS to get a digital high input. The series diode is used to prevent the digital inputs from being damaged or clamped if they are driven higher than V_BIAS. The digital inputs accept CMOS voltage levels.

V_BIAS is the supply voltage for the VID section. It is normally connected to INTV_CC but can be driven from other sources. If it is driven from another source, that source must be in the range of 2.7V to 5.5V and must be alive prior to enabling the LTC3716.
Soft-Start/Run Function

The RUN/SS pin provides three functions: 1) Run/Shut-down, 2) soft-start and 3) a defeatable short-circuit latchoff timer. Soft-start reduces the input power sources’ surge currents by gradually increasing the controller’s current limit $I_{TH(MAX)}$. The latchoff timer prevents very short, extreme load transients from tripping the overcurrent latch. A small pull-up current (>5μA) supplied to the RUN/SS pin will prevent the overcurrent latch from operating. The following explanation describes how the functions operate.

An internal 1.2μA current source charges up the soft-start capacitor, $C_{SS}$. When the voltage on RUN/SS reaches 1.5V, the controller is permitted to start operating. As the voltage on RUN/SS increases from 1.5V to 3.0V, the internal current limit is increased from 25mV/$R_{SENSE}$ to 75mV/$R_{SENSE}$. The output current limit ramps up slowly, taking an additional 1.4s/μF to reach full current. The output current thus ramps up slowly, reducing the starting surge current required from the input power supply. If RUN/SS has been pulled all the way to ground there is a delay before starting of approximately:

$$t_{DELAY} = \frac{1.5V}{1.2\mu A} C_{SS} = (1.25s/\mu F) C_{SS}$$

The time for the output current to ramp up is then:

$$t_{RAMP} = \frac{3V - 1.5V}{1.2\mu A} C_{SS} = (1.25s/\mu F) C_{SS}$$

By pulling the RUN/SS pin below 0.8V the LTC3716 is put into low current shutdown ($I_Q < 40\mu A$). The RUN/SS pins can be driven directly from logic as shown in Figure 6. Diode D1 in Figure 6 reduces the start delay but allows $C_{SS}$ to ramp up slowly providing the soft-start function. The RUN/SS pin has an internal 6V zener clamp (see Functional Diagram).

### Table 1. VID Output Voltage Programming

<table>
<thead>
<tr>
<th>VID4</th>
<th>VID3</th>
<th>VID2</th>
<th>VID1</th>
<th>VID0</th>
<th>LTC3716</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1.750V</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1.700V</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1.650V</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1.600V</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1.550V</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1.500V</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1.450V</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1.400V</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1.350V</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1.300V</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1.250V</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1.200V</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1.150V</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1.100V</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1.050V</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1.000V</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0.975V</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0.950V</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0.925V</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0.900V</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0.875V</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0.850V</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0.825V</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0.800V</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0.775V</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0.750V</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0.725V</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0.700V</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0.675V</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0.650V</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0.625V</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0.600V</td>
</tr>
</tbody>
</table>
APPLICATIONS INFORMATION

Fault Conditions: Overcurrent Latchoff

The RUN/SS pin also provides the ability to latch off the controllers when an overcurrent condition is detected. The RUN/SS capacitor, \( \text{CSS} \), is used initially to limit the inrush current of both controllers. After the controllers have been started and been given adequate time to charge up the output capacitors and provide full load current, the RUN/SS capacitor is used for a short-circuit timer. If the output voltage falls to less than 70% of its nominal value after \( \text{CSS} \) reaches 4.1V, \( \text{CSS} \) begins discharging on the assumption that the output is in an overcurrent condition. If the condition lasts for a long enough period as determined by the size of the \( \text{CSS} \), the controller will be shut down until the RUN/SS pin voltage is recycled. If the overload occurs during start-up, the time can be approximated by:

\[
\text{t}_{\text{LO1}} = \left( \frac{\text{CSS} \times 0.6V}{1.2 \mu A} \right) = 5 \times 10^5 \text{ (CSS)}
\]

If the overload occurs after start-up, the voltage on \( \text{CSS} \) will continue charging and will provide additional time before latching off:

\[
\text{t}_{\text{LO2}} = \left( \frac{\text{CSS} \times 3V}{1.2 \mu A} \right) = 2.5 \times 10^6 \text{ (CSS)}
\]

This built-in overcurrent latchoff can be overridden by providing a pull-up resistor, \( \text{RSS} \), to the RUN/SS pin as shown in Figure 6. This resistance shortens the soft-start period and prevents the discharge of the RUN/SS capacitor during a severe overcurrent and/or short-circuit condition. When deriving the 5μA current from \( \text{VIN} \) as in the figure, current latchoff is always defeated. The diode connecting this pull-up resistor to \( \text{INTVCC} \), as in Figure 6, eliminates any extra supply current during shutdown while eliminating the \( \text{INTVCC} \) loading from preventing controller start-up.

Why should you defeat current latchoff? During the prototyping stage of a design, there may be a problem with noise pickup or poor layout causing the protection circuit to latch off the controller. Defeating this feature allows troubleshooting of the circuit and PC layout. The internal short-circuit and foldback current limiting still remains active, thereby protecting the power supply system from failure. A decision can be made after the design is complete whether to rely solely on foldback current limiting or to enable the latchoff feature by removing the pull-up resistor.

The value of the soft-start capacitor \( \text{CSS} \) may need to be scaled with output voltage, output capacitance and load current characteristics. The minimum soft-start capacitance is given by:

\[
\text{CSS} > (\text{COUT} \times \text{VOUT} \times 10^{-4}) \times \text{RSENSE}
\]

The minimum recommended soft-start capacitor of \( \text{CSS} = 0.1 \mu F \) will be sufficient for most applications.

Phase-Locked Loop and Frequency Synchronization

The LTC3716 has a phase-locked loop comprised of an internal voltage controlled oscillator and phase detector. This allows the top MOSFET turn-on to be locked to the rising edge of an external source. The frequency range of the voltage controlled oscillator is ±50% around the center frequency \( f_0 \). A voltage applied to the PLLFLTR pin of 1.2V corresponds to a frequency of approximately 220kHz. The nominal operating frequency range of the LTC3716 is 140kHz to 310kHz.

The phase detector used is an edge sensitive digital type which provides zero degrees phase shift between the external and internal oscillators. This type of phase detector will not lock up on input frequencies close to the harmonics of the VCO center frequency. The PLL hold-in range, \( \Delta f_H \), is equal to the capture range, \( \Delta f_C \):

\[
\Delta f_H = \Delta f_C = \pm 0.5 f_0 \text{ (150kHz-300kHz)}
\]

The output of the phase detector is a complementary pair of current sources charging or discharging the external filter network on the PLLFLTR pin. A simplified block diagram is shown in Figure 7.

Figure 7. Phase-Locked Loop Block Diagram
If the external frequency \( f_{PLLIN} \) is greater than the oscillator frequency \( f_{OSC} \), current is sourced continuously, pulling up the PLLFLTR pin. When the external frequency is less than \( f_{OSC} \), current is sunk continuously, pulling down the PLLFLTR pin. If the external and internal frequencies are the same but exhibit a phase difference, the current sources turn on for an amount of time corresponding to the phase difference. Thus the voltage on the PLLFLTR pin is adjusted until the phase and frequency of the external and internal oscillators are identical. At this stable operating point the phase comparator output is open and the filter capacitor \( C_{LP} \) holds the voltage. The LTC3716 PLLIN pin must be driven from a low impedance source such as a logic gate located close to the pin.

The loop filter components \( (C_{LP}, R_{LP}) \) smooth out the current pulses from the phase detector and provide a stable input to the voltage controlled oscillator. The filter components \( C_{LP} \) and \( R_{LP} \) determine how fast the loop acquires lock. Typically \( R_{LP} = 10k \) and \( C_{LP} \) is \( 0.01 \mu F \) to \( 0.1 \mu F \).

### Minimum On-Time Considerations

Minimum on-time, \( t_{ON(MIN)} \), is the smallest time duration that the LTC3716 is capable of turning on the top MOSFET. It is determined by internal timing delays and the gate charge required to turn on the top MOSFET. Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure that:

\[
t_{ON(MIN)} < \frac{V_{OUT}}{V_{IN}(f)}
\]

If the duty cycle falls below what can be accommodated by the minimum on-time, the LTC3716 will begin to skip cycles resulting in variable frequency operation. The output voltage will continue to be regulated, but the ripple current and ripple voltage will increase.

The minimum on-time for the LTC3716 is generally less than 200ns. However, as the peak sense voltage decreases, the minimum on-time gradually increases. This is of particular concern in forced continuous applications with low ripple current at light loads. If the duty cycle drops below the minimum on-time limit in this situation, a significant amount of cycle skipping can occur with correspondingly larger ripple current and voltage ripple.

If an application can operate close to the minimum on-time limit, an inductor must be chosen that has a low enough inductance to provide sufficient ripple amplitude to meet the minimum on-time requirement. **As a general rule, keep the inductor ripple current of each phase equal to or greater than 15% of \( I_{OUT(MAX)} \) at \( V_{IN(MAX)} \).**

### FCB Pin Operation

The FCB pin can be used to regulate a secondary winding or as a logic level input. Continuous operation is forced when the FCB pin drops below 0.6V. During continuous mode, current flows continuously in the transformer primary. The secondary winding(s) supply current only when the bottom, synchronous switch is on. When primary load currents are low and/or the \( V_{IN}/V_{OUT} \) ratio is low, the synchronous switch may not be on for a sufficient amount of time to transfer power from the output capacitor to the secondary load. Forced continuous operation will support secondary windings providing there is sufficient synchronous switch duty factor. Thus, the FCB input pin removes the requirement that power must be drawn from the inductor primary in order to extract power from the auxiliary winding(s). With the loop in continuous mode, the auxiliary output(s) may nominally be loaded without regard to the primary output load.

The secondary output voltage \( V_{SEC} \) is normally set as shown in Figure 5a by the turns ratio \( N \) of the transformer:

\[
V_{SEC} = (N + 1) V_{OUT}
\]

However, if the controller goes into Burst Mode operation and halts switching due to a light primary load current, then \( V_{SEC} \) will droop. An external resistive divider from \( V_{SEC} \) to the FCB pin sets a minimum voltage \( V_{SEC(MIN)} \):

\[
V_{SEC(MIN)} = 0.6V \left( 1 + \frac{R_6}{R_5} \right)
\]

where \( R_5 \) and \( R_6 \) are shown in Figure 5a.

If \( V_{SEC} \) drops below this level, the FCB voltage forces temporary continuous switching operation until \( V_{SEC} \) is again above its minimum.
APPLICATONS INFORMATION

In order to prevent erratic operation if no external connections are made to the FCB pin, the FCB pin has a 0.18\(\mu\)A internal current source pulling the pin high. Include this current when choosing resistor values R5 and R6.

The following table summarizes the possible states available on the FCB pin:

<table>
<thead>
<tr>
<th>FCB Pin</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>0V to 0.55V</td>
<td>Forced Continuous (Current Reversal Allowed—Burst Inhibited)</td>
</tr>
<tr>
<td>0.65V &lt; V_{FCB} &lt; 4.3V (typ)</td>
<td>Minimum Peak Current Induces Burst Mode Operation No Current Reversal Allowed</td>
</tr>
<tr>
<td>Feedback Resistors</td>
<td>Regulating a Secondary Winding</td>
</tr>
<tr>
<td>&gt;4.8V</td>
<td>Burst Mode Operation Disallowed Constant Frequency Mode Enabled No Current Reversal Allowed No Minimum Peak Current</td>
</tr>
</tbody>
</table>

Active Voltage Positioning

Active voltage positioning can be used to minimize peak-to-peak output voltage excursion under worst-case transient loading conditions. The open-loop DC gain of the control loop is reduced depending upon the maximum load step specifications. Active voltage positioning can easily be added to the LTC3716 by loading the I_{TH} pin with a resistive divider having a Thevenin equivalent voltage source equal to the midpoint operating voltage of the error amplifier, or 1.2V (see Figure 8).

Figure 8. Active Voltage Positioning Applied to the LTC3716

The resistive load reduces the DC loop gain while maintaining the linear control range of the error amplifier. The worst-case peak-to-peak output voltage deviation due to transient loading can theoretically be reduced to half or alternatively the amount of output capacitance can be reduced for a particular application. A complete explanation is included in Design Solutions 10 or the LTC1736 data sheet. (See www.linear-tech.com)

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

\[
\text{%Efficiency} = 100\% - (L1 + L2 + L3 + \ldots)
\]

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC3716 circuits: 1) \(I^2R\) losses, 2) Topside MOSFET transition losses, 3) INTV\(_{CC}\) regulator current and 4) LTC3716 \(V_{IN}\) current (including loading on the differential amplifier output).

1) \(I^2R\) losses are predicted from the DC resistances of the fuse (if used), MOSFET, inductor, current sense resistor, and input and output capacitor ESR. In continuous mode the average output current flows through L and R_{SENSE}, but is “chopped” between the topside MOSFET and the synchronous MOSFET. If the two MOSFETs have approximately the same \(R_{DS(ON)}\), then the resistance of one MOSFET can simply be summed with the resistances of L, R_{SENSE} and ESR to obtain \(I^2R\) losses. For example, if each \(R_{DS(ON)} = 10m\Omega\), \(R_L = 10m\Omega\), and \(R_{SENSE} = 5m\Omega\), then the total resistance is 25m\Omega. This results in losses ranging from 2% to 8% as the output current increases from 3A to 15A per output stage for a 5V output, or a 3% to 12% loss per output stage for a 3.3V output. Efficiency varies as the inverse square of \(V_{OUT}\) for the same external components and output power level. The combined effects of increasingly lower output voltages and higher currents required by high performance digital systems is not doubling but quadrupling the importance of loss terms in the switching regulator system!
2) Transition losses apply only to the topside MOSFET(s), and are significant only when operating at high input voltages (typically 12V or greater). Transition losses can be estimated from:

\[
\text{Transition Loss} = (1.7)V_{\text{IN}}^2 \left( \frac{I_{\text{O(MAX)}}}{2} \right) C_{\text{RSS}} f
\]

3) INTVCC current is the sum of the MOSFET driver and control currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from INTVCC to ground. The resulting dQ/dt is a current out of INTVCC that is typically much larger than the control circuit current. In continuous mode, \( I_{\text{GATECHG}} = (Q_T + Q_B) \), where \( Q_T \) and \( Q_B \) are the gate charges of the topside and bottom side MOSFETs.

Supplying INTVCC power through the EXTVCC switch input from an output-derived source will scale the V IN current required for the driver and control circuits by the ratio (Duty Factor)/(Efficiency). For example, in a 20V to 5V application, 10mA of INTVCC current results in approximately 3mA of V IN current. This reduces the mid-current loss from 10% or more (if the driver was powered directly from V IN) to only a few percent.

4) The V IN current has two components: the first is the DC supply current given in the Electrical Characteristics table, which excludes MOSFET driver and control currents; the second is the current drawn from the differential amplifier output. V IN current typically results in a small (<0.1%) loss.

Other “hidden” losses such as copper trace and internal battery resistances can account for an additional 5% to 10% efficiency degradation in portable systems. It is very important to include these “system” level losses in the design of a system. The internal battery and input fuse resistance losses can be minimized by making sure that \( C_{\text{IN}} \) has adequate charge storage and a very low ESR at the switching frequency. A 50W supply will typically require a minimum of 200\( \mu \)F to 300\( \mu \)F of output capacitance having a maximum of 10m\( \Omega \) to 20m\( \Omega \) of ESR. The LTC3716 2-phase architecture typically halves the input and output capacitance requirements over competing solutions. Other losses including Schottky conduction losses during dead-time and inductor core losses generally account for less than 2% total additional loss.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, \( V_{\text{OUT}} \) shifts by an amount equal to \( \Delta I_{\text{LOAD}}(\text{ESR}) \), where ESR is the effective series resistance of \( C_{\text{OUT}} \). The resulting change in \( V_{\text{OUT}} \) also begins to charge or discharge \( C_{\text{OUT}} \) generating the feedback error signal that forces the regulator to adapt to the current change and return \( V_{\text{OUT}} \) to its steady-state value. During this recovery time \( V_{\text{OUT}} \) can be monitored for excessive overshoot or ringing, which would indicate a stability problem. The availability of the \( I_{\text{TH}} \) pin not only allows optimization of control loop behavior but also provides a DC coupled and AC filtered closed loop response test point. The DC step, rise time, and settling at this test point truly reflects the closed loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin. The \( I_{\text{TH}} \) external components shown in the Figure 1 circuit will provide an adequate starting point for most applications.

The \( I_{\text{TH}} \) series \( R_{\text{C}}-C_{\text{C}} \) filter sets the dominant pole-zero loop compensation. The values can be modified slightly (from 0.2 to 5 times their suggested values) to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be decided upon first because the various types and values determine the loop gain and phase. An output current pulse of 20% to 80% of full-load current having a rise time of <2\( \mu \)s will produce output voltage and \( I_{\text{TH}} \) pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop. The initial output voltage step resulting from the step change in output current may not be within the bandwidth of the feedback loop, so this signal cannot be used to determine phase margin. This is why it is better to look at the Ith pin signal which is in the feedback...
APPLICATIONS INFORMATION

loop and is the filtered and compensated control loop response. The gain of the loop will be increased by increasing $R_C$ and the bandwidth of the loop will be increased by decreasing $C_C$. If $R_C$ is increased by the same factor that $C_C$ is decreased, the zero frequency will be kept the same, thereby keeping the phase the same in the most critical frequency range of the feedback loop. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance.

Automotive Considerations: Plugging into the Cigarette Lighter

As battery-powered devices go mobile, there is a natural interest in plugging into the cigarette lighter in order to conserve or even recharge battery packs during operation. But before you connect, be advised: you are plugging into the supply from hell. The main battery line in an automobile is the source of a number of nasty potential transients, including load-dump, reverse-battery and double-battery.

Load-dump is the result of a loose battery cable. When the cable breaks connection, the field collapse in the alternator can cause a positive spike as high as 60V which takes several hundred milliseconds to decay. Reverse-battery is just what it says, while double-battery is a consequence of tow truck operators finding that a 24V jump start cranks cold engines faster than 12V.

The network shown in Figure 9 is the most straightforward approach to protect a DC/DC converter from the ravages of an automotive power line. The series diode prevents current from flowing during reverse-battery, while the transient suppressor clamps the input voltage during load-dump. Note that the transient suppressor should not conduct during double-battery operation, but must still clamp the input voltage below breakdown of the converter. Although the LT3716 has a maximum input voltage of 36V, most applications will be limited to 30V by the MOSFET BV$_{DSS}$:

**Design Example**

As a design example, assume $V_{IN} = 5$V (nominal), $V_{IN} = 5.5$V (max), $V_{OUT} = 1.2$V, $I_{MAX} = 20$A, $T_A = 70°C$ and $f = 300$kHz.

The inductance value is chosen first based on a 30% ripple current assumption. The highest value of ripple current occurs at the maximum input voltage. Tie the FREQSET pin to the INTV$_{CC}$ pin for 300kHz operation. The minimum inductance for 30% ripple current is:

$$L \geq \frac{V_{OUT}}{f(\Delta L)} \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

$$\geq \frac{1.2V}{(300kHz)(30\%)(10A)} \left(1 - \frac{1.2V}{5.5V}\right)$$

$$\geq 1.04\mu H$$

A 1$\mu$H inductor will produce 31% ripple current. The peak inductor current will be the maximum DC value plus one half the ripple current, or 11.5A. The minimum on-time occurs at maximum $V_{IN}$:

$$t_{ON\,(MIN)} = \frac{V_{OUT}}{V_{IN} f} = \frac{1.2V}{(5.5V)(300kHz)} = 0.73\mu s$$

The $R_{SENSE}$ resistors value can be calculated by using the maximum current sense voltage specification with some accommodation for tolerances:

$$R_{SENSE} = \frac{50mV}{11.5A} \approx 0.004\Omega$$

The power dissipation on the topside MOSFET can be easily estimated. Using a Siliconix Si4420DY for example; $R_{DS\,(ON)} = 0.013\Omega$, $C_{RSS} = 300pF$. At maximum input voltage with $T_J$ (estimated) = 110°C at an elevated ambient temperature:
The worst-case power dissipated by the synchronous MOSFET under normal operating conditions at elevated ambient temperature and estimated 50°C junction temperature rise is:

\[ P_{\text{SYNC}} = \frac{5.5V - 1.2V}{5.5V} \cdot 2(10A)^2(1.48)(0.013\Omega) = 1.5W \]

A short-circuit to ground will result in a folded back current of about:

\[ I_{\text{SC}} = \frac{25mV}{0.004\Omega} + \frac{1}{2} \left[ \frac{200ns(5.5V)}{1\mu\text{H}} \right] = 6.8A \]

The worst-case power dissipated by the synchronous MOSFET under short-circuit conditions at elevated ambient temperature and estimated 50°C junction temperature rise is:

\[ P_{\text{SYNC}} = \frac{5.5V - 1.2V}{5.5V} \cdot (6.8A)^2(1.48)(0.013\Omega) = 696mW \]

which is less than normal, full-load conditions. Incidentally, since the load no longer dissipates power in the shorted condition, total system power dissipation is decreased by over 99%.

The duty factor for this application is:

\[ \text{DF} = \frac{V_O}{V_{\text{IN}}} = \frac{1.2V}{5V} = 0.24 \]

Using Figure 4, the RMS ripple current will be:

\[ I_{\text{IN RMS}} = (20A)(0.25) = 5A_{\text{RMS}} \]

An input capacitor(s) with a 5A_{\text{RMS}} ripple current rating is required.

The output capacitor ripple current is calculated by using the inductor ripple already calculated for each inductor and multiplying by the factor obtained from Figure 3 along with the calculated duty factor. The output ripple in continuous mode will be highest at the maximum input voltage since the duty factor is <50%. The maximum output current ripple is:

\[ \Delta I_{\text{OUT}} = \frac{\Delta V_{\text{OUT}}}{\text{fL}}(0.5) \text{ at } 24\% \text{ DF} \]

\[ \Delta I_{\text{OUT MAX}} = \frac{1.2V}{(300kHz)(1.0\mu\text{H})} \cdot 0.5 \]

\[ V_{\text{OUT RIPPLE}} = 20m\Omega(2A_{\text{P-P}}) = 40m\text{V}_{\text{P-P}} \]

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3716. Check the following in your layout:

1) Are the signal and power grounds separate? The signal ground traces should return to Pin 9 first. Connect Pin 9 to Pin 28 through a wide and straight trace. Then the signal ground joins the power ground plane beside Pin 28. It is recommended that the Pin 28 return to the (–) plates of C_{\text{IN}}.

2) Does the LTC3716 V_{\text{OS+}} pin connect to the point of load? Does the LTC3716 V_{\text{OS–}} pin connect to the load return?

Figure 10. Proper Current Sense Connections
APPLICATIONS INFORMATION

3) Are the SENSE\(^-\) and SENSE\(^+\) leads routed together with minimum PC trace spacing? The filter capacitors between SENSE\(^+\) and SENSE\(^-\) pin pairs should be as close as possible to the LTC3716. Ensure accurate current sensing with Kelvin connections at the current sense resistor. See Figure 10.

4) Does the (+) plate of C\(_{IN}\) connect to the drains of the topside MOSFETs as closely as possible? This capacitor provides the AC current to the MOSFETs. Keep the input current path formed by the input capacitor, top and bottom MOSFETs, and the Schottky diode on the same side of the PC board in a tight loop to minimize conducted and radiated EMI.

5) Is the INTV\(_{CC}\) 1\(\mu\)F ceramic decoupling capacitor connected closely between INTV\(_{CC}\) and the PGND pin? This capacitor carries the MOSFET driver peak currents. A small value is recommended to allow placement immediately adjacent to the IC.

6) Keep the switching nodes, SW1 (SW2), away from sensitive small-signal nodes. Ideally the switch nodes should be placed at the furthest point from the LTC3716.

7) Use a low impedance source such as a logic gate to drive the PLLIN pin and keep the lead as short as possible.

The diagram in Figure 11 illustrates all branch currents in a 2-phase switching regulator. It becomes very clear after studying the current waveforms why it is critical to keep the high-switching-current paths to a small physical size. High electric and magnetic fields will radiate from these “loops” just as radio stations transmit signals. The output capacitor ground should return to the negative terminal of the input capacitor and not share a common ground path with any switched current paths. The left half of the circuit gives rise to the “noise” generated by a switching regulator. The ground terminations of the synchronous MOSFETs and Schottky diodes should return to the negative plate(s).

Figure 11. Instantaneous Current Path Flow in a Multiple Phase Switching Regulator
of the input capacitor(s) with a short isolated PC trace since very high switched currents are present. A separate isolated path from the negative plate(s) of the input capacitor(s) should be used to tie in the IC power ground pin (PGND) and the signal ground pin (SGND). This technique keeps inherent signals generated by high current pulses from taking alternate current paths that have finite impedances during the total period of the switching regulator. External OPTI-LOOP compensation allows overcompensation for PC layouts which are not optimized but this is not the recommended design procedure.

**Simplified Visual Explanation of How a 2-Phase Controller Reduces Both Input and Output RMS Ripple Current**

A multiphase power supply significantly reduces the amount of ripple current in both the input and output capacitors. The RMS input ripple current is divided by, and the effective ripple frequency is multiplied up by the number of phases used (assuming that the input voltage is greater than the number of phases used times the output voltage). The output ripple amplitude is also reduced by, and the effective ripple frequency is increased by the number of phases used. Figure 12 graphically illustrates the principle.

The worst-case RMS ripple current for a single stage design peaks at an input voltage of twice the output voltage. The worst-case RMS ripple current for a two stage design results in peak outputs of 1/4 and 3/4 of input voltage. When the RMS current is calculated, higher effective duty factor results and the peak current levels are divided as long as the currents in each stage are balanced. Refer to Application Note 19 for a detailed description of how to calculate RMS current for the single stage switching regulator. Figures 3 and 4 illustrate how the input and output currents are reduced by using an additional phase. The input current peaks drop in half and the frequency is doubled for this 2-phase converter. The input capacity requirement is thus reduced theoretically by a factor of four! Ceramic input capacitors with their unbeatably low ESR characteristics can be used.

Figure 4 illustrates the RMS input current drawn from the input capacitance vs the duty cycle as determined by the ratio of input and output voltage. The peak input RMS current level of the single phase system is reduced by 50% in a 2-phase solution due to the current splitting between the two stages.

An interesting result of the 2-phase solution is that the $V_{IN}$ which produces worst-case ripple current for the input capacitor, $V_{OUT} = V_{IN}/2$, in the single phase design produces zero input current ripple in the 2-phase design.

The output ripple current is reduced significantly when compared to the single phase solution using the same inductance value because the $V_{OUT}/L$ discharge current term from the stage that has its bottom MOSFET on subtracts current from the $(V_{IN} - V_{OUT})/L$ charging current resulting from the stage which has its top MOSFET on. The output ripple current is:

$$\Delta I_{RIPPLE} = \frac{2V_{OUT}}{fL} \left[ \frac{1 - 2D(1-D)}{|1 - 2D| + 1} \right]$$

where $D$ is duty factor.

The input and output ripple frequency is increased by the number of stages used, reducing the output capacity requirements. When $V_{IN}$ is approximately equal to $2(V_{OUT})$ as illustrated in Figures 3 and 4, very low input and output ripple currents result.
Figure 13 shows a typical application using LTC3716 to power the mobile CPU core. The input can vary from 7V to 24V, the output voltage can be programmed from 0.6V to 1.75V with a maximum current of 30A. This power supply receives three input signals to generate different output voltage offsets based on the operation conditions. With the AMPMD pin of LTC3716 tied to INTVCC, the LTC3716 provides a regular operational amplifier to implement these offsets. When GMUXSEL is low, the output voltage is offset –1.2% from the VID command voltage. The offset equals Ra/Rb. When DPSLP# is low, the output voltage is decreased by approximately 4%. This offset can be increased by decreasing Rc and will be disabled when the DPRSLPVR signal is high. The optional filtering circuit (Q1 and Q2) is used to mask the PWRGOOD during the VID transitions.
### RELATED PARTS

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>LTC1438/LTC1439</td>
<td>Dual High Efficiency Low Noise Synchronous Step-Down Switching Regulators</td>
<td>POR, Auxiliary Regulator</td>
</tr>
<tr>
<td>LTC1438-ADJ</td>
<td>Dual Synchronous Controller with Auxiliary Regulator</td>
<td>POR, External Feedback Divider</td>
</tr>
<tr>
<td>LTC1538-AUX</td>
<td>Dual High Efficiency Low Noise Synchronous Step-Down Switching Regulator</td>
<td>Auxiliary Regulator, 5V Standby</td>
</tr>
<tr>
<td>LTC1539</td>
<td>Dual High Efficiency Low Noise Synchronous Step-Down Switching Regulator</td>
<td>5V Standby, POR, Low Battery, Aux Regulator</td>
</tr>
<tr>
<td>LTC1436A-PLL</td>
<td>High Efficiency Low Noise Synchronous Step-Down Switching Regulator</td>
<td>Adaptive Power™ Mode, 24-Pin SSOP</td>
</tr>
<tr>
<td>LTC1628/LTC1628-PG</td>
<td>Dual High Efficiency, 2-Phase Synchronous Step-Down Switching Regulator</td>
<td>Constant Frequency, Standby, 5V and 3.3V LDOs</td>
</tr>
<tr>
<td>LTC1629/LTC1629-PG</td>
<td>PolyPhase High Efficiency Controller</td>
<td>Expandable Up to 12 Phases, G-28, Up to 120A</td>
</tr>
<tr>
<td>LTC1929/LTC1929-PG</td>
<td>2-Phase High Efficiency Controller</td>
<td>Adjustable Output up to 40A, G-28</td>
</tr>
<tr>
<td>LTC1702/LTC1703</td>
<td>Dual High Efficiency, 2-Phase Synchronous Step-Down Switching Regulator</td>
<td>500kHz, 25MHz GBW</td>
</tr>
<tr>
<td>LTC1708-PG</td>
<td>Dual High Efficiency, 2-Phase Synchronous Step-Down Switching Regulator</td>
<td>1.3V ≤ V_{OUT} ≤ 3.5V, Current Mode Ensures Accurate Current Sharing, 3.5V ≤ V_{IN} ≤ 36V</td>
</tr>
<tr>
<td>LTC1709-7</td>
<td>2-Phase High Efficiency Controller with 5-Bit Mobile VID and Power Good Indication (0.9V ≤ V_{OUT} ≤ 2V)</td>
<td>Burst Mode Operation and Cycle Skip Low Current Modes, 3.5V ≤ V_{IN} ≤ 36V</td>
</tr>
<tr>
<td>LTC1709-8/LTC1709-9</td>
<td>2-Phase High Efficiency Controller with 5-Bit VID and Power Good Indication</td>
<td>VID Tables VRM 8.4 and VRM9.0</td>
</tr>
<tr>
<td>LTC1735</td>
<td>High Efficiency Synchronous Step-Down Controller</td>
<td>Burst Mode Operation, 16-Pin Narrow SSOP, Fault Protection, 3.5V ≤ V_{IN} ≤ 36V</td>
</tr>
<tr>
<td>LTC1736</td>
<td>High Efficiency Synchronous Step-Down Controller with 5-Bit VID</td>
<td>Output Fault Protection, Power Good, GN-24, 3.5V ≤ V_{IN} ≤ 36V, 0.925V ≤ V_{OUT} ≤ 2V</td>
</tr>
<tr>
<td>LTC1778</td>
<td>No R_{SENSE}™ Synchronous Current Mode Step-Down Controller</td>
<td>No Sense Resistor Required, 4V ≤ V_{IN} ≤ 36V, 0.8V ≤ V_{IN} ≤ V_{IN} - GN16</td>
</tr>
</tbody>
</table>

Adaptive Power and No R_{SENSE} are trademarks of Linear Technology Corporation.