The LTC3704 is a wide input range, current mode, positive-to-negative DC/DC controller that drives an N-channel power MOSFET and requires very few external components. Intended for low to high power applications, it eliminates the need for a current sense resistor by utilizing the power MOSFET’s on-resistance, thereby maximizing efficiency.

The IC’s operating frequency can be set with an external resistor over a 50kHz to 1MHz range, and can be synchronized to an external clock using the MODE/SYNC pin. Burst Mode operation at light loads, a low minimum operating supply voltage of 2.5V and a low shutdown quiescent current of 10μA make the LTC3704 ideally suited for battery-operated systems.

For applications requiring constant frequency operation, the Burst Mode operation feature can be defeated using the MODE/SYNC pin. Higher than 36V switch voltage applications are possible with the LTC3704 by connecting the SENSE pin to a resistor in the source of the power MOSFET.

The LTC3704 is available in the 10-lead MSOP package.

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### ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ C$.

**$V_{IN} = V_{INTVCC} = 5V$, $V_{RUN} = 1.5V$, $R_T = 80k$, $V_{MODE/SYNC} = 0V$, unless otherwise specified.**

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td><strong>Main Control Loop</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IN(MIN)}$</td>
<td>Minimum Input Voltage</td>
<td></td>
<td>2.5</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_Q$</td>
<td>Input Voltage Supply Current</td>
<td>Continuous Mode</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Burst Mode Operation, No Load</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Shutdown Mode</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_{RUN^+}$</td>
<td>Rising RUN Input Threshold Voltage</td>
<td>1.348</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$V_{RUN^-}$</td>
<td>Falling RUN Input Threshold Voltage</td>
<td>1.223</td>
<td>1.248</td>
<td>1.273</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$V_{RUN(HYST)}$</td>
<td>RUN Pin Input Threshold Hysteresian</td>
<td>50</td>
<td>100</td>
<td>150</td>
<td>mV</td>
</tr>
<tr>
<td>$I_{RUN}$</td>
<td>RUN Input Current</td>
<td></td>
<td></td>
<td>1</td>
<td>100</td>
<td>nA</td>
</tr>
<tr>
<td>$V_{NFB}$</td>
<td>Negative Feedback Voltage</td>
<td>$V_{ITH} = 0.4V$ (Note 5)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{ITH} = 0.4V$ (Note 5)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{ITH} = 0.4V$ (I-Grade) (Notes 2 and 5)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{NFB}$</td>
<td>NFB Pin Input Current</td>
<td></td>
<td>7.5</td>
<td>15</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>$\Delta V_{NFB}$</td>
<td>Line Regulation</td>
<td>$2.5V \leq V_{IN} \leq 30V$</td>
<td>0.002</td>
<td>0.02</td>
<td></td>
<td>%/V</td>
</tr>
<tr>
<td>$\Delta V_{ITH}$</td>
<td>Load Regulation</td>
<td>$V_{MODE/SYNC} = 0V, V_{ITH} = 0.5V$ to 0.90V (Note 5)</td>
<td></td>
<td></td>
<td>-1</td>
<td>-0.1</td>
</tr>
<tr>
<td>$g_{m}$</td>
<td>Error Amplifier Transconductance</td>
<td>$I_{TH}$ Pin Load $\approx 5\mu A$ (Note 5)</td>
<td>650</td>
<td></td>
<td></td>
<td>μmho</td>
</tr>
<tr>
<td>$V_{ITH(BURST)}$</td>
<td>Burst Mode Operation $I_{TH}$ Pin Voltage</td>
<td>Falling $I_{TH}$ Voltage</td>
<td>0.17</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{SENSE(MAX)}$</td>
<td>Maximum Current Sense Input Threshold</td>
<td>Duty Cycle $&lt; 20%$</td>
<td>120</td>
<td>150</td>
<td>180</td>
<td>mV</td>
</tr>
<tr>
<td>$I_{SENSE(ON)}$</td>
<td>SENSE Pin Current (GATE High)</td>
<td>$V_{SENSE} = 0V$</td>
<td>40</td>
<td>75</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>$I_{SENSE(OFF)}$</td>
<td>SENSE Pin Current (GATE Low)</td>
<td>$V_{SENSE} = 30V$</td>
<td>0.1</td>
<td>5</td>
<td></td>
<td>μA</td>
</tr>
</tbody>
</table>
ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. $V_{IN} = V_{INTVCC} = 5V$, $V_{RUN} = 1.5V$, $R_{FREQ} = 80k$, $V_{MODE/SYNC} = 0V$, unless otherwise specified.

### SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS
--- | --- | --- | --- | --- | --- | ---

#### Oscillator
- $f_{OSC}$ Oscillator Frequency $R_{FREQ} = 80k$
  
- Oscillator Frequency Range
  
- $D_{MAX}$ Maximum Duty Cycle
  
- $f_{SYNC/OSC}$ Recommended Maximum Synchronized Frequency Ratio $f_{OSC} = 300kHz$ (Note 6)
  
- $t_{SYNC(MIN)}$ MODE/SYNC Minimum Input Pulse Width $V_{SYNC} = 0V$ to $5V$
  
- $t_{SYNC(MAX)}$ MODE/SYNC Maximum Input Pulse Width $V_{SYNC} = 0V$ to $5V$
  
- $V_{IL(MODE)}$ Low Level MODE/SYNC Input Voltage
  
- $V_{IH(MODE)}$ High Level MODE/SYNC Input Voltage
  
- $R_{MODE/SYNC}$ MODE/SYNC Input Pull-Down Resistance
  
- $V_{FREQ}$ Nominal $FREQ$ Pin Voltage

#### Low Dropout Regulator
- $V_{INTVCC}$ INTVCC Regulator Output Voltage $V_{IN} = 7.5V$
  
- $\Delta V_{INTVCC}$ INTVCC Regulator Line Regulation $7.5V \leq V_{IN} \leq 15V$
  
- $\Delta V_{IN1}$ INTVCC Regulator Line Regulation $15V \leq V_{IN} \leq 30V$
  
- $V_{LOD(O/LOAD)}$ INTVCC Load Regulation $V_{IN} = 7.5V$, $0 \leq I_{INTVCC} \leq 20mA$
  
- $V_{DROPOUT}$ INTVCC Regulator Dropout Voltage $V_{INTVCC} = \text{Open}$, $I_{INTVCC} = 20mA$
  
- $I_{INTVCC}$ Bootstrap Mode INTVCC Supply Current in Shutdown $RUN = 0V$, SENSE = $5V$

#### GATE Driver
- $t_r$ GATE Driver Output Rise Time $C_L = 3300pF$ (Note 7)
  
- $t_f$ GATE Driver Output Fall Time $C_L = 3300pF$ (Note 7)

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LTC3704E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the −40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3704I is guaranteed over the full −40°C to 125°C operating temperature range.

**Note 3:** $T_J$ is calculated from the ambient temperature $T_A$ and power dissipation $P_D$ according to the following formula:

$$T_J = T_A + (P_D \times 120°C/W)$$

**Note 4:** The dynamic input supply current is higher due to power MOSFET gate charging ($Q_G \times f_{OSC}$). See Applications Information.

**Note 5:** The LTC3704 is tested in a feedback loop that servos $V_{FB}$ to the reference voltage with the $I_{TH}$ pin forced to a voltage between 0V and 1.4V (the no load to full load operating voltage range for the $I_{TH}$ pin is 0.3V to 1.23V).

**Note 6:** In a synchronized application, the internal slope compensation gain is increased by 25%. Synchronizing to a significantly higher ratio will reduce the effective amount of slope compensation, which could result in subharmonic oscillation for duty cycles greater than 50%.

**Note 7:** Rise and fall times are measured at 10% and 90% levels.
TYPICAL PERFORMANCE CHARACTERISTICS

NFB Voltage vs Temp

NFB Voltage Line Regulation

NFB Pin Current vs Temperature

Shutdown Mode IQ vs VIN

Shutdown Mode IQ vs Temperature

Burst Mode IQ vs VIN

Burst Mode IQ vs Temperature

Dynamic IQ vs Frequency

Gate Drive Rise and Fall Time vs CL

\[
C_L = 3300 \text{pF} \\
I_{Q(TOT)} = 550 \mu A + Qg \times f
\]
**TYPICAL PERFORMANCE CHARACTERISTICS**

**RUN Thresholds vs $V_{IN}$**

- $V_{IN}$ (V) vs RUN Thresholds (V)
- $V_{IN}$ range: 0 to 40
- RUN Thresholds range: 1.2 to 1.5

**RUN Thresholds vs Temperature**

- Temperature ($^\circ$C) vs RUN Thresholds (V)
- Temperature range: -50 to 150
- RUN Thresholds range: 1.3 to 1.5

**$R_T$ vs Frequency**

- Frequency (kHz) vs $R_T$ (kΩ)
- Frequency range: 0 to 1000
- $R_T$ range: 10 to 1000

**Frequency vs Temperature**

- Temperature ($^\circ$C) vs Gate Frequency (kHz)
- Temperature range: -50 to 150
- Gate Frequency range: 275 to 350

**Maximum Sense Threshold vs Temperature**

- Temperature ($^\circ$C) vs Maximum Sense Threshold (mV)
- Temperature range: -50 to 150
- Maximum Sense Threshold range: 140 to 160

**SENSE Pin Current vs Temperature**

- Temperature ($^\circ$C) vs SENSE Pin Current (μA)
- Temperature range: -25 to 125
- SENSE Pin Current range: 0 to 45

**INTVCC Load Regulation**

- TA = 25°C
- INTVCC Load (mA) vs INTVCC Voltage (V)
- INTVCC Load range: 0 to 80
- INTVCC Voltage range: 5.0 to 5.2

**INTVCC Line Regulation**

- TA = 25°C
- $V_{IN}$ (V) vs INTVCC Voltage (V)
- $V_{IN}$ range: 0 to 40
- INTVCC Voltage range: 5.1 to 5.4

**INTVCC Dropout Voltage vs Current, Temperature**

- INTVCC Load (mA) vs Dropout Voltage (mV)
- Temperature range: -50 to 150°C
- Dropout Voltage range: 0 to 500

**INTVCC Dropout Voltage vs Current, Temperature**

- Temperature range: -50 to 150°C
- Dropout Voltage range: 0 to 500
- INTVCC Load range: 0 to 20 mA
PIN FUNCTIONS

RUN (Pin 1): The RUN pin provides the user with an accurate means for sensing the input voltage and programming the start-up threshold for the converter. The falling RUN pin threshold is nominally 1.248V and the comparator has 100mV of hysteresis for noise immunity. When the RUN pin is below this input threshold, the IC is shut down and the V\text{IN} supply current is kept to a low value (typ 10\mu A). The Absolute Maximum Rating for the voltage on this pin is 7V.

I_{TH} (Pin 2): Error Amplifier Compensation Pin. The current comparator input threshold increases with this control voltage. Nominal voltage range for this pin is 0V to 1.40V.

NFB (Pin 3): Receives the feedback voltage from the external resistor divider across the output. Nominal voltage for this pin in regulation is –1.230V.

FREQ (Pin 4): A resistor from the FREQ pin to ground programs the operating frequency of the chip. The nominal voltage at the FREQ pin is 0.62V.

MODE/SYNC (Pin 5): This input controls the operating mode of the converter and allows for synchronizing the operating frequency to an external clock. If the MODE/SYNC pin is connected to ground, Burst Mode operation is enabled. If the MODE/SYNC pin is connected to \text{INTV}_{CC}, or if an external logic-level synchronization signal is applied to this input, Burst Mode operation is disabled and the IC operates in a continuous mode.

GND (Pin 6): Ground Pin.

GATE (Pin 7): Gate Driver Output.

\text{INTV}_{CC} (Pin 8): The Internal 5.20V Regulator Output. The gate driver and control circuits are powered from this voltage. Decouple this pin locally to the IC ground with a minimum of 4.7\mu F low ESR tantalum or ceramic capacitor.

V\text{IN} (Pin 9): Main Supply Pin. Must be closely decoupled to ground.

SENSE (Pin 10): The Current Sense Input for the Control Loop. Connect this pin to the drain of the power MOSFET for V_{DS} sensing and highest efficiency. Alternatively, the SENSE pin may be connected to a resistor in the source of the power MOSFET. Internal leading edge blanking is provided for both sensing methods.
The LTC3704 is a constant frequency, current mode controller for DC/DC positive-to-negative converter applications. The LTC3704 is distinguished from conventional current mode controllers because the current control loop can be closed by sensing the voltage drop across the power MOSFET switch instead of across a discrete sense resistor, as shown in Figure 2. This sensing technique improves efficiency, increases power density, and reduces the cost of the overall solution.

The nominal operating frequency of the LTC3704 is programmed using a resistor from the FREQ pin to ground and can be controlled over a 50kHz to 1000kHz range. In addition, the internal oscillator can be synchronized to an external clock applied to the MODE/SYNC pin and can be locked to a frequency between 100% and 130% of its nominal value. When the MODE/SYNC pin is left open, it is pulled low by an internal 50k resistor and Burst Mode operation is enabled. If this pin is taken above 2V or an external clock is applied, Burst Mode operation is disabled and the IC operates in continuous mode. With no load (or an extremely light load), the controller will skip pulses in order to maintain regulation and prevent excessive output ripple.

For circuit operation, please refer to the Block Diagram of the IC and Figure 1. In normal operation, the power MOSFET is turned on when the oscillator sets the PWM latch and is turned off when the current comparator C1 resets the latch. The divided-down output voltage is compared to an internal 1.230V reference by the error amplifier EA, which outputs an error signal at the ITH pin. The voltage on the ITH pin sets the current comparator C1 input threshold. When the load current increases, a fall in the NFB voltage relative to the reference voltage causes the ITH pin to rise, which causes the current comparator C1 to trip at a higher peak inductor current value. The average inductor current will therefore rise until it equals the load current, thereby maintaining output regulation.

For applications where maximizing the efficiency at very light loads (e.g., <100μA) is a high priority, Burst Mode operation should be applied (i.e., the MODE/SYNC pin should be connected to ground). In applications where fixed frequency operation is more critical than low current efficiency, or where the lowest output ripple is desired, pulse-skip mode operation should be used and the MODE/SYNC pin should be connected to the INTVCC pin. This allows discontinuous conduction mode (DCM) operation down to near the limit defined by the chip’s...
minimum on-time (about 175ns). Below this output current level, the converter will begin to skip cycles in order to maintain output regulation. Figures 3 and 4 show the light load switching waveforms for Burst Mode and Pulse-Skip Mode operation for the converter in Figure 1.

Burst Mode Operation

Burst Mode operation is selected by leaving the MODE/SYNC pin unconnected or by connecting it to ground. In normal operation, the range on the I_{TH} pin corresponding to no load to full load is 0.30V to 1.2V. In Burst Mode operation, if the error amplifier EA drives the I_{TH} voltage below 0.525V, the buffered I_{TH} input to the current comparator C1 will be clamped at 0.525V (which corresponds to 25% of maximum load current). The inductor current peak is then held at approximately 30mV divided by the power MOSFET R_{DS(ON)}. If the I_{TH} pin drops below 0.30V, the Burst Mode comparator B1 will turn off the power MOSFET and scale back the quiescent current of the IC to 250\mu A (sleep mode). In this condition, the load current will be supplied by the output capacitor until the I_{TH} voltage rises above the 50mV hysteresis of the burst comparator. At light loads, short bursts of switching (where the average inductor current is 25% of its maximum value) followed by long periods of sleep will be observed, thereby greatly improving converter efficiency. Oscilloscope waveforms illustrating Burst Mode operation are shown in Figure 3.

When an external clock signal drives the MODE/SYNC pin at a rate faster than the chip’s internal oscillator, the oscillator will synchronize to it. In this synchronized mode, Burst Mode operation is disabled. The constant frequency associated with synchronized operation provides a more controlled noise spectrum from the converter, at the expense of overall system efficiency of light loads.

When the oscillator’s internal logic circuitry detects a synchronizing signal on the MODE/SYNC pin, the internal oscillator ramp is terminated early and the slope compensation is increased by approximately 30%. As a result, in applications requiring synchronization, it is recommended that the nominal operating frequency of the IC be programmed to be about 75% of the external clock frequency. Attempting to synchronize to too high an external frequency (above 1.3f_{O}) can result in inadequate slope compensation and possible subharmonic oscillation (or jitter).

The external clock signal must exceed 2V for at least 25ns, and should have a maximum duty cycle of 80%, as shown in Figure 5. The MOSFET turn on will synchronize to the rising edge of the external clock signal.

Pulse-Skip Mode Operation

With the MODE/SYNC pin tied to a DC voltage above 1.2V, Burst Mode operation is disabled. The internal, 0.525V buffered I_{TH} burst clamp is removed, allowing the I_{TH} pin to directly control the current comparator from no load to full load. With no load, the I_{TH} pin is driven below 0.30V, the power MOSFET is turned off and sleep mode is invoked. Oscilloscope waveforms illustrating this mode of operation are shown in Figure 4.
INTVCC Regulator Bypassing and Operation

An internal, P-channel low dropout voltage regulator produces the 5.2V supply which powers the gate driver and logic circuitry within the LTC3704, as shown in Figure 7. The INTVCC regulator can supply up to 50mA and must be bypassed to ground immediately adjacent to the IC pins with a minimum of 4.7μF tantalum or ceramic capacitor. Good bypassing is necessary to supply the high transient currents required by the MOSFET gate driver.

Figure 7. Bypassing the LDO Regulator and Gate Driver Supply

For input voltages that don’t exceed 7V (the absolute maximum rating for this pin), the internal low dropout regulator in the LTC3704 is redundant and the INTVCC pin can be shorted directly to the VIN pin. With the INTVCC pin shorted to VIN, however, the divider that programs the regulated INTVCC voltage will draw 10μA of current from the input supply, even in shutdown mode. For applications that require the lowest shutdown mode input supply current, do not connect the INTVCC pin to VIN. Regardless of whether the INTVCC pin is shorted to VIN or not, it is always necessary to have the driver circuitry bypassed with a 4.7μF tantalum or low ESR ceramic capacitor to ground immediately adjacent to the INTVCC and GND pins.

In an actual application, most of the IC supply current is used to drive the gate capacitance of the power MOSFET. As a result, high input voltage applications in which a large power MOSFET is being driven at high frequencies can
APPLICATIONS INFORMATION

cause the LTC3704 to exceed its maximum junction temperature rating. The junction temperature can be estimated using the following equations:

\[ I_{Q(TOT)} = I_Q + f \cdot Q_G \]
\[ P_{IC} = V_{IN} \cdot (I_Q + f \cdot Q_G) \]
\[ T_J = T_A + P_{IC} \cdot R_{TH(JA)} \]

The total quiescent current \( I_{Q(TOT)} \) consists of the static supply current \( (I_Q) \) and the current required to charge and discharge the gate of the power MOSFET. The 10-pin MSOP package has a thermal resistance of \( R_{TH(JA)} = 120 \, ^\circ C/W \).

As an example, consider a power supply with \( V_{IN} = 5V \) and \( V_{SW(MAX)} = 12V \). The switching frequency is 500kHz, and the maximum ambient temperature is 70\(^\circ\)C. The power MOSFET chosen is the IRF7805, which has a maximum \( R_{DS(ON)} \) of 11m\( \Omega \) (at room temperature) and a maximum total gate charge of 37nC (the temperature coefficient of the gate charge is low).

\[ I_{Q(TOT)} = 600 \, \mu A + 37nC \cdot 500kHz = 19.1mA \]
\[ P_{IC} = 5V \cdot 19.1mA = 95mW \]
\[ T_J = 70^\circ C + 120^\circ C/W \cdot 95mW = 81.4^\circ C \]

This demonstrates how significant the gate charge current can be when compared to the static quiescent current in the IC.

To prevent the maximum junction temperature from being exceeded, the input supply current must be checked when operating in a continuous mode at high \( V_{IN} \). A tradeoff between the operating frequency and the size of the power MOSFET may need to be made in order to maintain a reliable IC junction temperature. Prior to lowering the operating frequency, however, be sure to check with power MOSFET manufacturers for their latest-and-greatest low \( Q_G \), low \( R_{DS(ON)} \) devices. Power MOSFET manufacturing technologies are continually improving, with newer and better performance devices being introduced almost yearly.

Output Voltage Programming

The output voltage is set by a resistor divider according to the following formula:

\[ V_O = V_{REF} \cdot \left(1 + \frac{R_2}{R_1}\right) + I_{NFB} \cdot R_2 \]

where \( V_{REF} = -1.230V \), and \( I_{NFB} \) is the current which flows out of the NFB pin \( (I_{NFB} = -7.5\mu A) \). In order to properly dimension \( R_2 \), including the effect of the NFB pin current, the following formula can be used:

\[ R_2 = \frac{V_{OUT} - V_{REF}}{\left(\frac{V_{REF} + I_{NFB}}{R_1}\right)} \]

The nominal 7.5\( \mu A \) current which flows out of the NFB pin has a production tolerance of approximately \( \pm 2.5\mu A \), so an output divider current of 500\( \mu A \) \( (R_1 = 2.49k) \) results in a 0.5% uncertainty in the output voltage. For low power applications where the output voltage tolerance is less important, efficiency can be increased by increasing the value of \( R_1 \).

Programming Turn-On and Turn-Off Thresholds with the RUN Pin

The LTC3704 contains an independent, micropower voltage reference and comparator detection circuit that remains active even when the device is shut down, as shown in Figure 8. This allows users to accurately program an input voltage at which the converter will turn on and off. The falling threshold voltage on the RUN pin is equal to the internal reference voltage of 1.248V. The comparator has 100mV of hysteresis to increase noise immunity.

The turn-on and turn-off input voltage thresholds are programmed using a resistor divider according to the following formulas:

\[ V_{IN(OFF)} = 1.248V \cdot \left(1 + \frac{R_2}{R_1}\right) \]
\[ V_{IN(ON)} = 1.348V \cdot \left(1 + \frac{R_2}{R_1}\right) \]
The resistor R1 is typically chosen to be less than 1M. For applications where the RUN pin is only to be used as a logic input, the user should be aware of the 7V Absolute Maximum Rating for this pin! The RUN pin can be connected to the input voltage through an external 1M resistor, as shown in Figure 8c, for “always on” operation.
Applications Circuits

A simple positive-to-negative application circuit for the LTC3704 is shown in Figure 1. The basic operation of this circuit is shown in Figure 9. During the on-time the inductor currents flow through the switch, and during the off-time these currents flow through the output diode. The use of inductors in series with both the input and output results in continuous currents in these capacitors, resulting in low input and output noise. Discontinuous currents flow in the switch, the coupling capacitor, and the diode.

Peak and Average Input and Switch Currents

The control loop in the LTC3704 is measuring the peak switch current (either by using the \( R_{\text{DS(ON)}} \) of the power MOSFET or by using a sense resistor in the MOSFET source), so the output current needs to be reflected back to the switch in order to dimension the power MOSFET and inductors properly. Based on the fact that, ideally, the input power is equal to the output power, the maximum average input current is:

\[
I_{\text{IN(MAX)}} = -I_{\text{O(MAX)}} \cdot \frac{D_{\text{MAX}}}{1-D_{\text{MAX}}}
\]

where \( I_{\text{O(MAX)}} \) is a negative number. The peak input current is:

\[
I_{\text{IN(PEAK)}} = -\left(1 + \frac{x}{2}\right) \cdot I_{\text{O(MAX)}} \cdot \frac{D_{\text{MAX}}}{1-D_{\text{MAX}}}
\]

In a positive-to-negative converter, however, the switch current is equal to \( I_{\text{IN}} + I_{\text{O}} \), so the maximum average switch current is:

\[
I_{\text{SW(MAX)}} = -I_{\text{O(MAX)}} \cdot \frac{1}{1-D_{\text{MAX}}}
\]

and the peak switch current is:

\[
I_{\text{SW(PEAK)}} = -\left(1 + \frac{x}{2}\right) \cdot I_{\text{O(MAX)}} \cdot \frac{1}{1-D_{\text{MAX}}}
\]

The maximum duty cycle, \( D_{\text{MAX}} \), should be calculated at minimum \( V_{\text{IN}} \).

Ripple Current \( \Delta I_L \) and the ‘\( x \)’ Factor

The constant ‘\( x \)’ in the equation above represents the percentage peak-to-peak total ripple current in the inductor, relative to its maximum value. For example, if 30% ripple current is chosen, then \( x = 0.30 \), and the peak current is 15% greater than the average.

For a current mode converter operating in CCM, slope compensation must be added for duty cycles above 50% in order to avoid subharmonic oscillation. For the LTC3704, this ramp compensation is internal. Having an internally fixed ramp compensation waveform, however, does place some constraints on the value of the inductor and the operating frequency. If too large an inductor is used, the resulting current ramp (\( \Delta I_L \)) will be small relative to the
APPLICATIONS INFORMATION

Internal ramp compensation (at duty cycles above 50%), and the converter operation will approach voltage mode (ramp compensation reduces the gain of the current loop). If too small an inductor is used, but the converter is still operating in CCM (near critical conduction mode), the internal ramp compensation may be inadequate to prevent subharmonic oscillation. To ensure good current mode gain and avoid subharmonic oscillation, it is recommended that the ripple current in the inductor fall in the range of 20% to 40% of the maximum average switch current. For example, if the maximum average switch current is 1A, choose a $\Delta I_L$ between 0.2A and 0.4A, and a value ‘$\chi$’ between 0.2 and 0.4.

Inductor Selection

Selecting inductors for a positive-to-negative converter is slightly more complicated than for a single-inductor topology like a buck or boost. The use of separate, uncoupled inductors can reduce the size of the solution, at the expense of input and output ripple. Using a coupled inductor complicates the design procedure, but can result in significantly lower input and/or output ripple. It will also reduce the number of components that the purchasing department has to keep track of.

Regardless of the design goals, however, the inductor selection process is an iterative one. The best recommendation is to use the equations as a guideline, and then to build a solution and measure the circuit’s performance. If the measured performance deviates from the design guidelines, substitute a bigger (or smaller) inductor, as appropriate, and repeat the measurements. In addition, do your best to minimize layout parasitics, which can have a significant effect on circuit performance.

The inductor currents for a positive-to-negative converter are calculated at full load current and minimum input voltage. The peak inductor currents can be significantly higher than the output current, especially with smaller inductors and lighter loads. The following formulae assume uncoupled inductors and CCM operation.

\[
I_{L1(PEAK)} = -\left(1 + \frac{\chi}{2}\right) \cdot I_{O(MAX)} \cdot \frac{D_{MAX}}{1 - D_{MAX}}
\]

\[
I_{L2(PEAK)} = -\left(1 + \frac{\chi}{2}\right) \cdot I_{O(MAX)}
\]

where “$\chi$” represents the percentage of ripple current. In a positive-to-negative converter, however, the switch current is the sum of the two inductor currents. Therefore,

\[
I_{SW(PEAK)} = -\left(1 + \frac{\chi}{2}\right) \cdot I_{O(MAX)} \cdot \frac{1}{1 - D_{MAX}}
\]

Since the control loop is looking at the switch current, and since the internal slope compensation is acting on this switch current, the ripple current percentage should be between 20% and 40% of the maximum average current at $V_{IN(MIN)}$ and $I_{O(MAX)}$. This corresponds to a value of “$\chi$” in the equations above between 0.20 and 0.40. Expressing this ripple current as a function of the output current results in the following equation for calculating the inductor value:

\[
L1 = L2 = \frac{V_{IN(MIN)} \cdot D_{MAX}}{\Delta I_{SW} \cdot f}
\]

where:

\[
\Delta I_{SW} = -\chi \cdot I_{O(MAX)} \cdot \frac{1}{1 - D_{MAX}}
\]

By using a coupled inductor with a 1:1 turns ratio, the value of inductance in the equation above can be replaced by 2L due to mutual inductance. Doing this maintains the same total ripple current and energy storage in the inductor. Substituting 2L yields the following equation for 1:1 coupled inductors:

\[
L1 = L2 = \frac{V_{IN(MIN)} \cdot \Delta L \cdot f}{2 \cdot \Delta I_{L} \cdot f} \cdot D_{MAX}
\]

For the case of uncoupled inductors, choose minimum saturation currents based on the peak currents outlined in
the initial equations for $I_{L1(\text{PEAK})}$ and $I_{L2(\text{PEAK})}$. If a coupled inductor is used, make sure that the minimum saturation current for the parallel configuration exceeds the maximum switch current, or:

$$I_{\text{SAT(MIN)}} \geq \left(1 + \frac{\chi}{2}\right) \cdot I_{\text{O(MAX)}} \cdot \frac{1}{1 - D_{\text{MAX}}}$$

The saturation current rating should be checked at minimum input voltage (which results in the highest average inductor current) and maximum load current.

**Operating in Discontinuous Mode**

Discontinuous mode operation occurs when the load current is low enough to allow the inductor current to run out during the off-time of the switch, as shown in Figure 10. Once the inductor current is near zero, the switch and diode capacitances resonate with the inductance to form damped ringing at 1MHz to 10MHz. If the off-time is long enough, the drain voltage will settle to the input voltage.

Depending on the input voltage and the residual energy in the inductor, this ringing can cause the drain of the power MOSFET to go below ground where it is clamped by the body diode. This ringing is not harmful to the IC and it has not been shown to contribute significantly to EMI. Any attempt to damp it with a snubber will degrade the efficiency.

**Power MOSFET or Sense Resistor Selection**

If the maximum voltage on the drain of the power MOSFET (which is $V_{\text{IN(MAX)}} + V_{\text{OUT}}$, plus any transients) is less than 36V then the circuit can take advantage of the LTC3704’s No RSENSE technology in order to improve efficiency and eliminate the sense resistor. For higher switch voltages the SENSE pin should be connected to a resistor in the source of the power MOSFET, as shown in Figure 2. Internal leading-edge blanking is provided in the LTC3704 to eliminate the need for filtering components on the SENSE pin.

In both positive-to-negative and flyback converters the maximum switch current is equal to the inductor current plus the output current. As a result, the peak switch current is:

$$I_{\text{SW(PEAK)}} = \left(1 + \frac{\chi}{2}\right) \cdot I_{\text{O(MAX)}} \cdot \frac{1}{1 - D_{\text{MAX}}}$$

where $I_{\text{O(MAX)}}$ is a negative number.

During the switch on-time, the control circuit limits the maximum voltage drop across the power MOSFET to 150mV (at low duty cycles). The peak switch current is therefore limited to $150\text{mV} / R_{\text{DS(ON)}}$. The relationship between the maximum load current, the duty cycle and the $R_{\text{DS(ON)}}$ of the power MOSFET is:

$$R_{\text{DS(ON)}} \leq \frac{V_{\text{SENSE(MAX)}}}{I_{\text{SW(PEAK)}}}$$

or

$$R_{\text{DS(ON)}} \leq V_{\text{SENSE(MAX)}} \cdot \frac{D_{\text{MAX}} - 1}{\left(1 + \frac{\chi}{2}\right) \cdot I_{\text{O(MAX)}} \cdot \rho_{T}}$$

again, where $I_{\text{O(MAX)}}$ is a negative number. The $V_{\text{SENSE(MAX)}}$ term is typically 150mV at low duty cycle, and is reduced to about 100mV at a duty cycle of 92% due to slope compensation, as shown in Figure 11. The $\rho_{T}$ term accounts for the temperature coefficient of the $R_{\text{DS(ON)}}$ of the MOSFET, which is typically 0.4%/°C. Figure 12 illustrates the variation of $R_{\text{DS(ON)}}$ over temperature for a typical power MOSFET (normalized for simplicity).
Another method of choosing which power MOSFET to use is to check the maximum output current for a given \( R_{DS(ON)} \), since MOSFET on-resistances are generally available in discrete values.

\[
I_{O(MAX)} = -V_{SENSE(MAX)} \cdot \frac{1-D_{MAX}}{\left(1+\frac{\chi}{2}\right) \cdot R_{DS(ON)} \cdot \rho_T}
\]

For the case where a conventional sense resistor is used,

\[
R_{SENSE} = V_{SENSE(MAX)} \cdot \frac{D_{MAX} - 1}{\left(1+\frac{\chi}{2}\right) \cdot I_{O(MAX)}}
\]

Sense resistors are generally low TC and are available with different ranges of tolerance depending on price. The power dissipated in the sense resistor is:

\[
P_{SENSE} = (I_{SW(PEAK)})^2 \cdot R_{SENSE} \cdot D_{MAX}
\]

### Calculating Power MOSFET Switching and Conduction Losses and Junction Temperatures

In order to calculate the junction temperature of the power MOSFET, the power dissipated by the device must be known. This power dissipation is a function of the duty cycle, the load current and the junction temperature itself (due to the positive temperature coefficient of its \( R_{DS(ON)} \)).

\[
P_{FET} = \left(\frac{-I_{O(MAX)}}{1-D_{MAX}}\right)^2 \cdot R_{DS(ON)} \cdot \frac{I_{O(MAX)}}{1-D_{MAX}} \cdot C_{RSS} \cdot f + k \cdot (V_{IN} - V_O)^{1.85} \cdot \frac{I_{O(MAX)}}{1-D_{MAX}} \cdot C_{RSS} \cdot f
\]

where \( I_{O(MAX)} \) and \( V_O \) are negative numbers.

The first term in the equation above represents the \( I^2R \) losses in the device, and the second term, the switching losses. The constant, \( k = 1.7 \), is an empirical factor inversely related to the gate drive current and has the dimension of 1/current.

From a known power dissipated in the power MOSFET, its junction temperature can be obtained using the following formula:

\[
T_J = T_A + P_{FET} \cdot R_{TH(JA)}
\]
The $R_{TH(JA)}$ to be used in this equation normally includes the $R_{TH(JC)}$ for the device plus the thermal resistance from the case to the ambient temperature ($R_{TH(CA)}$). This value of $T_J$ can then be compared to the original, assumed value used in the iterative calculation process.

**Output Diode Selection**

To maximize efficiency, a fast switching diode with low forward drop and low reverse leakage is desired. The output diode in a positive-to-negative converter conducts current during the switch off-time. The peak reverse voltage that the diode must withstand is equal to $V_{IN(MAX)} - V_O$. The average forward current in normal operation is equal to the output current, and the peak current is equal to the peak inductor current.

\[
I_D(\text{PEAK}) = \left(1 + \frac{x}{2}\right) \cdot I_O(\text{MAX}) \cdot \frac{1}{1 - D_{\text{MAX}}}
\]

The power dissipated by the diode is:

\[P_D = I_O(\text{MAX}) \cdot V_D\]

and the diode junction temperature is:

\[T_J = T_A + P_D \cdot R_{TH(JA)}\]

The $R_{TH(JA)}$ to be used in this equation normally includes the $R_{TH(JC)}$ for the device plus the thermal resistance from the board to the ambient temperature in the enclosure.

Remember to keep the diode lead lengths short and to observe proper switch-node layout (see Board Layout Checklist) to avoid excessive ringing and increased dissipation.

**Selecting the DC Coupling Capacitor**

The voltage on the coupling capacitor in a positive-to-negative converter is $V_{IN(MAX)} - V_O$, plus any additional $\Delta V$ due to the ripple currents in the inductors. Generally, the DC coupling capacitor is dimensioned based on the high RMS ripple which flows in it, as shown in Figure 13.

The minimum RMS current rating of this capacitor must exceed:

\[I_{\text{RMS(CAP)}} = - I_O(\text{MAX}) \cdot \sqrt{\frac{D_{\text{MAX}}}{1 - D_{\text{MAX}}}}\]

\[\Delta V_{O(\text{P-P})} = \frac{1 - D_{\text{MAX}}}{f} \cdot \frac{V_O}{L_2} \left[ - ESR \cdot \frac{1}{8 \cdot f \cdot C_0} \right]\]

The ESR can be minimized by using high quality, X5R- or X7R-dielectric ceramic capacitor in parallel with a larger value tantalum or aluminum electrolytic bulk capacitor. Depending upon the application, it may be that the ceramic capacitor alone will be sufficient.

The RMS ripple current rating of the output capacitor needs to be greater than:
\[ I_{\text{RMS\text{\textregistered}COUT}} \geq \sqrt{\frac{1}{12} \cdot (1-D_{\text{MAX}}) \cdot V_0 \cdot \frac{1}{\text{f} \cdot \text{L}^2}} \]

It should be noted that these equations assume no coupling between the inductors. If the inductors are wound on the same core, the ripple currents at the input and output can be tuned to very low values, and so the equations above would be extremely conservative. It is highly recommended that the user experiment in the lab with the same magnetics and capacitors which will be used in production.

Note that the ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor or to choose a capacitor rated at a higher temperature than required. Several capacitors may also be placed in parallel to meet size or height requirements in the design.

Manufacturers such as Nichicon, United Chemicon and Sanyo should be considered for high performance through-hole capacitors. The OS-CON semiconductor dielectric capacitor available from Sanyo has the lowest product of ESR and size of any aluminum electrolytic, at a somewhat higher price.

In surface mount applications, multiple capacitors may have to be placed in parallel in order to meet the ESR or RMS current handling requirements of the application.

<table>
<thead>
<tr>
<th>VENDOR</th>
<th>COMPONENTS</th>
<th>TELEPHONE</th>
<th>WEB ADDRESS</th>
</tr>
</thead>
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</tbody>
</table>
APPLICATIONS INFORMATION

Aluminum electrolytic and dry tantalum capacitors are both available in surface mount packages. In the case of tantalum, it is critical that the capacitors have been surge tested for use in switching power supplies. An excellent choice is AVX TPS series of surface mount tantalum. Also, ceramic capacitors are now available with extremely low ESR, ESL and high ripple current ratings.

Input Capacitor Selection

The input voltage source impedance determines the size of the input capacitor, which is typically in the range of 10μF to 100μF. A low ESR capacitor is recommended, although it is not as critical as for the output capacitor.

The RMS input capacitor ripple current for a positive-to-negative converter is:

\[ I_{\text{RMS(CIN)}} = \sqrt{\frac{1}{12} \cdot \frac{V_{\text{IN(MIN)}}}{L_1 \cdot f} \cdot D_{\text{MAX}}} \]

Please note that the input capacitor can see a very high surge current when a battery is suddenly connected to the input of the converter and solid tantalum capacitors can fail catastrophically under these conditions. Be sure to specify surge-tested capacitors!

Burst Mode Operation and Considerations

The choice of MOSFET R_{DS(ON)} and inductor value also determines the load current at which the LTC3704 enters Burst Mode operation. When bursting, the controller clamps the peak inductor current to approximately:

\[ I_{\text{BURST(PEAK)}} = \frac{30\text{mV}}{R_{\text{DS(ON)}}} \]

which represents about 20% of the maximum 150mV SENSE pin voltage. The corresponding average current depends upon the amount of ripple current. Lower inductor values (higher \( \Delta I_L \)) will reduce the load current at which Burst Mode operations begins, since it is the peak current that is being clamped.

The output voltage ripple can increase during Burst Mode operation if \( \Delta I_L \) is substantially less than \( I_{\text{BURST}} \). This can occur if the input voltage is very low or if a very large inductor is chosen. At high duty cycles, a skipped cycle causes the inductor current to quickly decay to zero. However, because \( \Delta I_L \) is small, it takes multiple cycles for the current to ramp back up to \( I_{\text{BURST(PEAK)}} \). During this inductor charging interval, the output capacitor must supply the load current and a significant droop in the output voltage can occur. Generally, it is a good idea to choose a value of inductor \( \Delta I_L \) between 20% and 40% of \( I_{\text{IN(MAX)}} \). The alternative is to either increase the value of the output capacitor or disable Burst Mode operation using the MODE/SYNC pin.

Burst Mode operation can be defeated by connecting the MODE/SYNC pin to a high logic-level voltage (either with a control input or by connecting this pin to INTV_{CC}). In this mode, the burst clamp is removed, and the chip can operate at constant frequency from continuous conduction mode (CCM) at full load, down into deep discontinuous conduction mode (DCM) at light load. Prior to skipping pulses at very light load (i.e., <5-10% of full load), the controller will operate with a minimum switch on-time in DCM. Pulse skipping prevents a loss of control of the output at very light loads and reduces output voltage ripple.

Checking Transient Response

The regulator loop response can be verified by looking at the load transient response. Switching regulators generally take several cycles to respond to an instantaneous step in resistive load current. When the load step occurs, \( V_O \) immediately shifts by an amount equal to \( (\Delta I_{LOAD})(ESR) \), and then \( C_O \) begins to charge or discharge (depending on the direction of the load step) as shown in Figure 14. The

![Figure 14. Load Step Response for the Circuit in Figure 1.](image)
regulator feedback loop acts on the resulting error amp output signal to return \( V_0 \) to its steady-state value. During this recovery time, \( V_0 \) can be monitored for overshoot or ringing that would indicate a stability problem.

A second, more severe transient can occur when connecting loads with large (>1\( \mu \)F) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with \( C_O \), causing a nearly instantaneous drop in \( V_0 \). No regulator can deliver enough current to prevent this problem if the load switch resistance is low and it is driven quickly. The only solution is to limit the rise time of the switch drive in order to limit the inrush current \( \frac{dI}{dt} \) to the load.

**Design Example: A 5V to 15V Input, –5V at 2A Output Positive-to-Negative Converter**

The design example presented here will be for the circuit shown in Figure 1. The input voltage range is 5V to 15V, and the output is -5V. The maximum load current is 2A at an input voltage of 5V (3A peak), and 3A at an input voltage of 15V (5A peak).

1. The maximum duty cycle of the main switch is:

\[
D_{\text{MAX}} = \frac{V_{\text{OUT}}}{V_{\text{OUT}} - V_{\text{IN(MIN)}}} = -\frac{-5}{-10} = 50\%
\]

2. Pulse-Skip operation is chosen, so the MODE/SYNC pin is connected to the INTVCC pin.

3. The operating frequency is chosen to be 300kHz to reduce the size of the inductors. From Figure 5, the resistor from the FREQ pin to ground is 80.6k.

4. A total inductor ripple current of 40% of the maximum is chosen, so the inductor ripple current is:

\[
\Delta I_{L1} = -\chi \cdot I_{O(\text{MAX})} \cdot \frac{D_{\text{MAX}}}{1 - D_{\text{MAX}}} = 0.4 \cdot 2.0 \cdot \frac{0.5}{1 - 0.5} = 0.8A
\]

For a standard 1:1 coupled inductor, the inductance is therefore:

\[
L1 = L2 = \frac{V_{\text{IN(MIN)}}}{2 \cdot \Delta I_{L1} \cdot f} = \frac{5}{2 \cdot 0.8 \cdot 300k} \cdot 0.5 = 5.2\mu H
\]

The minimum saturation current for this inductor is:

\[
I_{\text{LSAT(MIN)}} \geq -\left(1 + \frac{\chi}{2}\right) \cdot I_{O(\text{MAX})} \cdot \frac{1}{1 - D_{\text{MAX}}} = 1.2 \cdot 2.0 \cdot \frac{1}{1 - 0.5} = 4.8A
\]

The inductor chosen is a BH Electronics part # 510-1009, which has an open circuit parallel inductance of 4.56\( \mu \)H and a maximum dc current rating of 6.5A.

5. For the power MOSFET,

\[
R_{\text{DS(ON)}} \leq V_{\text{SENSE(MAX)}} \cdot \frac{D_{\text{MAX}} - 1}{\left(1 + \frac{\chi}{2}\right) \cdot I_{O(\text{MAX})} \cdot \rho_T}
\]

At the maximum duty cycle of 50%, the maximum SENSE pin voltage is reduced to 130mV due to slope compensation, as shown in Figure 11. Assuming a maximum junction temperature of 125°C for the power MOSFET, \( \rho_T = 1.5 \), and

\[
R_{\text{DS(ON)}} \leq 0.13 \cdot \frac{0.5 - 1}{-1.2 \cdot 2.0 \cdot 1.5} = 18.1\text{m\Omega}
\]

The MOSFET chosen was Siliconix/Vishay’s Si4884, which has a maximum \( R_{\text{DS(ON)}} = 16.5\text{m\Omega} \) at \( V_{GS} = 4.5V \) at 25°C. The minimum \( B V_{DSS} = 30V \) and the maximum gate charge is \( Q_G = 20nC \).

6. The output diode must withstand a reverse voltage \( V_{\text{IN(MAX)}} - V_0 = 20V \) and a continuous current of \( I_{O(\text{MAX})} = 5.0A \) (peak output current at \( V_{\text{IN}} = 15V \)). The peak current in the diode is:

\[
I_{D(\text{PEAK})} = \left(1 + \frac{\chi}{2}\right) \cdot I_{O(\text{MAX})} = 6A
\]

The power dissipated in this diode at full load is:
\[ P_D = I_{O(MAX)} \cdot V_F \]

Assuming a maximum junction temperature of 125°C and a forward voltage of approximately 0.33V at 3A (the maximum output current at \( V_{IN} = 15V \)), this diode will dissipate 1W at full load. The diode selected was the MBRD835L from On Semiconductor, packaged in a D-Pak.

7. The DC coupling capacitor must be capable of handling an RMS current of:

\[ I_{D(PEAK)} = I_{O(MAX)} \cdot \sqrt{\frac{D_{MAX}}{1 - D_{MAX}}} = 3A \]
The capacitor used was a TDK 47μF, 16V X5R-dielectric ceramic (C5750X5R1C476M), mainly because of its low ESR (2.4mΩ) and high RMS current capability.

8. The peak-to-peak output ripple is:

\[
\Delta V_{O(P-P)} = \frac{1 - 0.5 \cdot \frac{5.0}{300k}}{8 \cdot f \cdot C_0} = 13.7mV
\]

As a first try, a TDK 100μF, 6.3V X5R-dielectric ceramic capacitor was chosen (C5750X5R0J107M). This capacitor has a very low 1.6mΩ of ESR. As a result, the peak-to-peak output ripple voltage is:

This ripple voltage calculation also assumes no coupling between the inductors, making the 13.7mV number very conservative.

Figure 15 illustrates the same basic application shown in Figure 1, with the added features of soft-start and undervoltage lockout on the input supply. Figures 16 through 21 illustrate the measured performance for this converter. The peak efficiency is 87% at a load current of 2A and the peak-to-peak output ripple is less than 10mV. Figures 19 and 20 illustrate the load step response at 5V and 15V input, and Figure 21, the start-up characteristics with a resistive load.
Applications Information

PC Board Layout Checklist

1. In order to minimize switching noise and improve output load regulation, the GND pin of the LTC3704 should be connected directly to 1) the negative terminal of the INTVCC decoupling capacitor, 2) the negative terminal of the output decoupling capacitors, 3) the source of the power MOSFET or the bottom terminal of the sense resistor, 4) the negative terminal of the input capacitor and 5) at least one via to the ground plane immediately adjacent to Pin 6. The ground trace on the top layer of the PC board should be as wide and short as possible to minimize series resistance and inductance.

Figure 22. LTC3704 Positive-to-Negative Converter Suggested Layout

Figure 23. LTC3704 Positive-to-Negative Converter Layout Diagram
2. Beware of ground loops in multiple layer PC boards. Try to maintain one central ground node on the board and use the input capacitor to avoid excess input ripple for high output current power supplies. If the ground plane is to be used for high DC currents, choose a path away from the small-signal components.

3. Place the $C_{\text{VCC}}$ capacitor immediately adjacent to the INTV$_{\text{CC}}$ and GND pins on the IC package. This capacitor carries high di/dt MOSFET gate drive currents. A low ESR X5R-dielectric 4.7 μF ceramic capacitor works well here.

4. The high di/dt loop from the drain of the power MOSFET, through the coupling capacitor and back through the diode to ground should be kept as tight as possible to reduce inductive ringing. Excess inductance can cause increased stress on the power MOSFET and increase HF noise on the drain node. It is also important to keep the cathode of the diode as close as possible to the MOSFET source or the bottom of the sense resistor.

5. Check the stress on the power MOSFET by measuring its drain-to-source voltage directly across the device terminals (reference the ground of a single scope probe directly to the source pad on the PC board). Beware of inductive ringing which can exceed the maximum specified voltage rating of the MOSFET. If this ringing cannot be avoided and exceeds the maximum rating of the device, either choose a higher voltage device or specify an avalanche-rated power MOSFET. Not all MOSFETs are created equal (some are more equal than others).

6. Place the small-signal components away from high frequency switching nodes. In the layout shown in Figure 22, all of the small-signal components have been placed on one side of the IC and all of the power components have been placed on the other. This also allows the use of a pseudo-Kelvin connection for the signal ground, where high di/dt gate driver currents flow out of the IC ground pin in one direction (to the bottom plate of the INTV$_{\text{CC}}$ decoupling capacitor) and small-signal currents flow in the other direction.

7. If a sense resistor is used in the source of the power MOSFET, minimize the capacitance between the SENSE pin trace and any high frequency switching nodes. The LTC3704 contains an internal leading edge blanking time of approximately 180ns, which should be adequate for most applications.

8. For optimum load regulation and true remote sensing, the top of the output resistor divider should connect independently to the top of the output capacitor (Kelvin connection), staying away from any high dV/dt traces. Place the divider resistors near the LTC3704 in order to keep the high impedance FB node short.

9. For applications with multiple switching power converters connected to the same input supply, make sure that the input filter capacitor for the LTC3704 is not shared with other converters. AC input current from another converter could cause substantial input voltage ripple, and this could interfere with the operation of the LTC3704. A few inches of PC trace or wire ($L \approx 100\text{nH}$) between the $C_{\text{IN}}$ of the LTC3704 and the actual source $V_{\text{IN}}$ should be sufficient to prevent current sharing problems.
**APPLICATIONS INFORMATION**

**Figure 24.** 3V to 5V Input, –8V at 1.2A Output Converter

**Figure 25.** Maximum Output Current vs Input Voltage

**Figure 26.** Output Efficiency at 3V and 5V Input

**Figure 27.** Load Step Response at 3V Input

**Figure 28.** Load Step Response at 5V Input
LTC3704

APPLICATIONS INFORMATION

Figure 29. High Power SLIC Supply
PACKAGE DESCRIPTION

MS Package  
10-Lead Plastic MSOP  
(Reference LTC DWG # 05-08-1661)

NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.  
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE  
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.  
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE  
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
## Related Parts

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>LT®1175</td>
<td>Negative Linear Low Dropout Regulator</td>
<td>User-Selectable Current Limit from 200mA to 800mA, 0.4V Dropout at 500mA, 45μA Operating Current</td>
</tr>
<tr>
<td>LT1619</td>
<td>Current Mode PWM Controller</td>
<td>300kHz Fixed Frequency, Boost, SEPIC, Flyback Topology</td>
</tr>
<tr>
<td>LTC1624</td>
<td>Current Mode DC/DC Controller</td>
<td>SO-8; 200kHz Operating Frequency; Buck, Boost, SEPIC Design; VIN Up to 36V</td>
</tr>
<tr>
<td>LTC1700</td>
<td>No RSENSE Synchronous Step-Up Controller</td>
<td>Up to 95% Efficiency, Operation as Low as 0.9V Input</td>
</tr>
<tr>
<td>LTC1871</td>
<td>No RSENSE Boost, Flyback and SEPIC Controller</td>
<td>2.5V ≤ VIN ≤ 30V, Current Mode Control, Programmable fOSC from 50kHz to 1MHz</td>
</tr>
<tr>
<td>LTC1872</td>
<td>SOT-23 Boost Controller</td>
<td>Delivers Up to 5A, 550kHz Fixed Frequency, Current Mode</td>
</tr>
<tr>
<td>LT1930</td>
<td>1.2MHz, SOT-23 Boost Converter</td>
<td>Up to 34V Output, 2.6V ≤ VIN ≤ 16V, Miniature Design</td>
</tr>
<tr>
<td>LT1931</td>
<td>Inverting 1.2MHz, SOT-23 Converter</td>
<td>Positive-to-Negative DC/DC Conversion, Miniature Design</td>
</tr>
<tr>
<td>LT1964</td>
<td>ThinSOT™ Linear Low Dropout Regulator</td>
<td>200mA Output Current, Low Noise, 340mV Drop Out at 200mA, 5-Lead ThinSOT</td>
</tr>
<tr>
<td>LTC3401/LTC3402</td>
<td>1A/2A 3MHz Synchronous Boost Converters</td>
<td>Up to 97% Efficiency, Very Small Solution, 0.5V ≤ VIN ≤ 5V</td>
</tr>
</tbody>
</table>

ThinSOT is a trademark of Linear Technology Corporation.