Photoflash Chargers with Adjustable Input Current and IGBT Drivers

**FEATURES**
- **Adjustable Input Current**
- **Integrated IGBT Driver**
- **No Output Voltage Divider Needed**
- **Uses Small Transformers: 5.8mm × 5.8mm × 3mm**
- **Fast Photoflash Charge Times**
- **Charges Any Size Photoflash Capacitor**
- **Supports Operation from Single Li-Ion Cell, Two AA Cells or any Supply from 1.5V Up to 16V**
- **Small 10-Lead (3mm × 2mm) DFN Package**

**DESCRIPTION**

The LT® 3585 series are highly integrated ICs designed to charge photoflash capacitors in digital and film cameras. A new control technique allows for the use of extremely small transformers. Each part contains an on-chip high voltage NPN power switch. Output voltage detection is completely contained within the part, eliminating the need for any discrete zener diodes or resistors. The output voltage can be adjusted by simply changing the turns ratio of the transformer.

The CHRG/IADJ pin gives full control of the part to the user. Driving CHRG/IADJ low puts the part in low power shutdown. The CHRG/IADJ pin can also be used to reduce the input current of the charger, useful in extending battery life. The DONE pin indicates when the part has completed charging.

The LT3585 series of parts are housed in tiny 3mm × 2mm DFN packages.

**APPLICATIONS**
- Digital/Film Camera Flash
- PDA/Cell Phone Flash
- Emergency Strobe

**TYPICAL APPLICATION**

LT3585-1 Photoflash Charger Uses High Efficiency 2mm Tall Transformers with Tunable IGBT Gate Drive

**Fast Charge Time**

<table>
<thead>
<tr>
<th>VERSION</th>
<th>INPUT CURRENT (mA)</th>
<th>NORMAL MODE CHARGE TIME (Sec)</th>
<th>REDUCED MODE CHARGE TIME (Sec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LT3585-3</td>
<td>800/400</td>
<td>3.3</td>
<td>6.6</td>
</tr>
<tr>
<td>LT3585-0</td>
<td>550/275</td>
<td>4.6</td>
<td>9.2</td>
</tr>
<tr>
<td>LT3585-2</td>
<td>400/200</td>
<td>5.8</td>
<td>12.6</td>
</tr>
<tr>
<td>LT3585-1*</td>
<td>250/115</td>
<td>5.0</td>
<td>14.6</td>
</tr>
</tbody>
</table>

100µF capacitor, 320V, \( V_{IN} = V_{BAT} = 3.6V \)

*50µF capacitor, 320V, \( V_{IN} = V_{BAT} = 3.6V \)

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**ABSOLUTE MAXIMUM RATING**

(Not 1)  
\( V_{IN} \) Voltage \( \leq 16V \)  
\( V_{BATT} \) Voltage \( \leq 16V \)  
\( SW \) Voltage \( \leq 60V \)  
\( SW \) Pin Negative Current \( \leq -1A \)  
CHRG/IADJ Voltage \( \leq 10V \)  
IGBTWR Voltage \( \leq 10V \)  
IGBTIN Voltage \( \leq 10V \)  
IGBTPU Voltage \( \leq 10V \)  
IGBTPD Voltage \( \leq 10V \)  
DONE Voltage \( \leq 10V \)  
Current Into DONE Pin \( 0.2mA/-1mA \)  
Maximum Junction Temperature \( \leq 125°C \)  
Operating Temperature Range (Note 2) \( -40°C \) to \( 85°C \)  
Storage Temperature Range \( -65°C \) to \( 125°C \)  

**ELECTRICAL CHARACTERISTICS**

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at \( T_A = 25°C \). \( V_{IN} = V_{BATT} = V_{CHRG} = 3V \) unless otherwise noted (Note 2). Specifications are for the LT3585-0, LT3585-1, LT3585-2, LT3585-3 unless otherwise noted.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Quiescent Current</td>
<td>( V_{CHRG} = 3V ), Not Switching, ( V_{CHRG} = 0V ), In Shutdown</td>
<td>5</td>
<td>8</td>
<td>0</td>
<td>mA</td>
</tr>
<tr>
<td>( V_{IN} ) Voltage Range</td>
<td>●</td>
<td>2.5</td>
<td>16</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( V_{BATT} ) Voltage Range</td>
<td>●</td>
<td>1.5</td>
<td>16</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Switch Current Limit</td>
<td>LT3585-3 (Note 3)</td>
<td>1.55</td>
<td>1.7</td>
<td>1.85</td>
<td>A</td>
</tr>
<tr>
<td></td>
<td>LT3585-0 (Note 3)</td>
<td>1.1</td>
<td>1.2</td>
<td>1.3</td>
<td>A</td>
</tr>
<tr>
<td></td>
<td>LT3585-2 (Note 3)</td>
<td>0.75</td>
<td>0.85</td>
<td>0.95</td>
<td>A</td>
</tr>
<tr>
<td></td>
<td>LT3585-1 (Note 3)</td>
<td>0.45</td>
<td>0.55</td>
<td>0.65</td>
<td>A</td>
</tr>
<tr>
<td>Switch ( V_{CESAT} )</td>
<td>LT3585-3, ( I_{SW} = 1.4A )</td>
<td>485</td>
<td>mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>LT3585-0, ( I_{SW} = 1A )</td>
<td>330</td>
<td>mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>LT3585-2, ( I_{SW} = 700mA )</td>
<td>230</td>
<td>mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>LT3585-1, ( I_{SW} = 400mA )</td>
<td>140</td>
<td>mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{OUT} ) Comparator Trip Voltage</td>
<td>Measured as ( V_{SW} - V_{BATT} )</td>
<td>31</td>
<td>31.5</td>
<td>32</td>
<td>V</td>
</tr>
<tr>
<td>( V_{OUT} ) Comparator Overdrive</td>
<td>300ns Pulse Width</td>
<td>200</td>
<td>400</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>DCM Comparator Trip Voltage</td>
<td>Measured as ( V_{SW} - V_{BATT} )</td>
<td>80</td>
<td>180</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>CHRG/IADJ Pin Current</td>
<td>( V_{CHRG} = 3V )</td>
<td>45</td>
<td>70</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>( V_{CHRG} = 0V )</td>
<td>0</td>
<td>0.1</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>Switch Leakage Current</td>
<td>( V_{BATT} = V_{SW} = 5V ), In Shutdown</td>
<td>0.01</td>
<td>1</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>CHRG/IADJ Minimum Enable Voltage</td>
<td>●</td>
<td>1.1</td>
<td>V</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
**ELECTRICAL CHARACTERISTICS**  
The *●* denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_{\text{IN}} = V_{\text{BAT}} = V_{\text{CHRG}} = 3\text{V}$ unless otherwise noted (Note 2). Specifications are for the LT3585-0, LT3585-1, LT3585-2, LT3585-3 unless otherwise noted.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>CHRG/IADJ Three-State Voltage for Reduced Input Current</td>
<td>CHRG/IADJ &gt; 1.1V then Float</td>
<td>1.1</td>
<td>1.28</td>
<td>1.4</td>
<td>V</td>
</tr>
<tr>
<td>CHRG/IADJ Voltage Range for Normal Input Current</td>
<td>●</td>
<td>1.6</td>
<td>10</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>CHRG/IADJ Low Voltage</td>
<td>●</td>
<td>0.3</td>
<td>V</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
| Delay Time for Reduced Input Current Mode | CHRG/IADJ Pin Three Stated:  
$V_{\text{BAT}} = 4.2\text{V}$, Fresh Li-Ion Cell  
$V_{\text{BAT}} = 2.8\text{V}$, Dead Li-Ion Cell  
$V_{\text{BAT}} = 3\text{V}$, Fresh 2 AA Cells  
$V_{\text{BAT}} = 2\text{V}$, Dead 2 AA Cells | 5.2 | 7.2 | 6.8 | 9.5 | µs |
| Minimum CHRG/IADJ Pin Low Time | High→Low→High | 20 | µs |
| DONE Output Signal High | 100kΩ from $V_{\text{IN}}$ to DONE | 3 | V |
| DONE Output Signal Low | 33µA into DONE Pin | 120 | 200 | mV |
| DONE Leakage Current | $V_{\text{DONE}} = 3\text{V}$, DONE NPN Off | 1 | 100 | nA |
| IGBT Voltage Range | ● | 2.5 | 10 | V |
| IGBT Input High Level | ● | 1.5 | V |
| IGBT Input Low Level | ● | 0.5 | V |
| IGBT Output Rise Time | IGBTPU Pin, $C_{\text{OUT}} = 4000\text{pF}$, IGBTPWR = 5V, IGBTIN = 0V→1.5V, 10%→90% | 0.4 | µs |
| IGBT Output Fall Time | IGBTPD Pin, $C_{\text{OUT}} = 4000\text{pF}$, IGBTPWR = 5V, IGBTIN = 1.5V→0V, 90%→10% | 0.13 | µs |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime. Ratings are for DC levels only.

**Note 2:** The LT3585 series is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the −40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

**Note 3:** Current limit is guaranteed by design and/or correlation to static test.
TYPICAL PERFORMANCE CHARACTERISTICS

LT3585-0 curves use Figure 11, LT3585-1 curves use Figure 12, LT3585-2 curves use Figure 13 and LT3585-3 curves use Figure 14 unless otherwise noted.

LT3585-0 Charging Waveform
Normal Input Current Mode

LT3585-1 Charging Waveform
Normal Input Current Mode

LT3585-2 Charging Waveform
Normal Input Current Mode

LT3585-3 Charging Waveform
Normal Input Current Mode

LT3585-0 Charging Waveform
Reduced Input Current Mode

LT3585-1 Charging Waveform
Reduced Input Current Mode

LT3585-2 Charging Waveform
Reduced Input Current Mode

LT3585-3 Charging Waveform
Reduced Input Current Mode

Charge Time*
Normal Input Current Mode

*USING RUBYCON 330V, 50µF PHOTOFLASH OUTPUT CAPACITOR (FW SERIES)
Typical Performance Characteristics

LT3585-0 curves use Figure 11, LT3585-1 curves use Figure 12, LT3585-2 curves use Figure 13 and LT3585-3 curves use Figure 14 unless otherwise noted.

Charge Time*
Reduced Input Current Mode

LT3585-0 Input Current
Normal Input Current Mode

LT3585-1 Input Current
Normal Input Current Mode

LT3585-2 Input Current
Normal Input Current Mode

LT3585-3 Input Current
Normal Input Current Mode

LT3585-0 Input Current
Reduced Input Current Mode

LT3585-1 Input Current
Reduced Input Current Mode

LT3585-2 Input Current
Reduced Input Current Mode

LT3585-3 Input Current
Reduced Input Current Mode

*USING RUBYCON 330V, 50µF PHOTOFLASH OUTPUT CAPACITOR (FW SERIES)
**TYPICAL PERFORMANCE CHARACTERISTICS**

LT3585-0 curves use Figure 11, LT3585-1 curves use Figure 12, LT3585-2 curves use Figure 13 and LT3585-3 curves use Figure 14 unless otherwise noted.

**LT3585-0 Efficiency**
Normal Input Current Mode

- **VBAT = 4.2V**
- **VBAT = 3.6V**
- **VBAT = 2.5V**

**LT3585-1 Efficiency**
Normal Input Current Mode

- **VBAT = 4.2V**
- **VBAT = 3.6V**
- **VBAT = 2.5V**

**LT3585-2 Efficiency**
Normal Input Current Mode

- **VBAT = 4.2V**
- **VBAT = 3.6V**
- **VBAT = 2.5V**

**LT3585-3 Efficiency**
Normal Input Current Mode

- **VBAT = 4.2V**
- **VBAT = 3.6V**
- **VBAT = 2.5V**

**LT3585-0 Efficiency**
Reduced Input Current Mode

**LT3585-1 Efficiency**
Reduced Input Current Mode

**LT3585-2 Efficiency**
Reduced Input Current Mode

**LT3585-3 Efficiency**
Reduced Input Current Mode

**LT3585-0 Output Voltage**

- **TA = –40°C**
- **TA = 25°C**
- **TA = 85°C**
TYPICAL PERFORMANCE CHARACTERISTICS

LT3585-0 curves use Figure 11, LT3585-1 curves use Figure 12, LT3585-2 curves use Figure 13 and LT3585-3 curves use Figure 14 unless otherwise noted.

LT3585-0 Switch Waveform
Normal Input Current Mode

LT3585-0 Switch Waveform
Reduced Input Current Mode

LT3585-0 Switch Waveform
Normal Input Current Mode

LT3585-0 Switch Waveform
Reduced Input Current Mode

Switch DC Current Limit*

*DYNAMIC CURRENT LIMIT IS HIGHER THAN DC CURRENT LIMIT

SW PIN IS RESISTIVE UNTIL BREAKDOWN VOLTAGE DUE TO INTEGRATED RESISTORS. THIS DOES NOT INCREASE QUIESCENT CURRENT OF THE PART
PIN FUNCTIONS

IGBTIN (Pin 1): Logic Input for the IGBT Driver. When this pin is driven higher than 1.5V, the output goes high. When the pin is below 0.5V, the output will go low.

IGBTPWR (Pin 2): Supply Pin for the IGBT Driver. Must be locally bypassed with a good quality ceramic capacitor. The minimum operating voltage for the IGBT driver is 2.5V.

GND (Pin 3): Ground. Tie directly to local ground plane.

VIN (Pin 4): Input Supply Pin. Must be locally bypassed with a good quality ceramic capacitor. The minimum operating voltage for VIN is 2.5V.

VBAT (Pin 5): Battery Supply Pin. Must be locally bypassed with a good quality ceramic capacitor. The minimum operating voltage for VBAT is 1.5V.

DONE (Pin 6): Open NPN Collector Indication Pin. When target output voltage is reached, NPN turns on. This pin needs a proper pull-up resistor or current source.

VOUT (Pin 7): Charge and Input Current Adjust Pin. A low (<0.3V) to high (>1.1V) transition on this pin puts the part into power delivery mode. Once the target output voltage is reached, the part will stop charging the output. Toggle this pin to start charging again. Ground to shut down. To enter into the input current reduction mode, the voltage on this pin should be driven high (>1.1V) and then floated. (For more information refer to the Operation section of this data sheet.) To enter normal mode, the voltage should be driven higher than 1.6V.

SW (Pin 8): Switch Pin. This is the collector of the internal NPN Power switch. Minimize the metal trace area connected to this pin to minimize EMI. Tie one side of the primary of the transformer to this pin. The target output voltage is set by the turns ratio of the transformer.

Choose turns ratio N by the following equation:

\[ N = \frac{V_{OUT} + 2}{31.5} \]

where V_OUT is the desired output voltage.

IGBTPD (Pin 9): Pull-down Output for IGBT Gate. Connect this pin to the IGBT Gate. Add a series resistor to increase the turn-off time to protect the IGBT.

IGBTPU (Pin 10): Pull-up Output for IGBT Gate. Connect this pin to the gate of the IGBT.

Exposed Pad (Pin 11): Ground. Tie directly to local ground plane.
SIMPLIFIED BLOCK DIAGRAM

Figure 1
The LT3585 series of parts operate on the edge of discontinuous conduction mode. When CHRG/IADJ is driven higher than 1.1V, the master latch is set. This enables the part to deliver power to the photoflash capacitor. When the power switch, Q1, is turned on, current builds up in the primary of the transformer. When the desired current level is reached, the output of comparator A1 goes high, resetting the switch latch that controls the state of Q1, and the output of the DCM comparator goes low. Q1 now turns off and the flyback waveform on the SW node quickly rises to a level proportional to V_{OUT}. The secondary current flows through high voltage diode(s), D1, and into the photoflash capacitor. When the secondary current decays to zero, the voltage on the SW node collapses. When this voltage reaches 130mV higher than V_{BAT}, the output of A3 goes high. This sets the switch latch and the power switch, Q1, turns back on. This cycle repeats until the target V_{OUT} level is reached. When the target V_{OUT} is reached, the master latch resets and the DONE pin goes low.

The input current of an LT3585 series circuit can be reduced by changing the voltage of the CHRG/IADJ pin. When this pin is between 1.1V and 1.4V, a time delay is added between when A3 goes high and the switch latch is set, see Figure 2. If the part is enabled, and the CHRG/IADJ pin is floated, internal circuitry drives the voltage on the pin to 1.28V. This allows a single I/O port pin, which can be three-stated, to enable or disable the part as well as place the part into the input current reduction mode. This feature effectively reduces the average input current into the flyback transformer. The magnitude of the delay decreases with increasing V_{BAT}. This causes the reduced average input current to remain relatively flat with changes in V_{BAT}. When CHRG/IADJ is brought higher than 1.6V, no delay is added. The CHRG/IADJ pin functionality is shown in Figure 3.

Both V_{BAT} and V_{IN} have undervoltage lockout (UVLO). When one of these pins goes below its UVLO voltage, the DONE pin goes low. With an insufficient bypass capacitor on V_{BAT} or V_{IN}, the ripple on the pin is likely to activate UVLO and terminate the charge. The applications circuits in the data sheet suggest values adequate for most applications.

The LT3585 series also includes an integrated IGBT driver. There are two output pins, IGBTPU and IGBTPD. The IGBTPU pin is used to pull the gate of the IGBT up. This should be done quickly to guarantee proper Xenon lamp ignition. Tie this pin directly to the gate of the IGBT. The IGBTPD pin is pinned out separately to allow for greater flexibility in choosing a series resistor between the pin and the gate of the IGBT. This resistor can be used to slow down the turn off of the IGBT.
Choosing the Right Device
(LT3585-0/LT3585-1/LT3585-2/LT3585-3)

The only difference between the four versions of the LT3585 series is the peak current level. For the fastest possible charge time, use the LT3585-3. The LT3585-1 has the lowest peak current capability, and is designed for applications that need a more limited drain on the batteries. Due to the lower peak current, the LT3585-1 can use a physically smaller transformer. The LT3585-0 and LT3585-2 have a current limit in between that of the LT3585-1 and the LT3585-3.

Transformer Design

The flyback transformer is a key element for any LT3585-0/LT3585-1/LT3585-2/LT3585-3 design. It must be designed carefully and checked that it does not cause excessive current or voltage on any pin of the part. The main parameters that need to be designed are shown in Table 1. The first transformer parameter that needs to be set is the turns ratio, N. The LT3585-0/LT3585-1/LT3585-2/LT3585-3 accomplish output voltage detection by monitoring the flyback waveform on the SW pin. When the SW voltage reaches 31.5V higher than the V_{BAT} voltage, the part halts power delivery. Thus, the choice of N sets the target output voltage and changes the amplitude gain of the reflected voltage from the output to the SW pin. Choose N according to the following equation:

\[
N = \frac{V_{OUT} + 2}{31.5}
\]

where \(V_{OUT}\) is the desired output voltage. The number 2 in the numerator is used to include the forward voltage drop across the output diode(s). Thus, for a 320V output, N should be 322/31.5 or 10.2. For a 300V output, choose N equal to 302/31.5 or 9.6. The next parameter that needs to be set is the primary inductance, \(L_{PRI}\). Choose \(L_{PRI}\) according to the following formula:

\[
L_{PRI} \geq \frac{V_{OUT} \cdot 200 \cdot 10^{-9}}{N \cdot I_{PK}}
\]

where \(V_{OUT}\) is the desired output voltage. N is the transformer turns ratio. \(I_{PK}\) is 1.4 (LT3585-0), 0.7 (LT3585-1), 1 (LT3585-2) and 2 (LT3585-3). \(L_{PRI}\) needs to be equal or larger than this value to ensure that the LT3585 series has adequate time to respond to the flyback waveform. All other parameters need to meet or exceed the recommended limits as shown in Table 1. A particularly important parameter is the leakage inductance, \(L_{LEAK}\). When the power switch of the LT3585 series turns off, the leakage inductance on the primary of the transformer causes a voltage spike to occur on the SW pin. The height of this spike must not exceed 50V, even though the absolute maximum rating of the SW pin is 60V. The 60V absolute maximum rating is a DC blocking voltage specification, which assumes that the current in the power NPN is zero. Figure 4 shows the SW voltage waveform for the circuit of Figure 8 (LT3585-0). Note that the absolute maximum rating of the SW pin is not exceeded. Make sure to check the SW voltage waveform with \(V_{OUT}\) near the target output voltage, as this is the worst-case condition for SW voltage. Figure 5 shows the various limits on the SW voltage during switch turn off.

Table 1. Recommended Transformer Parameters

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>NAME</th>
<th>TYPICAL RANGE LT3585-0</th>
<th>TYPICAL RANGE LT3585-1</th>
<th>TYPICAL RANGE LT3585-2</th>
<th>TYPICAL RANGE LT3585-3</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>(L_{PRI})</td>
<td>Primary Inductance</td>
<td>&gt;5</td>
<td>&gt;10</td>
<td>&gt;7</td>
<td>&gt;3.5</td>
<td>(\mu)H</td>
</tr>
<tr>
<td>(L_{LEAK})</td>
<td>Primary Leakage Inductance</td>
<td>100 to 300</td>
<td>200 to 500</td>
<td>200 to 500</td>
<td>100 to 300</td>
<td>(n)H</td>
</tr>
<tr>
<td>N</td>
<td>Secondary/Primary Turns Ratio</td>
<td>8 to 12</td>
<td>8 to 12</td>
<td>8 to 12</td>
<td>8 to 12</td>
<td></td>
</tr>
<tr>
<td>(V_{ISO})</td>
<td>Secondary to Primary Isolation Voltage</td>
<td>&gt;500</td>
<td>&gt;500</td>
<td>&gt;500</td>
<td>&gt;500</td>
<td>V</td>
</tr>
<tr>
<td>(I_{SAT})</td>
<td>Primary Saturation Current</td>
<td>&gt;1.6</td>
<td>&gt;0.8</td>
<td>&gt;1.0</td>
<td>&gt;2</td>
<td>A</td>
</tr>
<tr>
<td>(R_{PRI})</td>
<td>Primary Winding Resistance</td>
<td>&lt;300</td>
<td>&lt;500</td>
<td>&lt;400</td>
<td>&lt;200</td>
<td>(m)\Omega</td>
</tr>
<tr>
<td>(R_{SEC})</td>
<td>Secondary Winding Resistance</td>
<td>&lt;40</td>
<td>&lt;80</td>
<td>&lt;60</td>
<td>&lt;30</td>
<td>(\Omega)</td>
</tr>
</tbody>
</table>
It is important not to minimize the leakage inductance to a very low level. Although this would result in a very low leakage spike on the SW pin, the parasitic capacitance of the transformer would become large. This will adversely affect the charge time of the photoflash circuit. Linear Technology has worked with several leading magnetic component manufacturers to produce predesigned flyback transformers for use with the LT3585-0/LT3585-1/LT3585-2/LT3585-3. Table 2 shows the details of several of these transformers.

**Output Diode Selection**

The rectifying diode(s) should be low capacitance type with sufficient reverse voltage and forward current ratings. The peak reverse voltage that the diode(s) will see is approximately:

\[ V_{PK(R)} = V_{OUT} + (N \times V_{BAT}) \]

The peak current of the diode is simply:

\[ I_{PK(SEC)} = \frac{2}{N} \quad (LT3585-3) \]

\[ I_{PK(SEC)} = \frac{1.4}{N} \quad (LT3585-0) \]

\[ I_{PK(SEC)} = \frac{1}{N} \quad (LT3585-2) \]

\[ I_{PK(SEC)} = \frac{0.7}{N} \quad (LT3585-1) \]

For the circuit of Figure 8 with \( V_{BAT} \) of 5V, \( V_{PK(R)} \) is 371V and \( I_{PK(SEC)} \) is 137mA. The GSD2004S dual silicon diode is recommended for most applications. Table 3 shows the various diodes and relevant specifications. Use the appropriate number of diodes to achieve the necessary reverse breakdown voltage.

**Capacitor Selection**

For the input bypass capacitors, high quality X5R or X7R types should be used. Make sure the voltage capability of the part is adequate.

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**Table 2. Predesigned Transformers—Typical Specifications Unless Otherwise Noted**

<table>
<thead>
<tr>
<th>FOR USE WITH</th>
<th>TRANSFORMER DESIGNATION</th>
<th>SIZE ((W \times L \times H)) (mm)</th>
<th>LPRI ((\mu H))</th>
<th>LPRI LEAKAGE ((nH))</th>
<th>N</th>
<th>(R_{PRI}) ((\Omega))</th>
<th>(R_{SEC}) ((\Omega))</th>
<th>VENDOR</th>
</tr>
</thead>
<tbody>
<tr>
<td>LT3585-1</td>
<td>SBL-5.6S-1</td>
<td>5.6 x 8.5 x 3.0</td>
<td>24</td>
<td>400 Max</td>
<td>10.2</td>
<td>305</td>
<td>55</td>
<td>Kijima Musen Hong Kong Office</td>
</tr>
<tr>
<td></td>
<td>SBL-5.6-1</td>
<td>5.6 x 8.5 x 4.0</td>
<td>10</td>
<td>200 Max</td>
<td>10.2</td>
<td>103</td>
<td>26</td>
<td>852-2489-8266</td>
</tr>
<tr>
<td>LT3585-0/</td>
<td>LDT565620ST-203</td>
<td>5.8 x 5.8 x 2.0</td>
<td>8.2</td>
<td>390 Max</td>
<td>10.2</td>
<td>370 Max</td>
<td>11.2 Max</td>
<td>TDK</td>
</tr>
<tr>
<td>LT3585-2</td>
<td>LDT565630T-001</td>
<td>5.8 x 5.8 x 3.0</td>
<td>6</td>
<td>200 Max</td>
<td>10.4</td>
<td>100 Max</td>
<td>10 Max</td>
<td>Chicago Sales Office</td>
</tr>
<tr>
<td></td>
<td>LDT565630T-002</td>
<td>5.8 x 5.8 x 3.0</td>
<td>14.5</td>
<td>500 Max</td>
<td>10.2</td>
<td>240 Max</td>
<td>16.5 Max</td>
<td>(847) 803-6100</td>
</tr>
<tr>
<td>LT3585-3</td>
<td>LDT565630T-003</td>
<td>5.8 x 5.8 x 3.0</td>
<td>10.5</td>
<td>550 Max</td>
<td>10.2</td>
<td>210 Max</td>
<td>14 Max</td>
<td><a href="http://www.components.tdk.com">www.components.tdk.com</a></td>
</tr>
<tr>
<td></td>
<td>LDT565630T-041</td>
<td>5.8 x 5.8 x 3.0</td>
<td>4.7</td>
<td>150 Max</td>
<td>10.4</td>
<td>90 Max</td>
<td>6.4 Max</td>
<td>Tokyo Coil Engineering Japan Office</td>
</tr>
<tr>
<td>LT3585-0</td>
<td>TTRN-0530-000-T</td>
<td>5.0 x 5.0 x 3.0</td>
<td>6.6</td>
<td>200 Max</td>
<td>10.3</td>
<td>128 Max</td>
<td>28 Max</td>
<td>Tokyo Coil Engineering Japan Office</td>
</tr>
<tr>
<td>LT3585-1</td>
<td>TTRN-0530-012-T</td>
<td>5.0 x 5.0 x 3.0</td>
<td>16.0</td>
<td>400 Max</td>
<td>10.3</td>
<td>515 Max</td>
<td>32 Max</td>
<td>0426-56-6262</td>
</tr>
<tr>
<td>LT3585-2</td>
<td>TTRN-0530-021-T</td>
<td>5.0 x 5.0 x 3.0</td>
<td>11.8</td>
<td>300 Max</td>
<td>10.3</td>
<td>256 Max</td>
<td>37 Max</td>
<td></td>
</tr>
<tr>
<td>LT3585-3</td>
<td>TTRN-0530-022-T</td>
<td>5.0 x 5.0 x 3.0</td>
<td>4.0</td>
<td>300 Max</td>
<td>10.3</td>
<td>102 Max</td>
<td>16 Max</td>
<td></td>
</tr>
</tbody>
</table>

---

**Figure 4. LT3585 SW Voltage Waveform**

**Figure 5. New Transformer Design Check**
**APPLICATIONS INFORMATION**

![IGBT Drive](Image)

**Figure 6. IGBT Driver Output with 4000pF Load**

**Table 3. Recommended Output Diodes**

<table>
<thead>
<tr>
<th>PART</th>
<th>MAX REVERSE VOLTAGE (V)</th>
<th>MAX CONTINUOUS FORWARD CURRENT (mA)</th>
<th>CAPACITANCE (pF)</th>
<th>VENDOR</th>
</tr>
</thead>
<tbody>
<tr>
<td>GSD2004S (DUAL DIODE)</td>
<td>2 × 300</td>
<td>225</td>
<td>5</td>
<td>Vishay (402) 563-6866 <a href="http://www.vishay.com">www.vishay.com</a></td>
</tr>
<tr>
<td>CMSD2004S (DUAL DIODE)</td>
<td>2 × 300</td>
<td>225</td>
<td>5</td>
<td>Central Semiconductor (631) 435-1110 <a href="http://www.centralsemi.com">www.centralsemi.com</a></td>
</tr>
<tr>
<td>MMBD3004S (DUAL DIODE)</td>
<td>2 × 350</td>
<td>225</td>
<td>5</td>
<td>Diodes, Inc (816) 251-8800 <a href="http://www.diodes.com">www.diodes.com</a></td>
</tr>
</tbody>
</table>

**IGBT Drive**

The IGBT is a high current switch for the 100A+ current through the photoflash lamp. To create a redeye effect or to adjust the light output, the lamp current needs to be stopped or quenched with an IGBT before discharging the photoflash capacitor fully. The IGBT device also controls the 4kV trigger pulse required to ionize the Xenon gas in the photoflash lamp. Figure 8 is a schematic of a fully functional photoflash application with the LT3585-0 serving as the IGBT driver. An IGBT driver charges the gate capacitance to start the flash. The IGBT driver does not need to pull up the gate significantly fast because of the inherently slow nature of the IGBT. A rise time of 2µs is sufficient to charge the gate of the IGBT and create a trigger pulse. With slower rise times, the trigger circuitry will not have a fast enough edge to create the required 4kV pulse. The fall time of the IGBT driver is critical to the safe operation of the IGBT. The IGBT gate is a network of resistors and capacitors, as shown in Figure 9. When the gate terminal is pulled low, the capacitance closest to the terminal goes low but the capacitance further from the terminal remains high. This causes a smaller portion of the device to handle a larger portion of the current, which can damage the device. The pull-down circuitry needs to pull down slower than the internal RC time constant in the gate of the IGBT. This is easily accomplished with a resistor placed in series with the IGBTPD pin.

The LT3585 series integrated IGBT drive circuit is independent of the charging function and draws its power from the IGBTPWR pin. The drive pulls high to within 200mV of IGBTPWR and pulls down to 100mV. The circuit’s switching waveform is shown in Figure 6. The rise and fall times are measured using a 4000pF output capacitor. The typical 10% to 90% rise time is 320ns when IGBTPWR
is 5V and IGBTIN is driven by a 5V signal. The typical 90% to 10% fall time is 125ns but varies with \( R_{PD} \) given by Figure 7. The IGBT driver pulls a peak of 50mA when driving an IGBT with minimal quiescent current. In the low state, an active pull-down network is used during the initial transition but is deactivated after an internal time constant. This allows the IGBT driver’s quiescent current to drop to approximately 0.1\( \mu \)A during idle conditions. The pull-down circuit will clamp the output below 0.8V for currents not exceeding 10mA in its idle state. The pull-up network is always active when the IGBTIN is greater than 1.5V. Table 4 is a list of recommended IGBT devices for strobe applications. These devices are all packaged in 8-lead TSSOP packages unless otherwise noted.

Table 4. Recommended IGBTs

<table>
<thead>
<tr>
<th>PART</th>
<th>DRIVE VOLTAGE (V)</th>
<th>BREAKDOWN VOLTAGE (V)</th>
<th>COLLECTOR CURRENT (PULSED) (A)</th>
<th>VENDOR</th>
</tr>
</thead>
<tbody>
<tr>
<td>CY25CAH-8F*</td>
<td>2.5</td>
<td>400</td>
<td>150</td>
<td>Renesas (408) 382-7500</td>
</tr>
<tr>
<td>CY25CAJ-8F*</td>
<td>4</td>
<td>400</td>
<td>150</td>
<td>Renesas (408) 382-7500</td>
</tr>
<tr>
<td>CY25BAH-8F</td>
<td>2.5</td>
<td>400</td>
<td>150</td>
<td>Renesas (408) 382-7500</td>
</tr>
<tr>
<td>CY25BAJ-8F</td>
<td>4</td>
<td>400</td>
<td>150</td>
<td>Renesas (408) 382-7500</td>
</tr>
<tr>
<td>GT8G133</td>
<td>4</td>
<td>400</td>
<td>150</td>
<td>Toshiba Semiconductor (949) 623-2900 <a href="http://www.semicon.toshiba.co.jp/eng">www.semicon.toshiba.co.jp/eng</a></td>
</tr>
</tbody>
</table>

* Packaged in 8-lead VSON-8 package.

Figure 8. Complete Xenon Circuit

Figure 9. IGBT Gate
APPLICATIONS INFORMATION

Board Layout

The high voltage operation of these parts demand careful attention to board layout. You will not get advertised performance with careless layout. Figure 10 shows the recommended component placement. Keep the area for the high voltage end of the secondary as small as possible. Also note the larger than minimum spacing for all high voltage nodes in order to meet breakdown voltage requirements for the circuit board. It is imperative to keep the electrical path formed by C1, the primary of T1, and the LT3585 series IC as short as possible. If this path is haphazardly made long, it will effectively increase the leakage inductance of T1, which may result in an overvoltage condition on the SW pin. The CHRG/IADJ pin trace should be kept as short as possible while minimizing the adjacent edge with the SW pin trace. This will eliminate false toggling of the CHRG/IADJ pin during sharp transitions on the SW pin. Thermal vias should be added underneath the Exposed Pad, Pin 11, to enhance the LT3585’s thermal performance. These vias should go directly to a large area of ground plane. Acting as a heat sink, the thermal vias/ground plane will lower the device’s operating temperature.

Figure 10. LT3585 Suggested Layout
**TYPICAL APPLICATIONS**

**Figure 11.** LT3585-0 Photoflash Charger Uses High Efficiency 3mm Tall Transformer

- C1: 4.7 µF, 10V, X5R OR X7R
- C2: 0.22 µF, 10V, X5R OR X7R
- COUT: RUBYCON 330V, 50 µF PHOTOFLASH OUTPUT CAPACITOR (FW SERIES)
- D1: VISHAY GSD2004S DUAL DIODE CONNECTED IN SERIES
- R1: PULL-UP RESISTOR NEEDED IF DONE PIN USED
- T1: TDK LTDS65630T-001, Lpri = 6.9 µH, N = 10.4

**Figure 12.** LT3585-1 Photoflash Charger Uses High Efficiency 2mm Tall Transformer

- C1: 4.7 µF, 10V, X5R OR X7R
- C2: 0.22 µ F, 10V, X5R OR X7R
- COUT: RUBYCON 330V, 50 µ F PHOTOFLASH OUTPUT CAPACITOR (FW SERIES)
- D1: VISHAY GSD2004S DUAL DIODE CONNECTED IN SERIES
- R1: PULL-UP RESISTOR NEEDED IF DONE PIN USED
- T1: TDK LTDS65620ST-203, Lpri = 8.2 µH, N = 10.2
Figure 13. LT3585-2 Uses High Efficiency 3mm Tall Transformers

Figure 14. LT3585-3 Uses High Efficiency 3mm Tall Transformers
TYPICAL APPLICATIONS

The LT3585 series can be auto-refreshed using the additional circuitry shown in Figure 15 with its basic operation shown in Figure 16. The ENABLE pin is used to enable or disable the auto-refresh charging mode. Without an auto-refresh circuit, the output voltage will droop due to output capacitor and output diode leakage currents. The circuit in Figure 15 uses the DONE and CHRG/IADJ pins to form an open-loop control scheme. The output voltage target is sensed through the DONE pin with the PFET of U1, Panasonic UP04979 composite transistor. When the DONE pin goes low during the VOUT trip condition, the PFET charges the auto-refresh timing node comprised of R_T and C_T, and in turn, pulls the CHRG/IADJ pin low through a NFET and disables the LT3585 series part. The DONE pin immediately goes high in shutdown, releasing the timing node and allowing the voltage at Pins 2 and 3 to decay. After approximately a R_T C_T time constant, the CHRG/IADJ pin is released and the LT3585 series part is enabled. This cycle is repeated to maintain a constant DC output voltage. The open-loop control method places a constraint on the control loop dominant time constant, \( R_T \cdot C_T \), given by:

\[
R_T C_T > \frac{2 \cdot IPK^2 \cdot L_{PRI}}{I_{LK} \cdot V_{BAT}}
\]

where \( I_{LK} \) is the known leakage current, \( IPK \) is the transformer peak primary current, and \( L_{PRI} \) is the transformer primary inductance. If this condition is not met, a runaway condition could occur. The LT3585 series part would continue to charge the output voltage past the internal output trip voltage. Figure 17 shows the AC ripple of a typical auto-refresh circuit with the proper selection of \( R_T \) and \( C_T \).

![Diagram](image1)

**Figure 15. Auto Refresh Application**

![Graph](image2)

**Figure 16. Auto Refresh Basic Operation**

![Graph](image3)

**Figure 17. VOUT AC Ripple in Auto Refresh Mode**

---

LT3585-0/LT3585-1
LT3585-2/LT3585-3
PACKAGE DESCRIPTION

DDB Package
10-Lead Plastic DFN (3mm × 2mm)
(Reference LTC DWG # 05-08-1722 Rev 0)

RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

NOTE:
1. DRAWING CONFORMS TO VERSION (WECD-1) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE
TYPICAL APPLICATION

Figure 18. LT3585-3 Typical Application

RELATED PARTS

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>LTC®3407</td>
<td>Dual 600mA (I_{OUT}), 1.5MHz, Synchronous Step-Down DC/DC Converter</td>
<td>96% Efficiency, V_{IN}: 2.5V to 5.5V, V_{OUT}: 0.6V to 5V, I_{O} = 40µA, Converter I_{SD} &lt; 1µA, 10-Lead MSE/10-Lead DFN Packages</td>
</tr>
<tr>
<td>LT3420/LT3420-1</td>
<td>1.4A/1A, Photoflash Capacitor Chargers with Charges Automatic Top-Off</td>
<td>Charges 220µF to 320V in 3.7 Seconds from 5V, Automatic Top-Off V_{IN}: 2.2V to 16V, I_{O} = 90µA, I_{SD} &lt; 1µA, 10-Lead MS/10-Lead DFN Packages</td>
</tr>
<tr>
<td>LTC3425</td>
<td>3A (I_{OUT}), 8MHz, 4-Phase Synchronous Step-Up DC/DC Converter</td>
<td>95% Efficiency, V_{IN}: 0.5V to 4.5V, V_{OUT}: 2.4V to 5.25V, I_{O} = 12µA, I_{SD} &lt; 1µA, 32-Lead 5mm × 5mm QFN Package</td>
</tr>
<tr>
<td>LT3440</td>
<td>600mA (I_{OUT}), Synchronous Buck-Boost DC/DC Converter</td>
<td>95% Efficiency, V_{IN}: 2.5V to 5.5V, V_{OUT}: 2.4V to 5.5V, Converter I_{O} = 25µA, I_{SD} &lt; 1µA, 10-Lead MS/10-Lead DFN Packages</td>
</tr>
<tr>
<td>LT3463/LT3463A</td>
<td>Dual Boost (250mA)/Inverting (250mA/400mA) DC/DC Converter for CCD Bias</td>
<td>Integrated Schottkys, V_{IN}: 2.4V to 15V, V_{OUT(MAX)} = ±40V, DC/DC Converter for CCD Bias, I_{O} = 40µA, I_{SD} &lt; 1µA, 10-LeadDFN Package</td>
</tr>
<tr>
<td>LT3468</td>
<td>Photoflash Capacitor Charger in ThinSOT™ Package</td>
<td>Charges 100µF to 320V in 4.6 Seconds from 3.6V, V_{IN}: 2.5V to 16V, I_{O} = 5mA, I_{SD} &lt; 1µA, 5-Lead TSOT-23 Package</td>
</tr>
<tr>
<td>LT3472</td>
<td>Dual ±34V, 1.2MHz Boost (350mA)/Inverting (400mA) DC/DC Converter for CCD Bias</td>
<td>Integrated Schottkys, V_{IN}: 2.2V to 16V, V_{OUT(MAX)} = ±34V, DC/DC Converter for CCD Bias I_{O} = 2.8mA, I_{SD} &lt; 1µA, 10-Lead DFN Package</td>
</tr>
<tr>
<td>LT3484-0/LT3484-1</td>
<td>Photoflash Capacitor Chargers</td>
<td>Charges 100µF to 320V in 4.6 Seconds from 3.6V, LT3484-0 V_{IN}: 2.5V to 16V, V_{BAT}: 1.8V to 16V, I_{O} = 5mA, I_{SD} &lt; 1µA, 6-Lead 2mm × 3mm DFN Package</td>
</tr>
<tr>
<td>LT3485-0/LT3485-1</td>
<td>Photoflash Capacitor Charger with Output Voltage Monitor and Integrated IGBT Drive</td>
<td>Charges 100µF Capacitor to 320V in 2.5 Seconds from 3.6V, V_{IN}: 1.8V to 10V, I_{O} = 5mA, I_{SD} &lt; 1µA, 10-Lead 3mm × 3mm DFN Package</td>
</tr>
</tbody>
</table>

ThinSOT is a trademark of Linear Technology Corporation.