FEATURES

- Dual Synchronous Step-Up DC/DC Converters
- Delivers 3.3V at 200mA/100mA from one Alkaline/NiMH Cell, or 3.3V at 400mA/200mA from Two Cells
- VIN Start-Up Voltage: 700mV
- 0.5V to 5V VIN Range After Start-Up
- 1.6V to 5.25V VOUT Range
- Output Disconnect in Shutdown
- VIN > VOUT Operation
- 1.2MHz or 2.2MHz Operation
- Up to 94% Efficiency
- 12μA Quiescent Current in Burst Mode® Operation
- Inrush Current Limiting and Soft-Start
- Internal Synchronous Rectifiers
- Logic-Controlled Shutdown (< 2μA)
- Quick VOUT Discharge (LTC3527-1)
- 16-Lead, 0.75mm × 3mm × 3mm QFN Package

APPLICATIONS

- MP3/Personal Media Players
- Noise Canceling/Bluetooth Headsets
- Wireless Mice
- Portable Medical Instruments

DESCRIPTION

The LTC®3527/LTC3527-1 are dual high efficiency, step-up DC/DC converters in a space saving 16-lead 3mm × 3mm QFN package. Battery life is maximized with a 700mV start-up voltage and operation down to 500mV once started. The SHDN and PGOOD pins enable the converters to be sequenced or started together.

The LTC3527/LTC3527-1 limit inrush current during start-up. Selectable 1.2MHz or 2.2MHz operation provides a choice between the highest efficiency or smallest solution footprint. The current mode PWM design is internally compensated reducing external parts count. Burst Mode operation or fixed frequency operation is selectable via the MODE pin. Anti-ring circuitry reduces EMI in discontinuous mode. This device also features thermal shutdown.

True output disconnect allows the output to be completely open in shutdown. The LTC3527-1 actively discharges VOUT1 or VOUT2 when its respective SHDN goes low. Quiescent current in shutdown is less than 2μA.
**ABSOLUTE MAXIMUM RATINGS**

(Note 1)

- $V_{IN}$, $V_{IN1}$, $V_{IN2}$ Voltage $\ldots -0.3V$ to $6V$
- SW1, SW2 Voltage (DC) $\ldots -0.3V$ to $6V$ (Pulsed $<100ns$) $\ldots -0.3V$ to $7V$
- SHDN1, SHDN2, FB1, FB2 Voltage $\ldots -0.3V$ to $6V$
- $V_{OUT1}$, $V_{OUT2}$ $\ldots -0.3V$ to $6V$
- MODE, FSEL, PGOOD1, PGOOD2 $\ldots -0.3V$ to $6V$
- Operating Temperature (Notes 2, 5) $\ldots -40°C$ to $85°C$
- Junction Temperature $\ldots 125°C$
- Storage Temperature Range $\ldots -65°C$ to $125°C$

**PIN CONFIGURATION**

**ORDER INFORMATION**

**LEAD FREE FINISH**

<table>
<thead>
<tr>
<th>PART MARKING</th>
<th>PACKAGE DESCRIPTION</th>
<th>TEMPERATURE RANGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>LC3527EUD#PBF</td>
<td>16-Lead (3mm × 3mm) Plastic QFN</td>
<td>–40°C to 85°C</td>
</tr>
<tr>
<td>LC3527EUD-1#PBF</td>
<td>16-Lead (3mm × 3mm) Plastic QFN</td>
<td>–40°C to 85°C</td>
</tr>
</tbody>
</table>

**LEAD BASED FINISH**

<table>
<thead>
<tr>
<th>PART MARKING</th>
<th>PACKAGE DESCRIPTION</th>
<th>TEMPERATURE RANGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>LC3527EUD#TR</td>
<td>16-Lead (3mm × 3mm) Plastic QFN</td>
<td>–40°C to 85°C</td>
</tr>
<tr>
<td>LC3527EUD-1#TR</td>
<td>16-Lead (3mm × 3mm) Plastic QFN</td>
<td>–40°C to 85°C</td>
</tr>
</tbody>
</table>

Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: [http://www.linear.com/leadfree/](http://www.linear.com/leadfree/)

For more information on tape and reel specifications, go to: [http://www.linear.com/tapeandreel/](http://www.linear.com/tapeandreel/)

**ELECTRICAL CHARACTERISTICS**

The $\bullet$ denotes the specifications which apply over the full operating temperature range, $-40°C$ to $85°C$. $V_{IN} = V_{IN1} = V_{IN2} = 1.2V$, $V_{OUT1} = V_{OUT2} = 3.3V$, $T_A = 25°C$, unless otherwise noted.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum Start-Up Voltage</td>
<td>$I_{LOAD} = 1mA$</td>
<td>0.7</td>
<td>0.88</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Output Voltage Adjust Range</td>
<td>$V_{OUT1}$, $V_{OUT2}$</td>
<td>1.7</td>
<td>5.25</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.6</td>
<td>5.25</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.6</td>
<td>5.25</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Line Regulation</td>
<td>$V_{IN} = 1V$ to $5V$</td>
<td>0.005</td>
<td></td>
<td>%/V</td>
<td></td>
</tr>
<tr>
<td>Feedback Voltage FB1, FB2</td>
<td>$V_{FB1,2} = 1.20V$</td>
<td>1.176</td>
<td>1.20</td>
<td>1.224</td>
<td>V</td>
</tr>
<tr>
<td>Feedback Input Current FB1, FB2</td>
<td>$V_{FB1,2} = 1.20V$</td>
<td>1</td>
<td>50</td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>Quiescent Current: Shutdown</td>
<td>$V_{SHDN1} = V_{SHDN2} = 0V$, Not Including Switch Leakage, $V_{OUT1} = V_{OUT2} = 0V$</td>
<td>0.1</td>
<td>2</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>Quiescent Current: Burst Mode Operation</td>
<td>Measured on $V_{OUT}$. $V_{FB1} = V_{FB2} = 1.5V$</td>
<td>12</td>
<td></td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>Quiescent Current: Active</td>
<td>$V_{FB1} = V_{FB2} &gt; 1.2V$ (Note 3)</td>
<td>500</td>
<td>900</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>NMOS Switch Leakage Current (LTC3527)</td>
<td>$V_{SW1,2} = 5V$, SHDN1,2 = 0V</td>
<td>0.1</td>
<td>10</td>
<td></td>
<td>μA</td>
</tr>
</tbody>
</table>
ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, -40°C to 85°C. \( V_{\text{IN}} = V_{\text{IN1}} = V_{\text{IN2}} = 1.2\text{V}, V_{\text{OUT1}} = V_{\text{OUT2}} = 3.3\text{V}, T_A = 25\degree\text{C} \), unless otherwise noted.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMOS Switch Leakage Current (LTC3527)</td>
<td>( V_{SW1,2} = 5\text{V}, V_{OUT1,2} = 0\text{V}, SHDN1,2 = 0\text{V} )</td>
<td>0.1</td>
<td>10</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>NMOS and PMOS Combined Switch Leakage Current (LTC3527-1)</td>
<td>( V_{SW1,2} = 5\text{V}, V_{OUT1,2} = 0\text{V}, SHDN1,2 = 0\text{V} ) (Note 6)</td>
<td>0.2</td>
<td>20</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>NMOS Switch On-Resistance, SW1</td>
<td></td>
<td>0.30</td>
<td></td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>NMOS Switch On-Resistance, SW2</td>
<td></td>
<td>0.50</td>
<td></td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>PMOS Switch On-Resistance, SW1</td>
<td></td>
<td>0.40</td>
<td></td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>PMOS Switch On-Resistance, SW2</td>
<td></td>
<td>0.60</td>
<td></td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>NMOS Current Limit, SW1</td>
<td>●</td>
<td>800</td>
<td></td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>NMOS Current Limit, SW2</td>
<td>●</td>
<td>400</td>
<td></td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Current Limit Delay to Output Time</td>
<td>(Note 4)</td>
<td>60</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Maximum Duty Cycle</td>
<td>( V_{FB1,2} = 1\text{V} )</td>
<td>●</td>
<td>85</td>
<td>90</td>
<td>%</td>
</tr>
<tr>
<td>Minimum Duty Cycle</td>
<td>( V_{FB1,2} = 1.3\text{V} )</td>
<td>●</td>
<td>0</td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>Switching Frequency</td>
<td>( V_{FSEL} = 0\text{V} )</td>
<td>●</td>
<td>0.9</td>
<td>1.2</td>
<td>1.5</td>
</tr>
<tr>
<td>Switching Frequency</td>
<td>( V_{FSEL} = 3.3\text{V} )</td>
<td>●</td>
<td>1.8</td>
<td>2.2</td>
<td>2.8</td>
</tr>
<tr>
<td>SHDN1,2 Input High Voltage</td>
<td></td>
<td>0.88</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>SHDN1,2 Input Low Voltage</td>
<td></td>
<td>0.35</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>SHDN1,2 Input Current</td>
<td>( V_{SHDN1,2} = 3.3\text{V} )</td>
<td>1</td>
<td>2</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>PGOOD1, PGOOD2 Threshold</td>
<td>Referenced to the Feedback Voltage</td>
<td>–6</td>
<td>–9</td>
<td>–14</td>
<td>%</td>
</tr>
<tr>
<td>PGOOD1, PGOOD2 Low Voltage</td>
<td>( I_{PGOOD1,2} = 1\text{mA} )</td>
<td>0.1</td>
<td>0.2</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>PGOOD1, PGOOD2 Leakage Current</td>
<td>( V_{PGOOD1,2} = 5.25\text{V} )</td>
<td>0.01</td>
<td>1</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>MODE Input High Voltage</td>
<td></td>
<td>1</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>MODE Input Low Voltage</td>
<td></td>
<td>0.35</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>MODE Input Current</td>
<td>( V_{MODE} = 3.3\text{V} )</td>
<td>1</td>
<td>2</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>FSEL Input High Voltage</td>
<td></td>
<td>0.88</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>FSEL Input Low Voltage</td>
<td></td>
<td>0.35</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>FSEL Input Current</td>
<td>( V_{FSEL} = 3.3\text{V} )</td>
<td>1</td>
<td>2</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>Soft-Start Time</td>
<td></td>
<td>0.5</td>
<td></td>
<td>ms</td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LTC3527/LTC3527E-1 are guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the -40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

**Note 3:** Current is measured into the VOUT pin since the supply current is bootstrapped to the output. The current will reflect to the input supply by: \( V_{\text{OUT}}/V_{\text{IN}} \) • (1/Efficiency). All switches are off.

**Note 4:** Specification is guaranteed by design and not 100% tested in production.

**Note 5:** The LTC3527/LTC3527-1 includes an overtemperature shutdown that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when the over-temperature shutdown is active. Continuous operation above the specified maximum junction temperature may impair device reliability.

**Note 6:** The NMOS and PMOS switch leakage currents are tested in parallel for the LTC3527-1 because \( V_{\text{OUT1,2}} \) are actively pulled to ground when \( SHDN1,2 = 0\text{V} \).
TYPICAL PERFORMANCE CHARACTERISTICS

(T_A = 25°C, unless otherwise noted)

Efficiency vs Load Current and V_IN for V_OUT1 = 1.8V at 1.2MHz

Efficiency vs Load Current and V_IN for V_OUT2 = 1.8V at 1.2MHz

Efficiency vs Load Current and V_IN for V_OUT1 = 3.3V at 1.2MHz

Efficiency vs Load Current and V_IN for V_OUT2 = 3.3V at 1.2MHz

Efficiency vs Load Current and V_IN for V_OUT1 = 5V at 1.2MHz

Efficiency vs Load Current and V_IN for V_OUT2 = 5V at 1.2MHz
TYPICAL PERFORMANCE CHARACTERISTICS  (TA = 25°C, unless otherwise noted)

**Current Limit vs Temperature**

**Feedback Voltage vs Temperature**

**Start-Up Voltage vs Temperature**

**Burst Mode Quiescent Current vs VOUT**

**RDS(ON) (NMOS and PMOS) vs VOUT**

**RDS(ON) (NMOS and PMOS) Change vs Temperature**

**Fixed Frequency Switching Waveform and VOUT Ripple**

**Burst Mode Waveforms**
TYPICAL PERFORMANCE CHARACTERISTICS

(TA = 25°C, unless otherwise noted)

VOUT and IIN During Start-Up

VOUT1 Load Step Response
Burst Mode Operation at 1.2MHz

VOUT1 = 3.3V
COUT1 = 10μF

VIN = 3.6V
VOUT1 = 5V

20mA TO 170mA STEP
COUT1 = 10μF

VOUT1 = 5V Load Regulation

VIN = 2.4V
L = 3.3μH
MODE = HIGH

VOUT1 = 5V Load Regulation

VIN = 2.4V
L = 3.3μH
MODE = HIGH

VOUT2 Load Step Response
Fixed Frequency at 2.2MHz

VIN = 3.6V
VOUT2 = 5V

50mA TO 100mA STEP
COUT2 = 10μF

VOUT2 = 3.3V Load Regulation

VIN = 2.4V

L = 3.3μH
MODE = HIGH

VOUT2 CHANGE (%)

ILOAD2 (mA)

VOUT CHANGE (%)

ILOAD1 (mA)
PIN FUNCTIONS

SHDN1 (Pin 1): Boost Converter 1 Logic-Controlled Shutdown Input. There is an internal 4MΩ pull-down on this pin.

- SHDN1 = High: Normal free running operation, 1.2MHz/2.2MHz typical operating frequency.
- SHDN1 = Low: Shutdown, quiescent current < 2μA.

Note: Both converters must be shut down together to achieve < 2μA quiescent current.

FB1 (Pin 2): Boost Converter 1 Feedback Input to the gm Error Amplifier. Connect resistor divider tap to this pin. The output voltage can be adjusted from 1.6V to 5.25V by:

\[ V_{OUT1} = 1.20V \cdot \left[ 1 + \frac{R1}{R2} \right] \] (See Block Diagram)

MODE (Pin 3): Logic-Controlled Mode Input for Both Boost Converters.

- MODE = High: Fixed frequency operation
- MODE = Low: Automatic Burst Mode operation

MODE pin must be 1V or greater to ensure fixed frequency over all operating conditions.

VOUT1 (Pin 5): Boost Converter 1 Output Voltage Sense Input and Drain of the Internal Synchronous Rectifier MOSFET. Driver bias is derived from VOUT1. PCB trace length from VOUT1 to the output filter capacitor(s) should be as short and wide as possible.

SW1 (Pin 6): Boost Converter 1 Switch Pin. Connect the inductor between SW1 and VIN1. Keep these PCB trace lengths as short and wide as possible to reduce EMI and voltage overshoot. If the inductor current falls to zero or SHDN1 is low, an internal 100Ω anti-ringing switch is connected from SW1 to VIN1 to minimize EMI.

SW2 (Pin 7): Boost Converter 2 Switch Pin. Connect the inductor between SW2 and VIN2. Keep these PCB trace lengths as short and wide as possible to reduce EMI and voltage overshoot. If the inductor current falls to zero or SHDN2 is low, an internal 100Ω anti-ringing switch is connected from SW2 to VIN2 to minimize EMI.

VOUT2 (Pin 8): Boost Converter 2 Output Voltage Sense Input and Drain of the Internal Synchronous Rectifier MOSFET. Driver bias is derived from VOUT2. PCB trace length from VOUT2 to the output filter capacitor(s) should be as short and wide as possible.

FSEL (Pin 10): Logic-Controlled Frequency Select Input.

- FSEL = High: 2.2MHz operation
- FSEL = Low: 1.2MHz operation

FB2 (Pin 11): Boost Converter 2 Feedback Input to the gm Error Amplifier. Connect resistor divider tap to this pin. The output voltage can be adjusted from 1.6V to 5.25V by:

\[ V_{OUT2} = 1.20V \cdot \left[ 1 + \frac{R3}{R4} \right] \] (See Block Diagram)

SHDN2 (Pin 12): Boost Converter 2 Logic-Controlled Shutdown Input. There is an internal 4MΩ pull-down on this pin.

- SHDN2 = High: Normal free-running operation, 1.2MHz/2.2MHz typical operating frequency.
- SHDN2 = Low: Shutdown, quiescent current < 2μA.

Note: Both converters must be shut down together to achieve < 2μA quiescent current.

PGOOD2 (Pin 13): Boost Converter 2 Power Good Comparator Output. This open-drain output is low when VFB is 9% below its regulation voltage.

GND (Pin 14): Signal Ground. This pin is used as a ground reference for the internal circuitry of the LTC3527/LTC3527-1.

V\text{IN}, V\text{IN1}, V\text{IN2} (Pins 15, 4, 9): Battery Input Voltage. See Operation section for more information.

PGOOD1 (Pin 16): Boost Converter 1 Power Good Comparator Output. This open-drain output is low when VFB is 9% below its regulation voltage.

PGND (Exposed Pad Pin 17): Backplane. The exposed pad is PGND and must be soldered to the PCB ground plane. It serves as the power ground connection for VOUT1 and VOUT2, and as a means of conducting heat away from the package.
OPERATION (Refer to Block Diagram)

The LTC3527/LTC3527-1 are dual 1.2MHz/2.2MHz synchronous boost converters housed in a 16-lead 3mm × 3mm QFN package. With the ability to start up and operate from inputs less than 880mV, these devices feature fixed frequency, current mode PWM control for exceptional line and load regulation. The current mode architecture with adaptive slope compensation provides excellent transient load response, requiring minimal output filtering. Internal soft-start and loop compensation simplifies the design process while minimizing the number of external components. Each converter has a separate input supply pin and is operated independently of the other, but they share the same oscillator thus providing in-phase switching. If different input supply voltages are used, the third V_{IN} pin must be wired to the higher of the two supplies and each V_{OUT} must be higher than the highest V_{IN}. Bypass capacitors are recommended on all V_{IN} pins.

With low R_{DS(ON)} and low gate charge internal N-channel MOSFET switches and P-channel MOSFET synchronous rectifiers, the LTC3527/LTC3527-1 achieve high efficiency over a wide range of load current. With the MODE pin low, automatic Burst Mode operation maintains high efficiency at very light loads, reducing the quiescent current to just 12μA. If MODE is high, fixed frequency PWM switching provides low voltage ripple on the outputs. Operation can be best understood by referring to the Block Diagram.

A PGOOD signal is provided independently for each converter which can be used with the SHDN pins to provide sequencing of the outputs.

The LTC3527-1 provides an instant off feature which discharges V_{OUT1} or V_{OUT2} when their respective SHDN pins go low.

A frequency select function allows for 1.2MHz switching (FSEL = Low) or 2.2MHz switching (FSEL = High).

Low Voltage Start-Up

The LTC3527/LTC3527-1 include an independent start-up oscillator designed to start up at an input voltage of 0.7V (typical). The two converters can be started together or in either sequence of boost 1 and boost 2 with appropriate control of SHDN1 and SHDN2. Soft-start and inrush current limiting are provided to each converter independently during start-up, as well as during normal mode. When V_{IN}, V_{OUT1}, or V_{OUT2} exceeds 1.4V (typical), the IC enters normal operating mode. Once the higher of V_{OUT1} or V_{OUT2} exceeds V_{IN} by 0.24V, the IC powers itself from the higher V_{OUT} instead of V_{IN}. At this point the internal circuitry has no dependency on the V_{IN} input voltage, eliminating the requirement for a large input capacitor. The input voltage can drop as low as 0.5V.

With single-cell operation, the limiting factor for the application becomes the availability of the power source to supply sufficient energy to the outputs at low voltages, and maximum duty cycle, which is clamped at 90% (typical). Note that at low input voltages, small voltage drops due to the higher series resistance of a depleted cell become critical and greatly limit the power delivery capability of the converter. A higher value, low ESR input capacitor can help to improve this to a small degree.

Low Noise Fixed Frequency Operation

Soft-Start: The LTC3527/LTC3527-1 contain internal circuitry to provide independent soft-start operation to each converter. The soft-start circuitry ramps the peak inductor current from zero to its peak value of 900mA (typical) for converter 1 or 500mA (typical) for converter 2 in approximately 0.5ms, allowing start-up into heavy loads. The soft-start circuitry for both converters is reset in the event of a thermal shutdown or shutdown command.

Oscillator: An internal oscillator sets the switching frequency to 1.2MHz if the FSEL pin is below 0.35V, or 2.2MHz if the FSEL pin is above 0.88V.

Shutdown: Shutdown is accomplished independently for each converter by pulling its respective SHDN pin below 0.35V, and enabled by pulling each SHDN pin above 0.88V. Note that the SHDN pins can be driven above V_{IN} or V_{OUT}, as long as it is limited to less than the absolute maximum rating.

Error Amplifier: The noninverting input of each transconductance error amplifier is internally connected to the 1.20V reference. The inverting inputs are connected
to FB1 for converter 1 and FB2 for converter 2. Clamps limit the minimum and maximum error amp output voltages for improved large-signal transient response. Power converter control loop compensation is provided internally. An external resistive voltage divider from $V_{OUT1}$ ($V_{OUT2}$) to ground programs the respective output voltage via FB1 (FB2) from 1.6V to 5.25V.

$$\begin{align*}
V_{OUT1} &= 1.20V \cdot \left[1 + \frac{R1}{R2}\right] \\
V_{OUT2} &= 1.20V \cdot \left[1 + \frac{R3}{R4}\right] \\
\text{(See Block Diagram)}
\end{align*}$$

Current Sensing: Lossless current sensing converts the peak current signal of each N-channel MOSFET switch into a voltage which is summed with its corresponding internal slope compensation. The summed signals are compared to their respective error amplifier outputs to provide individual peak current control commands for the PWM of each converter.

Current Limit: The current limit comparators shut off the N-channel MOSFET switches once their threshold is reached. Each current limit comparator delay time to output is typically 60ns. Peak switch current is limited to approximately 900mA for converter 1 and 500mA for converter 2, independent of input or output voltage. If $V_{OUT1}$ or $V_{OUT2}$ falls below 1V, its respective current limit is cut in half.

Zero Current Comparator: The zero current comparators monitor the inductor current to the outputs and shut off the synchronous rectifiers when the current reduces to approximately 30mA. This prevents the inductor current from reversing in polarity, improving efficiency at light loads.

Synchronous Rectifier: To control inrush current and to prevent the inductor currents from running away when $V_{OUT1}$ or $V_{OUT2}$ is close to $V_{IN}$, the P-channel MOSFET synchronous rectifiers are only enabled when their respective $V_{OUT} > (V_{IN} + 0.24V)$.

Anti-Ringing Control: The anti-ringing control connects a resistor across the inductor to prevent high frequency ringing on the SW1 (SW2) pins during discontinuous current mode operation. Although the ringing of the resonant circuit formed by the inductors and $C_{SW}$ (capacitance on SW1 or SW2 pins) is low energy, it can cause EMI radiation.

Output Disconnect: The LTC3527/LTC3527-1 are designed to allow true output disconnect by eliminating body diode conduction of the internal P-channel MOSFET rectifiers. This allows $V_{OUT1}$ and $V_{OUT2}$ to go to zero volts during shutdown, drawing no current from the input source. It also allows for inrush current limiting at turn-on, minimizing surge currents seen by the input supply. Note that to obtain the advantages of output disconnect, there must not be external Schottky diodes connected between the SW1 (SW2) pins and $V_{OUT1}$ ($V_{OUT2}$). The output disconnect feature also allows $V_{OUT1}$ or $V_{OUT2}$ to be pulled high, without any reverse current into a battery on $V_{IN}$.

Thermal Shutdown: If the die temperature exceeds 160°C, the device will go into thermal shutdown. All switches will be turned off and the soft-start capacitors will be discharged. The device will be enabled again when the die temperature drops by about 15°C.

Burst Mode Operation

To realize the efficiency benefits of Burst Mode operation, both $V_{OUT1}$ and $V_{OUT2}$ must be under a light load current condition, if they are both enabled. If one converter is shut down, then Burst Mode operation is enabled on the other converter. With the MODE pin low, the LTC3527/LTC3527-1 will automatically enter Burst Mode operation at light load and return to fixed frequency PWM mode when the load increases. Refer to the Typical Performance Characteristics to see the Output Load Burst Mode Threshold Current vs $V_{IN}$. The load current at which Burst Mode operation is entered can be changed by adjusting the inductor value. Raising the inductor value will lower the load current at which Burst Mode is operation entered.

In Burst Mode operation, the LTC3527/LTC3527-1 still switch at a fixed frequency of 1.2MHz (FSEL = 0) or 2.2MHz (FSEL = 1), using the same error amplifier and loop compensation for peak current mode control. This control method eliminates the output transient when switching between modes. In Burst Mode operation, energy is delivered to the...
# LTC3527/LTC3527-1

## OPERATION

Output until it reaches the nominal regulation value, then the LTC3527/LTC3527-1 transition to sleep mode where the outputs are off and the LTC3527/LTC3527-1 consume only 12μA of quiescent current from the higher of $V_{OUT1}$ or $V_{OUT2}$. When the output voltage droops slightly, switching resumes. This maximizes efficiency at very light loads by minimizing switching and quiescent current losses. Burst Mode output voltage ripple, which is typically 1% peak-to-peak, can be reduced by using more output capacitance (10μF or greater), or with a small capacitor (15pF) connected between $V_{OUT1}$ ($V_{OUT2}$) and FB1 (FB2). If either load current increases, the LTC3527/LTC3527-1 will automatically leave Burst Mode operation. Note that larger output capacitor values may cause this transition to occur at lighter loads. Once the LTC3527/LTC3527-1 have left Burst Mode operation and returned to normal operation, they will remain there until both output loads are reduced below the burst threshold current.

Burst Mode operation is inhibited during start-up and soft-start and until both $V_{OUT1}$ and $V_{OUT2}$ are at least 0.24V greater than $V_{IN}$ if neither channel is in shutdown.

When the MODE pin is high, LTC3527/LTC3527-1 feature continuous PWM fixed frequency operation at 1.2MHz (FSEL = Low) or 2.2MHz (FSEL = High). At very light loads, the LTC3527/LTC3527-1 will exhibit pulse-skipping operation.

**Single Cell to 5V Step-Up Applications**

Due to the high inductor current slew rate in applications boosting to 5V from a single-cell (alkaline, NiCd or NiMH), the LTC3527/LTC3527-1 may not enter Burst Mode operation at input voltages below 1.5V in a 2.2MHz application (FSEL = high). For a single-cell to 5V application requiring Burst Mode 1.2MHz operation, (FSEL = low) is recommended. Refer to the Typical Performance Characteristics for the Burst Mode thresholds for different input and output voltages.

## APPLICATIONS INFORMATION

### $V_{IN} > V_{OUT}$ Operation

The LTC3527/LTC3527-1 will maintain output voltage regulation even when the input voltage is above one or both of the desired output voltages. Note, all $V_{INS}$ must be common to support this mode of operation. Since this mode is less efficient and will dissipate more power in the LTC3527/LTC3527-1, the maximum output current capability is limited in order to maintain an acceptable junction temperature. When operating with $V_{IN} > V_{OUT}$, the power is defined by:

$$P_{OUT} = I_{OUT} \left( (V_{IN} + 1.5) - V_{OUT} \right)$$

To maintain a junction temperature below 125°C, the following formula must be adhered to:

$$(P_{OUT1} + P_{OUT2}) \times 68°C/W = 125 - T_A$$

where $T_A$ is the ambient temperature.

### Short-Circuit Protection

The LTC3527/LTC3527-1 output disconnect feature allows an output short-circuit while maintaining a maximum internally set current limit. The converters also incorporate internal features such as current limit foldback and thermal shutdown for protection from an excessive overload or short circuit. To reduce power dissipation under short-circuit conditions, the peak switch current limit is reduced to 500mA (typical) for converter 1 and 350mA (typical) for converter 2 when $V_{OUT}$ is less than 1V.

### Schottky Diode

Although it is not required, adding a Schottky diode from SW1 (SW2) to $V_{OUT1}$ ($V_{OUT2}$) will improve efficiency by about 2%. Note that this defeats the output disconnect and short-circuit protection features.
APPLICATIONS INFORMATION

PCB Layout Guidelines

The high speed operation of the LTC3527/LTC3527-1 demands careful attention to board layout. A careless layout will result in reduced performance. Figure 1 shows the recommended component placement. A large ground pin copper area will help to lower the die temperature. A multilayer board with a separate ground plane is ideal, but not absolutely necessary.

COMPONENT SELECTION

Inductor Selection

The LTC3527/LTC3527-1 can utilize small surface mount inductors due to their fast 1.2MHz/2.2MHz switching frequencies. Inductor values between 3.3μH and 4.7μH are suitable for most 1.2MHz applications. Inductor values between 1.5μH and 2.2μH are suitable for most 2.2MHz applications. Larger values of inductance will allow slightly greater output current capability (and lower the Burst Mode threshold) by reducing the inductor ripple current. Increasing the inductance above 10μH will increase size while providing little improvement in output current capability.

The minimum inductance value is given by:

\[
L > \frac{V_{IN(MIN)} \cdot (V_{OUT(MAX)} - V_{IN(MIN)})}{f \cdot \text{Ripple} \cdot V_{OUT(MAX)}}
\]

where:

- \(V_{IN(MIN)}\) = Minimum input voltage
- \(V_{OUT(MAX)}\) = Maximum output voltage
- \(f\) = Oscillator frequency (MHz)
- \(\text{Ripple}\) = Allowable inductor current ripple (amps peak-to-peak)

The inductor current ripple is typically set for 20% to 40% of the maximum inductor current. High frequency ferrite core inductor materials reduce frequency dependent power losses compared to cheaper powdered iron types, improving efficiency. The inductor should have low ESR (series resistance of the windings) to reduce the \(I^2R\) power losses, and must be able to support the peak inductor current without saturating. Molded chokes and some chip inductors usually do not have enough core area to support the peak inductor currents of 900mA (500mA) seen on the LTC3527/LTC3527-1. To minimize radiated noise, use shielded inductors. See Table 1 for suggested components and suppliers.
## Table 1. Recommended Inductors

<table>
<thead>
<tr>
<th>VENDOR</th>
<th>PART/STYLE</th>
<th>L (μH)</th>
<th>MAXIMUM CURRENT (mA)</th>
<th>DCR (Ω)</th>
<th>DIMENSIONS L × W × H (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Coilcraft</td>
<td>MSS5131</td>
<td>2.2-10</td>
<td>1900-870</td>
<td>0.023-0.083</td>
<td>5.1 × 5.1 × 1</td>
</tr>
<tr>
<td></td>
<td>MSS4020</td>
<td>3.3-10</td>
<td>1100-540</td>
<td>0.085-0.210</td>
<td>4 × 4 × 2</td>
</tr>
<tr>
<td></td>
<td>ME3220</td>
<td>1-10</td>
<td>3000-780</td>
<td>0.05-0.90</td>
<td>3.2 × 2.5 × 2</td>
</tr>
<tr>
<td>Coiltronics</td>
<td>SD10</td>
<td>1-10</td>
<td>1930-760</td>
<td>0.045-0.289</td>
<td>5.2 × 5.2 × 1</td>
</tr>
<tr>
<td></td>
<td>SD12</td>
<td>1.2-10</td>
<td>2450-818</td>
<td>0.037-0.284</td>
<td>5.2 × 5.2 × 1.2</td>
</tr>
<tr>
<td>FDK</td>
<td>MIP3226D</td>
<td>1.5-6.8</td>
<td>1400-1000</td>
<td>0.07-0.12</td>
<td>3.2 × 2.6 × 1</td>
</tr>
<tr>
<td></td>
<td>MIPF2520D</td>
<td>1.5-4.7</td>
<td>1500-1000</td>
<td>0.07-0.11</td>
<td>2.5 × 2 × 1</td>
</tr>
<tr>
<td>Murata</td>
<td>LQH43C</td>
<td>1-10</td>
<td>1080-650</td>
<td>0.08-0.24</td>
<td>4.5 × 3.2 × 2</td>
</tr>
<tr>
<td></td>
<td>LQH32C</td>
<td>1.4-7</td>
<td>800-650</td>
<td>0.09-0.15</td>
<td>3.2 × 2.5 × 2</td>
</tr>
<tr>
<td>Sumida</td>
<td>CDRH3016</td>
<td>4.7-15</td>
<td>900-450</td>
<td>0.11-0.29</td>
<td>3.8 × 3.8 × 1.8</td>
</tr>
<tr>
<td></td>
<td>CDRH2014</td>
<td>4.7-12</td>
<td>680-420</td>
<td>0.12-0.32</td>
<td>3.2 × 3.2 × 1.5</td>
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<tr>
<td>TDK</td>
<td>VLF3010A</td>
<td>1.5-10</td>
<td>1200-490</td>
<td>0.068-0.58</td>
<td>2.6 × 2.8 × 1</td>
</tr>
<tr>
<td></td>
<td>VLF5012A</td>
<td>2.2-10</td>
<td>1500-800</td>
<td>0.090-0.30</td>
<td>4.5 × 4.7 × 1.2</td>
</tr>
<tr>
<td>Taiyo Yuden</td>
<td>NR3010</td>
<td>4.7-15</td>
<td>750-400</td>
<td>0.19-0.74</td>
<td>3 × 3 × 1</td>
</tr>
<tr>
<td></td>
<td>NR3015</td>
<td>4.7-15</td>
<td>1000-560</td>
<td>0.12-0.36</td>
<td>3 × 3 × 1.5</td>
</tr>
</tbody>
</table>

## Output and Input Capacitor Selection

Low ESR (equivalent series resistance) capacitors should be used to minimize output voltage ripple. Multilayer ceramic capacitors are an excellent choice as they have extremely low ESR and are available in small footprints. A 4.7μF to 10μF output capacitor is sufficient for most applications. Larger values up to 22μF may be used to obtain lower output voltage ripple and improve transient response. X5R and X7R dielectric materials are preferred for their ability to maintain capacitance over wide voltage and temperature ranges. Y5V types should not be used.

The internal loop compensation of the LTC3527/LTC3527-1 is designed to be stable with output capacitor values of 4.7μF or greater. Although ceramic capacitors are recommended, low ESR tantalum capacitors may be used as well.

A small ceramic capacitor in parallel with a larger tantalum capacitor may be used in demanding applications which have large load transients. Another method of improving the transient response is to add a small feedforward capacitor across the top resistor of the feedback divider [from \(V_{OUT1} \) (\(V_{OUT2}\)) to FB1 (FB2)]. A typical value of 15pF will generally suffice.

Low ESR input capacitors reduce input switching noise and reduce the peak current drawn from the battery. It follows that ceramic capacitors are also a good choice for input decoupling and should be located as close as possible to the device. A 2.2μF input capacitor is sufficient for most applications, although larger values may be used without limitations. Table 2 shows a list of several ceramic capacitor manufacturers. Consult the manufacturers directly for detailed information on their selection of ceramic parts.

## Table 2. Capacitor Vendor Information

<table>
<thead>
<tr>
<th>SUPPLIER</th>
<th>PHONE</th>
<th>WEBSITE</th>
</tr>
</thead>
<tbody>
<tr>
<td>AVX</td>
<td>(803) 448-9411</td>
<td><a href="http://www.avxcorporation.com">www.avxcorporation.com</a></td>
</tr>
<tr>
<td>Murata</td>
<td>(714) 852-2001</td>
<td><a href="http://www.murata.com">www.murata.com</a></td>
</tr>
<tr>
<td>Taiyo Yuden</td>
<td>(408) 573-4150</td>
<td><a href="http://www.t-yuden.com">www.t-yuden.com</a></td>
</tr>
<tr>
<td>TDK</td>
<td>(847) 803-6100</td>
<td><a href="http://www.component.tdk.com">www.component.tdk.com</a></td>
</tr>
</tbody>
</table>
TYPICAL APPLICATIONS

1.2MHz, 1-Cell to \( V_{OUT1} = 3V \), \( V_{OUT2} = 1.8V \)

Boost 1 Efficiency

Boost 2 Efficiency

L: SUMIDA CDRH3D164R7
\( C_{IN}, C_{OUT}: TAIYO YUDEN X5R JMK212BJ475MD \)
TYPICAL APPLICATIONS

1.2MHz, 1-Cell to \( V_{OUT1} = 1.8V, V_{OUT2} = 5V \)

Boost 1 Efficiency

Boost 2 Efficiency

L: SUMIDA CDRH3D164R7
\( C_{IN}, C_{OUT} \): TAIYO YUDEN X5R JMK212BJ475MD
TYPICAL APPLICATIONS

2.2MHz, 1-Cell to \( V_{OUT1} = 3.3V \), \( V_{OUT2} = 1.8V \)

Boost 1 Efficiency

Boost 2 Efficiency

L: SUMIDA CDRH3D162R2
\( C_{IN}, C_{OUT} \): TAIYO YUDEN X5R JMK212BJ475MD

LOAD CURRENT (mA) vs EFFICIENCY (%) graph for Boost 1 and Boost 2.
**TYPICAL APPLICATIONS**

1.2MHz, 2-Cell to \( V_{OUT1} = 5V, V_{OUT2} = 3.3V \)

- **Boost 1 Efficiency**
- **Boost 2 Efficiency**

\[ \text{LOAD CURRENT (mA)} \]
\[ \text{EFFICIENCY (%)} \]

1.8V TO 3.2V
ALKALINE CELLS

\[ \text{ON} \]
\[ \text{OFF} \]

\[ V_{OUT} \]
5V
300mA

\[ C_{IN} \]
4.7\( \mu \)F
10\( \mu \)H

\[ C_{OUT1} \]
4.7\( \mu \)F
15pF

\[ C_{OUT2} \]
4.7\( \mu \)F
15pF

\[ V_{IN1} \]
\[ V_{IN2} \]

\[ \text{SHDN1} \]
\[ \text{SHDN2} \]

L: SUMIDA CDRH3D164R7
\( C_{IN}, C_{OUT} \): TAIYO YUDEN X5R JMK212BJ475MD

- LTC3527
- LTC3527-1

**LOAD CURRENT (mA)**

0.01 1 10 100 1000

0.01 1 10 100 1000

**EFFICIENCY (%)**

20 30 40 50 60 70 80 90 100

20 30 40 50 60 70 80 90 100
Sequenced Start-Up $V_{OUT1}$ to $V_{OUT2}$

1.2MHz, 1-Cell to $V_{OUT1} = 1.8V$, $V_{OUT2} = 3.3V$

Boost 1 Efficiency

Boost 2 Efficiency

L: SUMIDA CDRH3D164R7
$C_{IN}, C_{OUT}$: TAIYO YUDEN X5R JMK212BJ475MD

TYPICAL APPLICATIONS
UD Package
16-Lead Plastic QFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1691)

NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WEED-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADIED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE
# Revision History

(Revision history begins at Rev C)

<table>
<thead>
<tr>
<th>REV</th>
<th>DATE</th>
<th>DESCRIPTION</th>
<th>PAGE NUMBER</th>
</tr>
</thead>
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| C   | 11/09| Changes to Typical Applications  
Change to Operation Section  
Changes to Applications Information Section | 1, 15, 16, 17, 18, 19, 12, 14 |
### RELATED PARTS

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>LTC3400/ LTC34008</td>
<td>600mA ISW, 1.2MHz Synchronous Step-Up DC/DC Converters</td>
<td>92% Efficiency, ( V_{IN} ): 0.85V to 5V, ( V_{OUT(MAX)} ) = 5V, ( I_Q ) = 19μA/300μA, ( I_{SD} &lt; 1μA ), ThinSOT™ Package</td>
</tr>
<tr>
<td>LTC3401</td>
<td>1A ISW, 3MHz Synchronous Step-Up DC/DC Converter</td>
<td>97% Efficiency, ( V_{IN} ): 0.5V to 5V, ( V_{OUT(MAX)} ) = 6V, ( I_Q ) = 38μA, ( I_{SD} &lt; 1μA ), 10-Lead MS Package</td>
</tr>
<tr>
<td>LTC3421</td>
<td>3A ISW, 3MHz Synchronous Step-Up DC/DC Converter with Output Disconnect</td>
<td>95% Efficiency, ( V_{IN} ): 0.5V to 4.5V, ( V_{OUT(MAX)} ) = 5.25V, ( I_Q ) = 12μA, ( I_{SD} &lt; 1μA ), QFN-24 Package</td>
</tr>
<tr>
<td>LTC3422</td>
<td>1.5A ISW, 3MHz Synchronous Step-Up DC/DC Converter with Output Disconnect</td>
<td>95% Efficiency, ( V_{IN} ): 0.5V to 4.5V, ( V_{OUT(MAX)} ) = 5.25V, ( I_Q ) = 25μA, ( I_{SD} &lt; 1μA ), 3mm × 3mm DFN Package</td>
</tr>
<tr>
<td>LTC3423/ LTC3424</td>
<td>2A ISW, 3MHz Synchronous Step-Up DC/DC Converter</td>
<td>97% Efficiency, ( V_{IN} ): 0.5V to 5V, ( V_{OUT(MAX)} ) = 6V, ( I_Q ) = 38μA, ( I_{SD} &lt; 1μA ), 10-Lead MS Package</td>
</tr>
<tr>
<td>LTC3426</td>
<td>2A ISW, 1.2MHz Synchronous Step-Up DC/DC Converter</td>
<td>92% Efficiency, ( V_{IN} ): 1.6V to 4.3V, ( V_{OUT(MAX)} ) = 5V, ( I_{SD} &lt; 1μA ), SOT-23 Package</td>
</tr>
<tr>
<td>LTC3428</td>
<td>500mA ISW, 1.25MHz/2.5MHz Synchronous Step-Up DC/DC Converter with Output Disconnect</td>
<td>92% Efficiency, ( V_{IN} ): 1.8V to 5V, ( V_{OUT(MAX)} ) = 5.25V, ( I_{SD} &lt; 1μA ), 2mm × 2mm DFN Package</td>
</tr>
<tr>
<td>LTC3429</td>
<td>600mA ISW, 500kHz Synchronous Step-Up DC/DC Converter with Output Disconnect and Soft-Start</td>
<td>96% Efficiency, ( V_{IN} ): 0.5V to 4.4V, ( V_{OUT(MAX)} ) = 5V, ( I_Q ) = 20μA/300μA, ( I_{SD} &lt; 1μA ), ThinSOT Package</td>
</tr>
<tr>
<td>LTC3458</td>
<td>1.4A ISW, 1.5MHz Synchronous Step-Up DC/DC Converter/ Output Disconnect/Burst Mode Operation</td>
<td>93% Efficiency, ( V_{IN} ): 1.5V to 6V, ( V_{OUT(MAX)} ) = 7.5V, ( I_Q ) = 15μA, ( I_{SD} &lt; 1μA ), DFN-12 Package</td>
</tr>
<tr>
<td>LTC3458L</td>
<td>1.7A ISW, 1.5MHz Synchronous Step-Up DC/DC Converter with Output Disconnect, Automatic Burst Mode Operation</td>
<td>94% Efficiency, ( V_{OUT(MAX)} ) = 6V, ( I_Q ) = 12μA, DFN-12 Package</td>
</tr>
<tr>
<td>LTC3459</td>
<td>70mA ISW, 10V Micropower Synchronous Boost Converter/ Output Disconnect/Burst Mode Operation</td>
<td>( V_{IN} ): 1.5V to 5.5V, ( V_{OUT(MAX)} ) = 10V, ( I_Q ) = 10μA, ( I_{SD} &lt; 1μA ), ThinSOT Package</td>
</tr>
<tr>
<td>LTC3525L-3</td>
<td>500mA ISW, 1.2MHz Synchronous Step-Up DC/DC Converters with Output Disconnect, Automatic Burst Mode Operation</td>
<td>94% Efficiency, ( V_{IN} ): 0.85V to 5V, ( V_{OUT(MAX)} ) = 5.25V, ( I_Q ) = 7μA, ( I_{SD} &lt; 1μA ), SC70 Package</td>
</tr>
<tr>
<td>LTC3526/ LTC3526B</td>
<td>500mA ISW, 1.2MHz Synchronous Step-Up DC/DC Converters with Output Disconnect, Automatic Burst Mode Operation (LTC3526), PWM Only (LTC3526B)</td>
<td>94% Efficiency, ( V_{IN} ): 0.85V to 5V, ( V_{OUT(MAX)} ) = 5.25V, ( I_Q ) = 10μA/300μA, ( I_{SD} &lt; 1μA ), 2mm × 2mm DFN Package</td>
</tr>
<tr>
<td>LTC3528/ LTC3528B</td>
<td>1A, 1MHz Synchronous Step-Up DC/DC Converter with Output Disconnect, Automatic Burst Mode Operation, PWM Only (LTC3528B)</td>
<td>94% Efficiency, ( V_{IN} ): 0.85V to 5V, ( V_{OUT(MAX)} ) = 5.25V, ( I_Q ) = 10μA/300μA, ( I_{SD} &lt; 1μA ), 2mm × 3mm DFN Package</td>
</tr>
</tbody>
</table>