LT3083
Adjustable 3A Single Resistor Low Dropout Regulator

**FEATURES**
- Outputs May be Paralleled for Higher Current and Heat Spreading
- Output Current: 3A
- Single Resistor Programs Output Voltage
- 50µA Set Pin Current: 1% Initial Accuracy
- Output Adjustable to 0V
- Low Output Noise: 40µVRMS (10Hz to 100kHz)
- Wide Input Voltage Range: 1.2V to 23V (DD-Pak and TO-220 Packages)
- Low Dropout Voltage: 310mV
- <1mV Load Regulation
- <0.001%/V Line Regulation
- Minimum Load Current: 1mA
- Stable with Minimum 10µF Ceramic Capacitor
- Current Limit with Foldback and Overtemperature Protection
- Available in 16-Lead TSSOP, 12-Lead 4mm × 4mm DFN, 5-Lead TO-220 and 5-Lead Surface Mount DD-PAK Packages

**APPLICATIONS**
- High Current All Surface Mount Supply
- High Efficiency Linear Regulator
- Post Regulator for Switching Supplies
- Low Parts Count Variable Voltage Supply
- Low Output Voltage Power Supplies

**DESCRIPTION**
The LT®3083 is a 3A low dropout linear regulator that can be paralleled to increase output current or spread heat on surface mounted boards. Architected as a precision current source and voltage follower, this new regulator finds use in many applications requiring high current, adjustability to zero, and no heat sink. The device also brings out the collector of the pass transistor to allow low dropout operation—down to 310mV—when used with multiple supplies.

A key feature of the LT3083 is the capability to supply a wide output voltage range. By using a reference current through a single resistor, the output voltage is programmed to any level between zero and 23V (DD-PAK and TO-220 packages). The LT3083 is stable with 10µF of capacitance on the output, and the IC is stable with small ceramic capacitors that do not require additional ESR as is common with other regulators.

Internal protection circuitry includes current limiting and thermal limiting. The LT3083 is offered in the 16-lead TSSOP (with an exposed pad for better thermal characteristics), 12-lead 4mm × 4mm DFN, 5-Lead TO-220 and 5-Lead Surface Mount DD-PAK packages.

**TYPICAL APPLICATION**

1.5V to 0.9V at 3A Supply (Using 3.3V $V_{\text{CONTROL}}$)

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**Set Pin Current Distribution**

N = 1052

Set Pin Current Distribution (µA)

49 49.5 50 50.5 51
LT3083

**ABSOLUTE MAXIMUM RATINGS**

(Note 1) All Voltages Relative to \( V_{OUT} \)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>CONTROL Pin Voltage</td>
<td>( \pm 28V )</td>
</tr>
<tr>
<td>IN Pin Voltage (T5, Q Packages)</td>
<td>18V, –0.3V</td>
</tr>
<tr>
<td>No Overload or Short-Circuit</td>
<td>23V, –0.3V</td>
</tr>
<tr>
<td>IN Pin Voltage (DF, FE Packages)</td>
<td>8V, –0.3V</td>
</tr>
<tr>
<td>No Overload or Short-Circuit</td>
<td>14V, –0.3V</td>
</tr>
<tr>
<td>SET Pin Current (Note 7)</td>
<td>( \pm 25mA )</td>
</tr>
<tr>
<td>SET Pin Voltage (Relative to OUT)</td>
<td>( \pm 10V )</td>
</tr>
<tr>
<td>Output Short-Circuit Duration</td>
<td>Indefinite</td>
</tr>
<tr>
<td>Operating Junction Temperature Range (Notes 2, 10)</td>
<td>–40°C to 125°C</td>
</tr>
<tr>
<td>E-, I-grades</td>
<td>–55°C to 125°C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>–65°C to 150°C</td>
</tr>
<tr>
<td>Lead Temperature (Soldering, 10 sec)</td>
<td>300°C</td>
</tr>
</tbody>
</table>

**PIN CONFIGURATION**

* TOP VIEW

**DF PACKAGE**

12-LEAD (4mm × 4mm) PLASTIC DFN

\( T_{J_{MAX}} = 125°C, \theta_{JA} = 37°C/W, \theta_{JC} = 8°C/W \)

*Exposed Pad (Pin 13) is OUT, must be soldered to PCB*

**FE PACKAGE**

16-LEAD PLASTIC TSSOP

\( T_{J_{MAX}} = 125°C, \theta_{JA} = 25°C/W, \theta_{JC} = 8°C/W \)

*Exposed Pad (Pin 17) is OUT, must be soldered to PCB*

**Q PACKAGE**

5-LEAD PLASTIC DD-PAK

\( T_{J_{MAX}} = 125°C, \theta_{JA} = 15°C/W, \theta_{JC} = 3°C/W \)

**T PACKAGE**

5-LEAD PLASTIC TO-220

\( T_{J_{MAX}} = 125°C, \theta_{JA} = 40°C/W, \theta_{JC} = 3°C/W \)

**ORDER INFORMATION**

<table>
<thead>
<tr>
<th>LEAD FREE FINISH</th>
<th>TAPE AND REEL</th>
<th>PART MARKING*</th>
<th>PACKAGE DESCRIPTION</th>
<th>TEMPERATURE RANGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>LT3083EDF#PBF</td>
<td>LT3083EDF#TRPBF</td>
<td>3083</td>
<td>12-Lead (4mm × 4mm) Plastic DFN</td>
<td>–40°C to 125°C</td>
</tr>
<tr>
<td>LT3083EFE#PBF</td>
<td>LT3083EFE#TRPBF</td>
<td>3083FE</td>
<td>16-Lead Plastic TSSOP</td>
<td>–40°C to 125°C</td>
</tr>
<tr>
<td>LT3083EQ#PBF</td>
<td>LT3083EQ#TRPBF</td>
<td>LT3083Q</td>
<td>5-Lead Plastic DD-PAK</td>
<td>–40°C to 125°C</td>
</tr>
<tr>
<td>LT3083ET#PBF</td>
<td>LT3083ET#TRPBF</td>
<td>LT3083T</td>
<td>5-Lead Plastic TO-220</td>
<td>–40°C to 125°C</td>
</tr>
<tr>
<td>LT3083IDF#PBF</td>
<td>LT3083IDF#TRPBF</td>
<td>3083</td>
<td>12-Lead (4mm × 4mm) Plastic DFN</td>
<td>–40°C to 125°C</td>
</tr>
<tr>
<td>LT3083IFE#PBF</td>
<td>LT3083IFE#TRPBF</td>
<td>3083FE</td>
<td>16-Lead Plastic TSSOP</td>
<td>–40°C to 125°C</td>
</tr>
</tbody>
</table>
## ORDER INFORMATION

<table>
<thead>
<tr>
<th>LT3083</th>
<th>TAPE AND REEL</th>
<th>PART MARKING*</th>
<th>PACKAGE DESCRIPTION</th>
<th>TEMPERATURE RANGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>LT3083IQ#PBF</td>
<td>LT3083IQ#TRPBF</td>
<td>LT3083Q</td>
<td>5-Lead Plastic DD-PAK</td>
<td>–40°C to 125°C</td>
</tr>
<tr>
<td>LT3083IT#PBF</td>
<td>LT3083IT#TRPBF</td>
<td>LT3083T</td>
<td>5-Lead Plastic TO-220</td>
<td>–40°C to 125°C</td>
</tr>
<tr>
<td>LT3083MPDF#PBF</td>
<td>LT3083MPDF#TRPBF</td>
<td>LT3083Q</td>
<td>5-Lead Plastic DD-PAK</td>
<td>–55°C to 125°C</td>
</tr>
<tr>
<td>LT3083MPFE#PBF</td>
<td>LT3083MPFE#TRPBF</td>
<td>LT3083Q</td>
<td>5-Lead Plastic TO-220</td>
<td>–55°C to 125°C</td>
</tr>
<tr>
<td>LT3083MPT#PBF</td>
<td>LT3083MPT#TRPBF</td>
<td>LT3083Q</td>
<td>5-Lead Plastic DD-PAK</td>
<td>–55°C to 125°C</td>
</tr>
</tbody>
</table>

### LEAD BASED FINISH

<table>
<thead>
<tr>
<th>LT3083</th>
<th>TAPE AND REEL</th>
<th>PART MARKING*</th>
<th>PACKAGE DESCRIPTION</th>
<th>TEMPERATURE RANGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>LT3083EDF</td>
<td>LT3083EDF#TR</td>
<td>LT3083Q</td>
<td>5-Lead Plastic DD-PAK</td>
<td>–40°C to 125°C</td>
</tr>
<tr>
<td>LT3083FE</td>
<td>LT3083FE#TR</td>
<td>LT3083Q</td>
<td>5-Lead Plastic DD-PAK</td>
<td>–40°C to 125°C</td>
</tr>
<tr>
<td>LT3083ET</td>
<td>LT3083ET#TR</td>
<td>LT3083Q</td>
<td>5-Lead Plastic DD-PAK</td>
<td>–40°C to 125°C</td>
</tr>
<tr>
<td>LT3083IDF</td>
<td>LT3083IDF#TR</td>
<td>LT3083Q</td>
<td>5-Lead Plastic DD-PAK</td>
<td>–40°C to 125°C</td>
</tr>
<tr>
<td>LT3083IQ</td>
<td>LT3083IQ#TR</td>
<td>LT3083Q</td>
<td>5-Lead Plastic DD-PAK</td>
<td>–40°C to 125°C</td>
</tr>
<tr>
<td>LT3083IT</td>
<td>LT3083IT#TR</td>
<td>LT3083Q</td>
<td>5-Lead Plastic DD-PAK</td>
<td>–40°C to 125°C</td>
</tr>
<tr>
<td>LT3083MPDF</td>
<td>LT3083MPDF#TR</td>
<td>LT3083Q</td>
<td>5-Lead Plastic DD-PAK</td>
<td>–55°C to 125°C</td>
</tr>
<tr>
<td>LT3083MPFE</td>
<td>LT3083MPFE#TR</td>
<td>LT3083Q</td>
<td>5-Lead Plastic DD-PAK</td>
<td>–55°C to 125°C</td>
</tr>
<tr>
<td>LT3083MPT</td>
<td>LT3083MPT#TR</td>
<td>LT3083Q</td>
<td>5-Lead Plastic DD-PAK</td>
<td>–55°C to 125°C</td>
</tr>
</tbody>
</table>

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: [http://www.linear.com/leadfree/](http://www.linear.com/leadfree/)
For more information on tape and reel specifications, go to: [http://www.linear.com/tapeandreel/](http://www.linear.com/tapeandreel/)

## ELECTRICAL CHARACTERISTICS

The **denotes the specifications which apply over the full operating temperature range, otherwise specifications are at TA = 25°C (Note 2).

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>SET Pin Current</td>
<td>$I_{SET}$</td>
<td>$V_{IN} = 1V, V_{CONTROL} = 2V, I_{LOAD} = 1mA, T_J = 25°C$</td>
<td>49.5</td>
<td>50</td>
<td>50.5</td>
</tr>
<tr>
<td>Output Offset Voltage ($V_{OUT} – V_{SET}$)</td>
<td>$V_{OS}$</td>
<td>DF, FE Packages</td>
<td>–3</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>T, Q Packages</td>
<td>–4</td>
<td>0</td>
<td>4</td>
</tr>
<tr>
<td>Load Regulation (DF, FE Packages)</td>
<td>$\Delta I_{SET}$</td>
<td>$\Delta I_{LOAD} = 1mA to 3A$</td>
<td>–10</td>
<td>–0.4</td>
<td>–1</td>
</tr>
<tr>
<td></td>
<td>$\Delta V_{OS}$</td>
<td>$\Delta I_{LOAD} = 5mA to 3A$ (Note 8)</td>
<td>–10</td>
<td>–0.7</td>
<td>–4</td>
</tr>
<tr>
<td>Load Regulation (T, Q Packages)</td>
<td>$\Delta I_{SET}$</td>
<td>$\Delta I_{LOAD} = 1mA to 3A$</td>
<td>–10</td>
<td>–0.4</td>
<td>–1</td>
</tr>
<tr>
<td></td>
<td>$\Delta V_{OS}$</td>
<td>$\Delta I_{LOAD} = 5mA to 3A$ (Note 8)</td>
<td>–10</td>
<td>–0.7</td>
<td>–4</td>
</tr>
<tr>
<td>Line Regulation (DF, FE Packages)</td>
<td>$\Delta I_{SET}$</td>
<td>$\Delta V_{IN} = 1V to 14V, \Delta V_{CONTROL} = 2V to 25V, I_{LOAD} = 1mA$</td>
<td>0.1</td>
<td>0.002</td>
<td>0.01</td>
</tr>
<tr>
<td></td>
<td>$\Delta V_{OS}$</td>
<td>$\Delta V_{IN} = 1V to 14V, \Delta V_{CONTROL} = 2V to 25V, I_{LOAD} = 1mA$</td>
<td>0.1</td>
<td>0.002</td>
<td>0.01</td>
</tr>
<tr>
<td>Line Regulation (T, Q Packages)</td>
<td>$\Delta I_{SET}$</td>
<td>$\Delta V_{IN} = 1V to 23V, \Delta V_{CONTROL} = 2V to 25V, I_{LOAD} = 1mA$</td>
<td>0.1</td>
<td>0.002</td>
<td>0.01</td>
</tr>
<tr>
<td></td>
<td>$\Delta V_{OS}$</td>
<td>$\Delta V_{IN} = 1V to 23V, \Delta V_{CONTROL} = 2V to 25V, I_{LOAD} = 1mA$</td>
<td>0.1</td>
<td>0.002</td>
<td>0.01</td>
</tr>
<tr>
<td>Minimum Load Current (Notes 3, 9)</td>
<td></td>
<td>$V_{IN} = 1V, V_{CONTROL} = 2V$</td>
<td>350</td>
<td>500</td>
<td>1</td>
</tr>
</tbody>
</table>
The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$ (Note 2).

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{\text{CONTROL}}$ Dropout Voltage (Note 4)</td>
<td>$I_{\text{LOAD}} = 100\text{mA}$</td>
<td>1.2</td>
<td>1.22</td>
<td>1.55</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$I_{\text{LOAD}} = 1\text{A}$</td>
<td>●</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$I_{\text{LOAD}} = 3\text{A}$</td>
<td>●</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$I_{\text{LOAD}} = 100\text{mA}$</td>
<td>10</td>
<td>25</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>$V_{\text{IN}}$ Dropout Voltage (Note 4)</td>
<td>$I_{\text{LOAD}} = 1\text{A}$, Q, T Packages</td>
<td>120</td>
<td>190</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$I_{\text{LOAD}} = 1\text{A}$, DF, FE Packages</td>
<td>90</td>
<td>160</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$I_{\text{LOAD}} = 3\text{A}$, Q, T Packages</td>
<td>310</td>
<td>510</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$I_{\text{LOAD}} = 3\text{A}$, DF, FE Packages</td>
<td>240</td>
<td>420</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>$V_{\text{CONTROL}}$ Pin Current (Note 5)</td>
<td>$I_{\text{LOAD}} = 100\text{mA}$</td>
<td>5.5</td>
<td>10</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$I_{\text{LOAD}} = 1\text{A}$</td>
<td>●</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$I_{\text{LOAD}} = 3\text{A}$</td>
<td>●</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current Limit</td>
<td>$V_{\text{IN}} = 5\text{V}$, $V_{\text{CONTROL}} = 5\text{V}$, $V_{\text{SET}} = 0\text{V}$, $V_{\text{OUT}} = –0.1\text{V}$</td>
<td>3</td>
<td>3.7</td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>Error Amplifier RMS Output Noise (Note 6)</td>
<td>$I_{\text{LOAD}} = 500\text{mA}$, $10\text{Hz} \leq f \leq 100\text{kHz}$, $C_{\text{OUT}} = 10\mu\text{F}$, $C_{\text{SET}} = 0.1\mu\text{F}$</td>
<td>40</td>
<td></td>
<td>$\mu\text{VRMS}$</td>
<td></td>
</tr>
<tr>
<td>Reference Current RMS Output Noise (Note 6)</td>
<td>$10\text{Hz} \leq f \leq 100\text{kHz}$</td>
<td>1</td>
<td></td>
<td>$\text{nARMS}$</td>
<td></td>
</tr>
<tr>
<td>Ripple Rejection</td>
<td>$V_{\text{RIPPLE}} = 0.5\text{V}<em>{\text{P-P}}$, $I_L = 0.1\text{A}$, $C</em>{\text{SET}} = 0.1\mu\text{F}$, $C_{\text{OUT}} = 10\mu\text{F}$</td>
<td>85</td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$f = 1\text{kHz}$</td>
<td>75</td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$f = 1\text{MHz}$</td>
<td>20</td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>Thermal Regulation, $I_{\text{SET}}$</td>
<td>10ms Pulse</td>
<td>0.003</td>
<td></td>
<td>%/W</td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** Unless otherwise specified, all voltages are with respect to $V_{\text{OUT}}$. The LT3083 is tested and specified under pulse load conditions such that $T_J = T_A$. The LT3083E is 100% tested at $T_A = 25^\circ\text{C}$. Performance of the LT3083E over the full $–40^\circ\text{C}$ to $125^\circ\text{C}$ operating junction temperature range is assured by design, characterization, and correlation with statistical process controls. The LT3083I regulators are guaranteed over the $–40^\circ\text{C}$ to $125^\circ\text{C}$ operating junction temperature range. The LT3083MP is 100% tested and guaranteed over the $–55^\circ\text{C}$ to $125^\circ\text{C}$ operating junction temperature range.

**Note 3:** Minimum load current is equivalent to the quiescent current of the part. Since all quiescent and drive current is delivered to the output of the part, the minimum load current is the minimum current required to maintain regulation.

**Note 4:** For the LT3083, dropout is caused by either minimum control voltage ($V_{\text{CONTROL}}$) or minimum input voltage ($V_{\text{IN}}$). Both parameters are specified with respect to the output voltage. The specifications represent the minimum input-to-output differential voltage required to maintain regulation.

**Note 5:** The $V_{\text{CONTROL}}$ pin current is the drive current required for the output transistor. This current will track output current with roughly a 1:60 ratio. The minimum value is equal to the quiescent current of the device.

**Note 6:** Output noise is lowered by adding a small capacitor across the voltage setting resistor. Adding this capacitor bypasses the voltage setting resistor shot noise and reference current noise; output noise is then equal to error amplifier noise (see the Applications Information section).

**Note 7:** The SET pin is clamped to the output with diodes through 1k resistors. These resistors and diodes will only carry current under transient overloads.

**Note 8:** Load regulation is Kelvin sensed at the package.

**Note 9:** Current limit includes foldback protection circuitry. Current limit decreases at higher input-to-output differential voltages.

**Note 10:** This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed the maximum operating junction temperature when overtemperature protection is active. Overtemperature protection (thermal limit) is typically active at junction temperatures of 165°C. Continuous operation above the specified maximum operating junction temperature may impair device reliability.
TYPICAL PERFORMANCE CHARACTERISTICS  \( T_A = 25^\circ C, \) unless otherwise noted.
TYPICAL PERFORMANCE CHARACTERISTICS  \( T_A = 25^\circ C \), unless otherwise noted.

 Dropout Voltage, FE/DF Packages

 Dropout Voltage, T/Q Packages (Minimum IN Voltage)

 Dropout Voltage, FE/DF Packages (Minimum IN Voltage)

 Dropout Voltage (Minimum \( V_{\text{CONTROL}} \) Pin Voltage)

 Dropout Voltage (Minimum \( V_{\text{CONTROL}} \) Pin Voltage)

 Current Limit

 Current Limit

 TA = 25°C, unless otherwise noted.
### TYPICAL PERFORMANCE CHARACTERISTICS

**T<sub>A</sub> = 25°C, unless otherwise noted.**

#### V<sub>CONTROL</sub> Pin Current

<table>
<thead>
<tr>
<th>LOAD CURRENT (A)</th>
<th>OUTPUT VOLTAGE DEVIATION (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0.5</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1.5</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
</tr>
</tbody>
</table>

#### Residual Output Voltage with Less Than Minimum Load

<table>
<thead>
<tr>
<th>SET PIN = 0V</th>
<th>V&lt;sub&gt;IN&lt;/sub&gt; = 10V</th>
<th>V&lt;sub&gt;IN&lt;/sub&gt; = 5V</th>
</tr>
</thead>
<tbody>
<tr>
<td>R&lt;sub&gt;TEST&lt;/sub&gt; &lt; 1k</td>
<td>ADD 1N4148 FOR</td>
<td>V&lt;sub&gt;OUT&lt;/sub&gt;</td>
</tr>
</tbody>
</table>

#### Line Transient Response

<table>
<thead>
<tr>
<th>LOAD CURRENT (A)</th>
<th>OUTPUT VOLTAGE DEVIATION (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0.5</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1.5</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
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</tbody>
</table>

#### Turn-On Response

<table>
<thead>
<tr>
<th>LOAD CURRENT (A)</th>
<th>OUTPUT VOLTAGE DEVIATION (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0.5</td>
<td>0</td>
</tr>
<tr>
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<tr>
<td>1.5</td>
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</tr>
<tr>
<td>2</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
</tr>
</tbody>
</table>

#### V<sub>IN</sub> = 2V | V<sub>CONTROL</sub> = 3V | V<sub>OUT</sub> = 1V | C<sub>SET</sub> = 0.1µF | C<sub>OUT</sub> = 22µF CERAMIC

### Ta = 25°C

#### Time (µs)

<table>
<thead>
<tr>
<th>LOAD CURRENT (A)</th>
<th>OUTPUT VOLTAGE DEVIATION (mV)</th>
</tr>
</thead>
<tbody>
<tr>
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</tr>
<tr>
<td>0.5</td>
<td>0</td>
</tr>
<tr>
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<tr>
<td>2</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
</tr>
</tbody>
</table>

#### Time (ms)

<table>
<thead>
<tr>
<th>LOAD CURRENT (A)</th>
<th>OUTPUT VOLTAGE DEVIATION (mV)</th>
</tr>
</thead>
<tbody>
<tr>
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<tr>
<td>0.5</td>
<td>0</td>
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<tr>
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<tr>
<td>2</td>
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<tr>
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</table>

### Ta = –50°C

#### Time (µs)

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<th>LOAD CURRENT (A)</th>
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</tr>
</thead>
<tbody>
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<tr>
<td>2</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
</tr>
</tbody>
</table>

### Ta = 125°C

#### Time (µs)

<table>
<thead>
<tr>
<th>LOAD CURRENT (A)</th>
<th>OUTPUT VOLTAGE DEVIATION (mV)</th>
</tr>
</thead>
<tbody>
<tr>
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<tr>
<td>0.5</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1.5</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
</tr>
</tbody>
</table>
**TYPICAL PERFORMANCE CHARACTERISTICS**  \( T_A = 25^\circ C, \) unless otherwise noted.

### Ripple Rejection, Single Supply

- **C\text{OUT} = 10\mu F CERAMIC**
- **C\text{SET} = 0.1\mu F CERAMIC**
- **RipPLE = 50m\text{V}_{p-p}**
- **V\text{IN} – V\text{CONTROL} = V\text{OUT(NOMINAL)} + 2V**

### Ripple Rejection, Dual Supply, V\text{CONTROL Pin}

- **C\text{OUT} = 10\mu F CERAMIC**
- **C\text{SET} = 0.1\mu F CERAMIC**
- **V\text{IN} = V\text{OUT(NOMINAL)} + 1V**
- **V\text{CONTROL} = V\text{OUT(NOMINAL)} + 2V**

### Ripple Rejection, Dual Supply, IN Pin

- **C\text{OUT} = 10\mu F CERAMIC**
- **C\text{SET} = 0.1\mu F CERAMIC**
- **V\text{IN} = V\text{OUT(NOMINAL)} + 1V**
- **V\text{CONTROL} = V\text{OUT(NOMINAL)} + 2V**

### Ripple Rejection (120Hz)

- **V\text{IN} = V\text{CONTROL} = V\text{OUT(NOMINAL)} + 2V**
- **Ripple = 500m\text{V}_{p-p}, f = 120Hz**
- **I\text{LOAD} = 0.5A**
- **C\text{SET} = 0.1\mu F, C\text{OUT} = 10\mu F**

### Noise Spectral Density

- **Reference Current Noise Spectral Density (pA/\sqrt{Hz})**
- **Reference Voltage Noise Spectral Density (nV/\sqrt{Hz})**

### Output Voltage Noise

- **V\text{OUT} = 1V, R\text{SET} = 20k**
- **C\text{SET} = 0.1\mu F, C\text{OUT} = 10\mu F**
- **I\text{LOAD} = 3A**

### Error Amplifier Gain and Phase

- **Gain (dB)**
**PIN FUNCTIONS (DF/FE/Q/T Packages)**

**OUT (Pins 1-5, 13/Pins 1-6, 8, 9, 16, 17/Pin 3, Tab/Pin 3, Tab):** Output. The exposed pad of the DF package (Pin 13) and the FE package (Pin 17) and the Tab of the DD-PAK and TO-220 packages is an electrical connection to OUT. Connect the exposed pad of the DF and FE packages and the Tab of the DD-PAK package directly to OUT on the PCB and the respective OUT pins for each package. There must be a minimum load current of 1mA or the output may not regulate.

**SET (Pin 6/Pin 7/Pin 2/Pin 2):** Set Point. This pin is the non-inverting input to the error amplifier and the regulation set point. A fixed current of 50μA flows out of this pin through a single external resistor, which programs the output voltage of the device. Output voltage range is zero to the $V_{\text{IN(MAX)}} - V_{\text{DROPOUT}}$. Transient performance can be improved by adding a small capacitor from the SET pin to ground.

**VCONTROL (Pins 7, 8/Pins 10, 11/Pin 4/Pin 4):** Bias Supply. This is the supply pin for the control circuitry of the device. Minimum input capacitance is 2.2μF (see Input Capacitance and Stability in the Applications Information section). The current flow into this pin is about 1.7% of the output current. For the device to regulate, this voltage must be more than 1.2V to 1.4V greater than the output voltage (see dropout specifications in the Electrical Characteristics section).

**IN (Pins 9-12/Pins 12-15/Pin 5/Pin 5):** Power Input. This is the collector to the power device of the LT3083. The output load current is supplied through this pin. Minimum IN capacitance is 10μF (see Input Capacitance and Stability in Applications Information section). For the device to regulate, the voltage at this pin must be more than 0.1V to 0.5V greater than the output voltage (see dropout specifications in the Electrical Characteristics section).

**NC (NA/NA/Pin 1/Pin 1):** No Connection. No Connect pins have no connection to internal circuitry and may be tied to $V_{\text{IN}}, V_{\text{CONTROL}}, V_{\text{OUT}}, GND$, or floated.

---

**BLOCK DIAGRAM**

[Diagram of LT3083 block diagram]
The LT3083 regulator is easy to use and has all the protection features expected in high performance regulators. Included are short-circuit protection and safe operating area protection, as well as thermal shutdown with hysteresis.

The LT3083 fits well in applications needing multiple rails. This new architecture adjusts down to zero with a single resistor, handling modern low voltage digital IC’s as well as allowing easy parallel operation and thermal management without heat sinks. Adjusting to zero output allows shutting off the powered circuitry. When the input is pre-regulated, such as with a 5V or 3.3V input supply, external resistors can help spread the heat.

A precision “0” TC 50μA reference current source connects to the noninverting input of a power operational amplifier. The power operational amplifier provides a low impedance buffered output to the voltage on the noninverting input. A single resistor from the noninverting input to ground sets the output voltage. If this resistor is set to 0Ω, zero output voltage results. Therefore, any output voltage can be obtained between zero and the maximum defined by the input power supply.

The benefit of using a true internal current source as the reference, as opposed to a bootstrapped reference in older regulators, is not so obvious in this architecture. A true reference current source allows the regulator to have gain and frequency response independent of the impedance on the positive input. On older adjustable regulators, such as the LT1086, loop gain changes with output voltage and bandwidth changes if the adjustment pin is bypassed to ground. For the LT3083, the loop gain is unchanged with output voltage changes or bypassing. Output regulation is not a fixed percentage of output voltage, but is a fixed fraction of millivolts. Use of a true current source allows all of the gain in the buffer amplifier to provide regulation, and none of that gain is needed to amplify up the reference to a higher output voltage.

The LT3083 has the collector of the output transistor connected to a separate pin from the control input. Since the dropout on the collector (IN pin) is typically only 310mV, two supplies can be used to power the LT3083 to reduce dissipation: a higher voltage supply for the control circuitry and a lower voltage supply for the collector. This increases efficiency and reduces dissipation. To further spread the heat, a resistor inserted in series with the collector moves some of the heat out of the IC to spread it on the PC board (see the section Reducing Power Dissipation).

The LT3083 can be operated in two modes. Three terminal mode has the VCONTROL pin connected to the IN pin and gives a limitation of 1.25V dropout. Alternatively, the VCONTROL pin is separately tied to a higher voltage and the IN pin to a lower voltage giving 310mV dropout on the IN pin, minimizing total power dissipation. This allows for a 3A supply regulating from 2.5VIN to 1.8VOUT or 1.8VIN to 1.2VOUT with low power dissipation.

Programming Output Voltage

The LT3083 sources a 50μA reference current that flows out of the SET pin. Connecting a resistor from SET to ground generates a voltage that becomes the reference point for the error amplifier (see Figure 1). The reference voltage equals 50μA multiplied by the value of the SET pin resistor. Any voltage can be generated and there is no minimum output voltage for the regulator.

![Figure 1. Basic Adjustable Regulator](image-url)
APPLICATIONS INFORMATION

Table 1 lists many common output voltages and the closest standard 1% resistor values used to generate that output voltage.

Regulation of the output voltage requires a minimum load current of 1mA. For a true zero voltage output operation, return this 1mA load current to a negative supply voltage.

Table 1. 1% Resistors for Common Output Voltages

<table>
<thead>
<tr>
<th>VOUT (V)</th>
<th>RSET (k)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>20</td>
</tr>
<tr>
<td>1.2</td>
<td>24.3</td>
</tr>
<tr>
<td>1.5</td>
<td>30.1</td>
</tr>
<tr>
<td>1.8</td>
<td>35.7</td>
</tr>
<tr>
<td>2.5</td>
<td>49.9</td>
</tr>
<tr>
<td>3.3</td>
<td>66.5</td>
</tr>
<tr>
<td>5</td>
<td>100</td>
</tr>
</tbody>
</table>

With the lower level current used to generate the reference voltage, leakage paths to or from the SET pin can create errors in the reference and output voltages. High quality insulation should be used (e.g., Teflon, Kel-F); cleaning of all insulating surfaces to remove fluxes and other residues will probably be required. Surface coating may be necessary to provide a moisture barrier in high humidity environments.

Minimize board leakage by encircling the SET pin and circuitry with a guard ring operated at a potential close to itself. Tie the guard ring to the OUT pin. Guard rings on both sides of the circuit board are required. Bulk leakage reduction depends on the guard ring width. 50nA of leakage into or out of the SET pin and its associated circuitry creates a 0.1% reference voltage error. Leakages of this magnitude, coupled with other sources of leakage, can cause significant offset voltage and reference drift, especially over the possible operating temperature range. Figure 2 depicts an example of a guard ring layout.

If guard ring techniques are used, this bootstraps any stray capacitance at the SET pin. Since the SET pin is a high impedance node, unwanted signals may couple into the SET pin and cause erratic behavior. This will be most noticeable when operating with minimum output capacitors at full load current. The easiest way to remedy this is to bypass the SET pin with a small amount of capacitance from SET to ground, 10pF to 20pF is sufficient.

Stability and Input Capacitance

Typical minimum input capacitance is 10µF for IN and 2.2µF for VCONTROL. These amounts of capacitance work well using low ESR ceramic capacitors when placed close to the LT3083 and the circuit is located in close proximity to the power source. Higher values of input capacitance may be necessary to maintain stability depending on the application.

Oscillating regulator circuits are often viewed as a problem of phase margin and inadequate stability with the output capacitor used. More and more frequently, the problem is not the regulator operating without sufficient output capacitance, but instead with too little input capacitance. The entire circuit must be analyzed and debugged as a whole; conditions relating to the input of the regulator cannot be ignored.

The LT3083 input presents a high impedance to its power source: the output voltage and load current are independent of input voltage variations. To maintain stability of the regulator circuit as a whole, the LT3083 must be powered from a low impedance supply. When using short supply lines or powering directly from a large switching supply, there is no issue—hundreds or thousands of microfarads of capacitance are available through a low impedance.
APPLICATIONS INFORMATION

When longer supply lines, filters, current sense resistors, or other impedances exist between the supply and the input to the LT3083, input bypassing should be reviewed if stability concerns are seen. Just as output capacitance supplies the instantaneous changes in load current for output transients until the regulator is able to respond, input capacitance supplies local power to the regulator until the main supply responds. When impedance separates the LT3083 from its main supply, the local input can droop so that the output follows. The entire circuit may break into oscillations, usually characterized by larger amplitude oscillations on the input and coupling to the output.

Low ESR, ceramic input bypass capacitors are acceptable for applications without long input leads. However, applications connecting a power supply to an LT3083 circuit’s IN and GND pins with long input wires combined with low ESR, ceramic input capacitors are prone to voltage spikes, reliability concerns and application-specific board oscillations. The input wire inductance found in many battery powered applications, combined with the low ESR ceramic input capacitor, forms a high-Q LC resonant tank circuit. In some instances this resonant frequency beats against the output current dependent LDO bandwidth and interferes with proper operation. Simple circuit modifications/solutions are then required. This behavior is not indicative of LT3083 instability, but is a common ceramic input bypass capacitor application issue.

The self-inductance, or isolated inductance, of a wire is directly proportional to its length. Wire diameter is not a major factor on its self-inductance. For example, the self-inductance of a 2-AWG isolated wire (diameter = 0.26”) is about half the self-inductance of a 30-AWG wire (diameter = 0.01”). One foot of 30-AWG wire has about 465nH of self-inductance.

One of two ways reduces a wire’s self-inductance. One method divides the current flowing towards the LT3083 between two parallel conductors. In this case, the farther apart the wires are from each other, the more the self-inductance is reduced; up to a 50% reduction when placed a few inches apart. Splitting the wires basically connects two equal inductors in parallel, but placing them in close proximity gives the wires mutual inductance adding to the self-inductance. The second and most effective way to reduce overall inductance is to place both forward and return current conductors (the input and GND wires) in very close proximity. Two 30-AWG wires separated by only 0.02”, used as forward- and return- current conductors, reduce the overall self-inductance to approximately one-fifth that of a single isolated wire.

If wiring modifications are not permissible for the applications, including series resistance between the power supply and the input of the LT3083 also stabilizes the application. As little as 0.1Ω to 0.5Ω, often less, is effective in damping the LC resonance. If the added impedance between the power supply and the input is unacceptable, adding ESR to the input capacitor also provides the necessary damping of the LC resonance. However, the required ESR is generally higher than the series impedance required.

Stability and Output Capacitance

The LT3083 requires an output capacitor for stability. It is designed to be stable with most low ESR capacitors (typically ceramic, tantalum or low ESR electrolytic). A minimum output capacitor of 10μF with an ESR of 0.5Ω or less is recommended to prevent oscillations. Larger values of output capacitance decrease peak deviations and provide improved transient response for larger load current changes. Bypass capacitors, used to decouple individual components powered by the LT3083, increase the effective output capacitor value. For improvement in transient performance, place a capacitor across the voltage setting resistor. Capacitors up to 1μF can be used. This bypass capacitor reduces system noise as well, but start-up time is proportional to the time constant of the voltage setting resistor (R\text{SET} in Figure 1) and SET pin bypass capacitor.

Give extra consideration to the use of ceramic capacitors. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior across temperature and applied voltage. The most common dielectrics used are specified with EIA temperature characteristic codes of Z5U, Y5V, X5R and X7R. The Z5U and Y5V dielectrics are good for providing high capacitances in a small package, but they tend to have strong voltage and temperature coefficients as shown in Figures 3 and 4. When used with a 5V regulator, a 16V 10μF Y5V capacitor can exhibit an
effective value as low as 1μF to 2μF for the DC bias voltage applied and over the operating temperature range. The X5R and X7R dielectrics result in more stable characteristics and are more suitable for use as the output capacitor. The X7R type has better stability across temperature, while the X5R is less expensive and is available in higher values. Care still must be exercised when using X5R and X7R capacitors. The X5R and X7R codes only specify operating temperature range and maximum capacitance change over temperature. Capacitance change due to DC bias with X5R and X7R capacitors is better than Y5V and Z5U capacitors, but can still be significant enough to drop capacitor values below appropriate levels. Capacitor DC bias characteristics tend to improve as component case size increases, but expected capacitance at operating voltage should be verified.

Voltage and temperature coefficients are not the only sources of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates voltage across its terminals due to mechanical stress. In a ceramic capacitor, the stress can be induced by vibrations in the system or thermal transients.

**Paralleling Devices**

Higher output current is obtained by paralleling multiple LT3083s together. Tie the individual SET pins together and tie the individual IN pins together. Connect the outputs in common using small pieces of PC trace as ballast resistors to promote equal current sharing. PC trace resistance in mΩ/inch is shown in Table 2. Ballasting requires only a tiny area on the PCB.

<table>
<thead>
<tr>
<th>WEIGHT (oz)</th>
<th>10mil WIDTH</th>
<th>20mil WIDTH</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>54.3</td>
<td>27.1</td>
</tr>
<tr>
<td>2</td>
<td>27.1</td>
<td>13.6</td>
</tr>
</tbody>
</table>

Trace resistance is measured in mΩ/in

The worst-case room temperature offset, only ±4mV (DD-PAK, T Packages) between the SET pin and the OUT pin, allows the use of very small ballast resistors.

As shown in Figure 5, each LT3083 has a small 10mΩ ballast resistor, which at full output current gives better than 80% equalized sharing of the current. The external
resistance of 10mΩ (5mΩ for the two devices in parallel) only adds about 30mV of output regulation drop at an output of 6A. With an output voltage of 3.3V, this only adds 1% to the regulation. Of course, paralleling more than two LT3083s yields even higher output current. Spreading the devices on the PC board also spreads the heat. Series input resistors can further spread the heat if the input-to-output difference is high.

Quieting the Noise

The LT3083 offers numerous noise performance advantages. Every linear regulator has its sources of noise. In general, a linear regulator's critical noise source is the reference. In addition, consider the error amplifier's noise contribution along with the resistor divider's noise gain.

Many traditional low noise regulators bond out the voltage reference to an external pin (usually through a large value resistor) to allow for bypassing and noise reduction. The LT3083 does not use a traditional voltage reference like other linear regulators. Instead, it uses a 50µA reference current. The 50µA current source generates noise current levels of 3.16pA/√Hz (1nA RMS) over the 10Hz to 100kHz bandwidth). The equivalent voltage noise equals the RMS noise current multiplied by the resistor value.

The SET pin resistor generates spot noise equal to √4kTR (k = Boltzmann’s constant, 1.38 • 10^{-23} J/°K, and T is absolute temperature) which is RMS summed with the voltage noise. If the application requires lower noise performance, bypass the voltage setting resistor with a capacitor to GND. Note that this noise-reduction capacitor increases start-up time as a factor of the RC time constant.

The LT3083 uses a unity-gain follower from the SET pin to the OUT pin. Therefore, multiple possibilities exist (besides a SET pin resistor) to set output voltage. For example, using a high accuracy voltage reference from SET to GND removes the errors in output voltage due to reference current tolerance and resistor tolerance. Active driving of the SET pin is acceptable.

The typical noise scenario for a linear regulator is that the output voltage setting resistor divider gains up the noise reference, especially if V_{OUT} is much greater than V_{REF}.

The LT3083’s noise advantage is that the unity gain follower presents no noise gain whatsoever from the SET pin to the output. Thus, noise figures do not increase accordingly. Error amplifier noise is typically 126.5nV/√Hz (40µVRMS) over the 10Hz to 100kHz bandwidth). The error amplifier’s noise is RMS summed with the other noise terms to give a final noise figure for the regulator.

Curves in the Typical Performance Characteristics section show noise spectral density and peak-to-peak noise characteristics for both the reference current and error amplifier over the 10Hz to 100kHz bandwidth.

Load Regulation

The LT3083 is a floating device. No ground pin exists on the packages. Thus, the IC delivers all quiescent current and drive current to the load. Therefore, it is not possible to provide true remote load sensing. The connection resistance between the regulator and the load determines load regulation performance. The data sheet’s load regulation specification is Kelvin sensed at the package’s pins. Negative-side sensing is a true Kelvin connection by returning the bottom of the voltage setting resistor to the negative side of the load (see Figure 6).

Connected as shown, system load regulation is the sum of the LT3083’s load regulation and the parasitic line resistance multiplied by the output current. To minimize load regulation, keep the positive connection between the regulator and load as short as possible. If possible, use large diameter wire or wide PC board traces.
APPLICATIONS INFORMATION

Thermal Considerations

The LT3083’s internal power and thermal limiting circuitry protects itself under overload conditions. For continuous normal load conditions, do not exceed the 125°C maximum junction temperature. Carefully consider all sources of thermal resistance from junction-to-ambient. This includes (but is not limited to) junction-to-case, case-to-heat sink interface, heat sink resistance or circuit board-to-ambient as the application dictates. Consider all additional, adjacent heat generating sources in proximity on the PCB.

Surface mount packages provide the necessary heat sinking by using the heat spreading capabilities of the PC board, copper traces, and planes. Surface mount heat sinks, plated through-holes and solder-filled vias can also spread the heat generated by power devices.

Junction-to-case thermal resistance is specified from the IC junction to the bottom of the case directly, or the bottom of the pin most directly in the heat path. This is the lowest thermal resistance path for heat flow. Only proper device mounting ensures the best possible thermal flow from this area of the packages to the heat sinking material.

Note that the exposed pad of the DFN and TSSOP packages and the tab of the DD-PAK and TO-220 packages are electrically connected to the output (V\text{OUT}).

Tables 3 through 5 list thermal resistance as a function of copper areas on a fixed board size. All measurements were taken in still air on a 4-layer FR-4 board with 1oz solid internal planes and 2oz external trace planes with a total finished board thickness of 1.6mm. Layers are not connected electrically or thermally.

Calculating Junction Temperature

Example: Given an output voltage of 0.9V, a V\text{CONTROL} voltage of 3.3V ±10%, an IN voltage of 1.5V ±5%, output current range from 10mA to 3A and a maximum ambient temperature of 50°C, what will the maximum junction temperature be for the DD-PAK on a 2500mm² board with topside copper of 1000mm²?

<table>
<thead>
<tr>
<th>TOPSIDE</th>
<th>BACKSIDE</th>
<th>BOARD AREA</th>
<th>THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2500mm²</td>
<td>2500mm²</td>
<td>2500mm²</td>
<td>18°C/W</td>
</tr>
<tr>
<td>1000mm²</td>
<td>2500mm²</td>
<td>2500mm²</td>
<td>22°C/W</td>
</tr>
<tr>
<td>225mm²</td>
<td>2500mm²</td>
<td>2500mm²</td>
<td>29°C/W</td>
</tr>
<tr>
<td>100mm²</td>
<td>2500mm²</td>
<td>2500mm²</td>
<td>35°C/W</td>
</tr>
</tbody>
</table>

*Device is mounted on topside.

<table>
<thead>
<tr>
<th>COPPER AREA</th>
</tr>
</thead>
<tbody>
<tr>
<td>TOPSIDE*</td>
</tr>
<tr>
<td>BACKSIDE</td>
</tr>
<tr>
<td>BOARD AREA</td>
</tr>
<tr>
<td>THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)</td>
</tr>
<tr>
<td>-------------</td>
</tr>
<tr>
<td>2500mm²</td>
</tr>
<tr>
<td>2500mm²</td>
</tr>
<tr>
<td>2500mm²</td>
</tr>
<tr>
<td>16°C/W</td>
</tr>
<tr>
<td>20°C/W</td>
</tr>
<tr>
<td>26°C/W</td>
</tr>
<tr>
<td>32°C/W</td>
</tr>
</tbody>
</table>

*Device is mounted on topside.
The power in the drive circuit equals:

\[ P_{\text{DRIVE}} = (V_{\text{CONTROL}} - V_{\text{OUT}})(I_{\text{CONTROL}}) \]

where \( I_{\text{CONTROL}} \) is equal to \( I_{\text{OUT}}/60 \). \( I_{\text{CONTROL}} \) is a function of output current. A curve of \( I_{\text{CONTROL}} \) vs \( I_{\text{OUT}} \) can be found in the Typical Performance Characteristics curves.

The total power equals:

\[ P_{\text{TOTAL}} = P_{\text{DRIVE}} + P_{\text{OUTPUT}} \]

The current delivered to the SET pin is negligible and can be ignored.

\[ V_{\text{CONTROL}}(\text{MAX\_CONTINUOUS}) = 3.630V \ (3.3V + 10\%) \]
\[ V_{\text{IN}}(\text{MAX\_CONTINUOUS}) = 1.575V \ (1.5V + 5\%) \]
\[ V_{\text{OUT}} = 0.9V, \ I_{\text{OUT}} = 3A, \ TA = 50^\circ C \]

Power dissipation under these conditions is equal to:

\[ P_{\text{DRIVE}} = (V_{\text{CONTROL}} - V_{\text{OUT}})(I_{\text{CONTROL}}) \]
\[ I_{\text{CONTROL}} = \frac{I_{\text{OUT}}}{60} = \frac{3A}{60} = 50mA \]
\[ P_{\text{DRIVE}} = (3.630V - 0.9V)(50mA) = 137mW \]
\[ P_{\text{OUTPUT}} = (V_{\text{IN}} - V_{\text{OUT}})(I_{\text{OUT}}) \]
\[ P_{\text{OUTPUT}} = (1.575V - 0.9V)(3A) = 2.03W \]

Total Power Dissipation = 2.16W

Junction Temperature will be equal to:

\[ T_J = T_A + P_{\text{TOTAL}} \cdot \theta_{JA} \ (\text{using tables}) \]
\[ T_J = 50^\circ C + 2.16W \cdot 16^\circ C/W = 84.6^\circ C \]

In this case, the junction temperature is below the maximum rating, ensuring reliable operation.

**Reducing Power Dissipation**

In some applications it may be necessary to reduce the power dissipation in the LT3083 package without sacrificing output current capability. Two techniques are available. The first technique, illustrated in Figure 7, employs a resistor in series with the regulator’s input. The voltage drop across \( R_S \) decreases the LT3083’s input-to-output differential voltage and correspondingly decreases the LT3083’s power dissipation.

As an example, assume: \( V_{\text{IN}} = V_{\text{CONTROL}} = 5V, V_{\text{OUT}} = 3.3V \) and \( I_{\text{OUT}}(\text{MAX}) = 2A \). Use the formulas from the Calculating Junction Temperature section previously discussed.

Without series resistor \( R_S \), power dissipation in the LT3083 equals:

\[ P_{\text{TOTAL}} = (5V - 3.3V) \cdot \left(\frac{2A}{60}\right) + (5V - 3.3V) \cdot 2A = 3.46W \]

If the voltage differential \( V_{\text{DIFF}} \) across the NPN pass transistor is chosen as 0.5V, then \( R_S \) equals:

\[ R_S = \frac{5V - 3.3V - 0.5V}{2A} = 0.6\Omega \]

Power dissipation in the LT3083 now equals:

\[ P_{\text{TOTAL}} = (5V - 3.3V) \cdot \left(\frac{2A}{60}\right) + 0.5V \cdot 2A = 1.06W \]

The LT3083’s power dissipation is now only 30% compared to no series resistor. \( R_S \) dissipates 2.4W of power. Choose appropriate wattage resistors or use multiple resistors in parallel to handle and dissipate the power properly.
APPLICATIONS INFORMATION

The second technique for reducing power dissipation, shown in Figure 8, uses a resistor in parallel with the LT3083. This resistor provides a parallel path for current flow, reducing the current flowing through the LT3083. This technique works well if input voltage is reasonably constant and output load current changes are small. This technique also increases the maximum available output current at the expense of minimum load requirements.

![Figure 8. Reducing Power Dissipation Using a Parallel Resistor](image)

As an example, assume: \( V_{\text{IN}} = V_{\text{CONTROL}} = 5\, \text{V} \), \( V_{\text{IN(MAX)}} = 5.5\, \text{V} \), \( V_{\text{OUT}} = 3.3\, \text{V} \), \( V_{\text{OUT(MIN)}} = 3.2\, \text{V} \), \( I_{\text{OUT(MAX)}} = 2\, \text{A} \) and \( I_{\text{OUT(MIN)}} = 0.7\, \text{A} \). Also, assuming that \( R_P \) carries no more than 90% of \( I_{\text{OUT(MIN)}} = 630\, \text{mA} \).

Calculating \( R_P \) yields:

\[
R_P = \frac{5.5\, \text{V} - 3.2\, \text{V}}{0.63\, \text{A}} = 3.65\, \Omega
\]

(5% Standard Value = 3.6Ω)

The maximum total power dissipation is \((5.5\, \text{V} - 3.2\, \text{V}) \cdot 2\, \text{A} = 4.6\, \text{W}\). However, the LT3083 supplies only:

\[
2\, \text{A} - \frac{5.5\, \text{V} - 3.2\, \text{V}}{3.6\, \Omega} = 1.36\, \text{A}
\]

Therefore, the LT3083’s power dissipation is only:

\[
P_{\text{DISS}} = (5.5\, \text{V} - 3.2\, \text{V}) \cdot 1.36\, \text{A} = 3.13\, \text{W}
\]

\( R_P \) dissipates 1.47W of power. As with the first technique, choose appropriate wattage resistors to handle and dissipate the power properly. With this configuration, the LT3083 supplies only 1.36A. Therefore, load current can increase by 1.64A to a total output current of 3.64A while keeping the LT3083 in its normal operating range.
**Adding Shutdown**

```
VIN  IN  VIN
    LT3083
       VCONTROL
           SET
             R1
                 Q1
                    VN2222LL
                      ON/OFF
                         SHUTDOWN

Q2* VN2222LL

*Q2 INSURES ZERO OUTPUT
IN THE ABSENCE OF ANY
OUTPUT LOAD.
```

**Current Source**

```
VIN  IN  VIN
    LT3083
       VCONTROL
           SET
             R1
                 Q1
                    VN2222LL
                      ON/OFF
                         SHUTDOWN

Q2* VN2222LL

*Q2 INSURES ZERO OUTPUT
IN THE ABSENCE OF ANY
OUTPUT LOAD.
```

**Low Dropout Voltage LED Driver**

```
VIN  IN  VIN
    LT3083
       VCONTROL
           SET
             R1
                 20k

C1

D1

1A

```

**DAC-Controlled Regulator**

```
VIN  IN  VIN
    LT3083
       VCONTROL
           SET
             150k
                 450k
                     150k
                         SPI
                             LTC2641

GAIN = 4

```

**Examples**

- **Low Dropout Voltage LED Driver**
- **DAC-Controlled Regulator**

**Notes**

- *Q2 INSURES ZERO OUTPUT IN THE ABSENCE OF ANY OUTPUT LOAD.*
TYPICAL APPLICATIONS

Adding Soft-Start

Lab Supply
TYPICAL APPLICATIONS

High Voltage Regulator

Ramp Generator

Reference Buffer

Boosting Fixed Output Regulators

*4mV DROP ENSURES LT3083 IS OFF WITH NO LOAD. MULTIPLE LT3083'S CAN BE USED

V_OUT = 20V
V_OUT = 50µA \times R_{SET}

V_OUT = 3A

\text{VIN} = 50V
\text{VIN} = 5V
\text{VIN} = 3.3V

\text{VOUT} = 20V
\text{VOUT} = 50µA \times R_{SET}

\text{VOUT} = 3A

\text{VOUT} = 3.3V

\text{VOUT} = 4.5A

\text{VOUT} = 3.3V

\text{VOUT} = 4.5A

\text{VOUT} = 3.3V

\text{VOUT} = 4.5A

*MIN LOAD 0.5mA

MUL TIPLE LT3083'S CAN BE USED
Low Voltage, High Current Adjustable High Efficiency Regulator*

DIFFERENTIAL VOLTAGE ON LT3083 IS 0.6V SET BY THE VBE OF THE 2N3906 PNP.
MAXIMUM OUTPUT VOLTAGE IS 1.5V BELOW INPUT VOLTAGE.
Adjustable High Efficiency Regulator*

DIFFERENTIAL VOLTAGE ON LT3083 ≈ 1.4V SET BY THE TP0610L P-CHANNEL THRESHOLD.

MAXIMUM OUTPUT VOLTAGE IS 2V BELOW INPUT VOLTAGE

2 Terminal Current Source

*CCOMP
R1 ≤ 10Ω 10µF
R1 ≥ 10Ω 2.2µF

IOUT = 1V / R1
PACKAGE DESCRIPTION

FE Package
16-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663 Rev H)

Exposed Pad Variation BB

NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN MILLIMETERS (INCHES)
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
*DIMENSIONS DO NOT INCLUDE MOLD FLASH, MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE
DT Package
12-Lead Plastic DFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1733 Rev 0)

2.50 REF
0.70 ±0.05

4.50 ±0.05
3.10 ±0.05

2.38 ±0.05
2.65 ± 0.05

NOTE:
1. DRAWING IS PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGD-X)—TO BE APPROVED
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PIN 1 NOTCH
R = 0.20 TYP OR
0.35 × 45° CHAMFER

PIN 1 TOP MARK (NOTE 6)

0.200 REF
0.75 ± 0.05
0.00 – 0.05

4.00 ± 0.10 (4 SIDES)

BOTTOM VIEW—EXPOSED PAD

RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

0.70 ±0.05
0.50 BSC

R = 0.115
TYP
0.25 ±0.05
0.50 BSC
Q Package

5-Lead Plastic DD-PAK

(Reference LTC DWG # 05-08-1461 Rev E)

BOTTOM VIEW OF DD PAK
HATCHED AREA IS SOLDER PLATED
COPPER HEAT SINK

RECOMMENDED SOLDER PAD LAYOUT

NOTE:
1. DIMENSIONS IN INCH/(MILLIMETER)
2. DRAWING NOT TO SCALE

Linear Technology
PACKAGE DESCRIPTION

T Package
5-Lead Plastic TO-220 (Standard)
(Reference LTC DWG # 05-08-1421)

T5 (TO-220) 0801
0.028 – 0.038
(0.711 – 0.965)

0.147 – 0.155
(3.734 – 3.937)
DIA

0.300 – 0.415
(9.906 – 10.541)

0.460 – 0.500
(11.684 – 12.700)

BSC 0.067
(1.70)

0.028 – 0.038
(0.711 – 0.965)

SEATING PLANE

0.152 – 0.202
(3.861 – 5.131)

0.260 – 0.320
(6.60 – 8.13)

0.165 – 0.180
(4.191 – 4.572)

0.700 – 0.728
(17.78 – 18.491)

0.045 – 0.055
(1.143 – 1.397)

0.155 – 0.195*
(3.937 – 4.953)

0.095 – 0.115
(2.413 – 2.921)

0.013 – 0.023
(0.330 – 0.584)

* MEASURED AT THE SEATING PLANE

(0.020)

(0.020)

(0.77)

(0.77)

(0.77)

(0.77)
### REVISION HISTORY

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<td>Revised part markings in Order Information section</td>
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RELATED PARTS

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<th>DESCRIPTION</th>
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<tr>
<td>LT1185</td>
<td>3A Negative Low Dropout Regulator</td>
<td>VIN: –4.5V to –35V, 0.8V Dropout Voltage, DD-PAK and TO-220 Packages</td>
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<td>LT1764/</td>
<td>3A, Fast Transient Response,</td>
<td>340mV Dropout Voltage, Low Noise: 40µVRMS, VIN = 2.7V to 20V, TO-220 and DD Packages. “A” Version Stable Also with Ceramic Capacitors</td>
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<td>LT1764A</td>
<td>Low Noise LDO</td>
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<tr>
<td>LT1963/A</td>
<td>1.5A Low Noise, Fast Transient</td>
<td>340mV Dropout Voltage, Low Noise: 40µVRMS, VIN = 2.5V to 20V, “A” Version Stable with Ceramic Capacitors, TO-220, DD, SOT-23 and SO-8 Packages</td>
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<td>LT1965</td>
<td>Low Noise, Low Dropout</td>
<td>290mV Dropout Voltage, Low Noise: 40µVRMS, VIN: 1.8V to 20V, VOUT: 1.2V to 19.5V, Stable with Ceramic Capacitors, TO-220, DD-PAK, MSOP and 3mm × 3mm DFN Packages</td>
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<td>LT3022</td>
<td>1A, Low Voltage, VLDO Linear</td>
<td>VIN: 0.9V to 10V, Dropout Voltage: 145mV Typical, Adjustable Output (VREF = VOUT(MIN) = 200mV), Stable with Low ESR, Ceramic Output Capacitors, 16-Pin DFN (5mm × 3mm) and 16-Lead MSOP Packages</td>
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<td>LT3070</td>
<td>5A, Low Noise, Programmable VOUT, 85mV Dropout Linear Regulator with Digital Margining</td>
<td>Dropout Voltage: 85mV, Digitally Programmable VOUT: 0.8V to 1.8V Digital Output Margining: ±1%, ±2% or ±3%, Low Output Noise: 25µVRMS (10Hz to 100kHz), Parallelable: Use Two for a 10A Output, Stable with Low ESR Ceramic Output Capacitors (15µF Minimum), 28-Lead 4mm × 5mm QFN Package</td>
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<td>LT3071</td>
<td>5A, Low Noise, Programmable Vout, 85mV Dropout Linear Regulator with Analog Margining</td>
<td>Dropout Voltage: 85mV, Digitally Programmable VOUT: 0.8V to 1.8V Analog Margining: ±10%, Low Output Noise: 25µVRMS (10Hz to 100kHz), Parallelable: Use Two for a 10A Output, IMON Output Current Monitor, Stable with Low ESR Ceramic Output Capacitors (15µF Minimum), 28-Lead 4mm × 5mm QFN Package</td>
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<td>LT3080/</td>
<td>1.1A, Parallelable, Low Noise,</td>
<td>300mV Dropout Voltage (2-Supply Operation), Low Noise: 40µVRMS, VIN: 1.2V to 36V, VOUT: 0V to 35.7V Current-Based Reference with 1-Resistor VOUT Set; Directly Parallelable (No Op Amp Required), Stable with Ceramic Capacitors, TO-220, DD-PAK, SOT-223, MSBE and 3mm × 3mm DFN-8 Packages; “-1” Version Has Integrated Internal Ballast Resistor</td>
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<td>LT3080-1</td>
<td>Low Dropout Linear Regulator</td>
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<td>LT3082</td>
<td>200mA, Parallelable, Single Resistor, Low Dropout Linear Regulator</td>
<td>Outputs May Be Parallelled for Higher Output, Current or Heat Spreading, Wide Input Voltage Range: 1.2V to 40V, Low Value Input/Output Capacitors Required: 0.22µF Single Resistor Sets Output Voltage, 8-Lead SOT-23, 3-Lead SOT-223 and 8-Lead 3mm × 3mm DFN Packages</td>
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<td>LT3085</td>
<td>500mA, Parallelable, Low Noise,</td>
<td>275mV Dropout Voltage (2-Supply Operation), Low Noise: 40µVRMS, VIN: 1.2V to 36V, VOUT: 0V to 35.7V Current-Based Reference with 1-Resistor VOUT Set; Directly Parallelable (No Op Amp Required), Stable with Ceramic Capacitors, MSBE and 2mm × 3mm DFN-6 Packages</td>
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<td>Low Dropout Linear Regulator</td>
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<td>LTC3026</td>
<td>1.5A, Low Input Voltage VLDO</td>
<td>VIN: 1.14V to 3.5V (Boost Enabled), 1.14V to 5.5V (with External 5V), VOUT = 0.1V, IOUT = 950µA, Stable with 10µF Ceramic Capacitors, 10-Lead MSOP-E and DFN-10 Packages</td>
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<tr>
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<td>Linear Regulator</td>
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