**FEATURES**

- Wide Operating Voltage Range: 2.7V to 27V
- Push Button Control of System Power
- Low Supply Current: 14μA
- Power Fail Comparator Generates Warning
- UVLO Comparator Gracefully Latches Power Off
- Adjustable Supply Monitor with 200ms Reset
- Adjustable Power Down Timer
- Low Leakage EN Output (LTC2953-1) Allows DC/DC Converter Control
- High Voltage EN Output (LTC2953-2) Allows Circuit Breaker Control
- Simple Interface Allows Orderly System Power Up and Down
- ±1.5% Threshold Tolerances
- ±10kV ESD HBM on PB Input
- 12-Pin 3mm × 3mm DFN

**APPLICATIONS**

- Push Button Power Path Control
- Battery Power Supervisor
- Portable Instrumentation, PDA
- Blade Servers
- Desktop and Notebook Computers

**DESCRIPTION**

The LTC®2953 is a push button On/Off controller that manages system power via a push button interface. An enable output toggles system power while an interrupt output provides debounced push button status. The interrupt output can be used in menu driven applications to request a system power down.

The LTC2953 also features input and output power supply monitors. An uncommitted power fail comparator provides real time input monitor information, while a de-glitched under voltage lockout comparator gracefully initiates a system power down. The under voltage lockout comparator prevents the system from powering from a low power supply.

The adjustable supply monitor input is compared against an accurate internal 0.5V reference. The reset output remains low until the supply monitor input has been in compliance for 200ms.

The LTC2953 operates over a wide 2.7V to 27V input voltage range and draws only 14μA of current. Two versions of the part accommodate either positive or negative enable polarities.

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**TYPICAL APPLICATION**

![Typical Application Diagram]

The diagram illustrates a push button on/off control with interrupt. The circuit diagram shows the connections and timing for the PB (Push Button) and EN (Enable) inputs, as well as the interrupt signal. The waveforms at the bottom of the diagram illustrate the pulse timing for PB and EN, and the corresponding system status.

**NOTE**

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LTC2953

**ABSOLUTE MAXIMUM RATINGS** *(Note 1)*

Supply Voltage (V\text{IN}) .................................. –0.3V to 33V

Input Voltages

- PB, PFI, UVLO ........................................... –6V to 33V
- VM ......................................................... –0.3V to 20V
- KILL ....................................................... –0.3V to 10V
- PDT ....................................................... –0.3V to 2.7V

Output Voltages

- EN/EN, PFO ............................................ –0.3V to 50V
- RST, INT ................................................ –0.3V to 10V

Operating Temperature Range

- LTC2953C ................................................ 0°C to 70°C
- LTC2953I ............................................. –40°C to 85°C

Storage Temperature Range ................... –65°C to 125°C

*(Note 1)* The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at TA = 25°C. VIN = 2.7V to 27V, unless otherwise noted (Note 2).

**PIN CONFIGURATION**

![PIN CONFIGURATION](image)

**ORDER INFORMATION**

<table>
<thead>
<tr>
<th>LEAD FREE FINISH</th>
<th>TAPE AND REEL</th>
<th>PART MARKING*</th>
<th>PACKAGE DESCRIPTION</th>
<th>TEMPERATURE RANGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>LTC2953CDD-1#PBF</td>
<td>LTC2953CDD-1#TRPBF</td>
<td>LCWT</td>
<td>12-Lead (3mm × 3mm) Plastic DFN</td>
<td>0°C to 70°C</td>
</tr>
<tr>
<td>LTC2953CDD-2#PBF</td>
<td>LTC2953CDD-2#TRPBF</td>
<td>LCWT</td>
<td>12-Lead (3mm × 3mm) Plastic DFN</td>
<td>0°C to 70°C</td>
</tr>
<tr>
<td>LTC2953IDD-1#PBF</td>
<td>LTC2953IDD-1#TRPBF</td>
<td>LCWT</td>
<td>12-Lead (3mm × 3mm) Plastic DFN</td>
<td>–40°C to 85°C</td>
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<td>LTC2953IDD-2#TRPBF</td>
<td>LCWT</td>
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<td>–40°C to 85°C</td>
</tr>
</tbody>
</table>

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: [http://www.linear.com/leadfree/](http://www.linear.com/leadfree/)

For more information on tape and reel specifications, go to: [http://www.linear.com/tapeandreel/](http://www.linear.com/tapeandreel/)

**ELECTRICAL CHARACTERISTICS**

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at TA = 25°C. VIN = 2.7V to 27V, unless otherwise noted (Note 2).

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<thead>
<tr>
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<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>V\text{IN}</td>
<td>Supply Voltage Range</td>
<td>Steady State Operation ●</td>
<td>2.7</td>
<td>27</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>I\text{IN}</td>
<td>V\text{IN} Supply Current</td>
<td>V\text{IN} = 2.7V to 27V</td>
<td>●</td>
<td>14</td>
<td>26</td>
<td>μA</td>
</tr>
<tr>
<td>V\text{UVL}</td>
<td>V\text{IN} Undervoltage Lockout</td>
<td>V\text{IN} Falling</td>
<td>●</td>
<td>2.2</td>
<td>2.3</td>
<td>2.5</td>
</tr>
<tr>
<td>V\text{PB(MIN, MAX)}</td>
<td>PB Operating Voltage Range</td>
<td>Single-Ended</td>
<td>●</td>
<td>–1</td>
<td>27</td>
<td>V</td>
</tr>
<tr>
<td>I\text{PB}</td>
<td>PB Input Current</td>
<td>2.5V &lt; V\text{PB} &lt; 27V</td>
<td>●</td>
<td>±1</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>V\text{PB} = 1V</td>
<td>●</td>
<td>–1</td>
<td>–6</td>
<td>–12</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>V\text{PB} = 0.6V</td>
<td>●</td>
<td>–3</td>
<td>–9</td>
<td>–15</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>V\text{PB(VTH)}</td>
<td>PB Input Threshold</td>
<td>PB Falling</td>
<td>●</td>
<td>0.6</td>
<td>0.8</td>
<td>1</td>
</tr>
<tr>
<td>V\text{PB(VOC)}</td>
<td>PB Open Circuit Voltage</td>
<td>IPB = –1μA</td>
<td>●</td>
<td>1</td>
<td>1.6</td>
<td>2</td>
</tr>
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</table>
ELECTRICAL CHARACTERISTICS

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</tr>
</thead>
<tbody>
<tr>
<td>$I_{EN(LKG)}$</td>
<td>EN/EN Leakage Current</td>
<td>$V_{EN/EN} = 1V$, Sink Current Off</td>
<td>●</td>
<td>±0.1</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>$V_{EN(VOL)}$</td>
<td>EN/EN Voltage Output Low</td>
<td>$I_{EN/EN} = 500μA$</td>
<td>●</td>
<td>0.11</td>
<td>0.4</td>
<td>V</td>
</tr>
<tr>
<td>$\tau_{EN, Lock Out}$</td>
<td>EN/EN Lock Out Time (Note 3)</td>
<td>Enable Released → Enable Asserted</td>
<td>●</td>
<td>52</td>
<td>64</td>
<td>82</td>
</tr>
</tbody>
</table>

On/Off Timing Pins (PB, UVLO, PDT, INT)

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
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</tr>
</thead>
<tbody>
<tr>
<td>$\tau_{DB, ON}$</td>
<td>Turn On Debounce Time</td>
<td>PB Falling → Enable Asserted</td>
<td>●</td>
<td>26</td>
<td>32</td>
<td>41</td>
</tr>
<tr>
<td>$I_{PDT(PU)}$</td>
<td>PDT Pull Up Current</td>
<td>$V_{PDT} = 0V$</td>
<td>●</td>
<td>–2.4</td>
<td>–3</td>
<td>–3.6</td>
</tr>
<tr>
<td>$I_{PDT(PD)}$</td>
<td>PDT Pull Down Current</td>
<td>$V_{PDT} = 1.3V$</td>
<td>●</td>
<td>2.4</td>
<td>3</td>
<td>3.6</td>
</tr>
<tr>
<td>$\tau_{DB, OFF}$</td>
<td>Turn Off Interrupt Debounce Time</td>
<td>PB, UVLO Falling → INT Falling</td>
<td>●</td>
<td>26</td>
<td>32</td>
<td>41</td>
</tr>
<tr>
<td>$\tau_{PD, Min}$</td>
<td>Internal PB Power Down Delay Time (Note 4)</td>
<td>PB, UVLO Falling → Enable Released PDT Open</td>
<td>●</td>
<td>52</td>
<td>64</td>
<td>82</td>
</tr>
<tr>
<td>$\tau_{PDT}$</td>
<td>Additional Adjustable PB Power Down Delay Time</td>
<td>$C_{PDT} = 1500pF$</td>
<td>●</td>
<td>9</td>
<td>11.5</td>
<td>13.5</td>
</tr>
<tr>
<td>$\tau_{INT, Min}$</td>
<td>Minimum INT Pulse Width</td>
<td>INT Asserted → INT Released</td>
<td>●</td>
<td>26</td>
<td>32</td>
<td>41</td>
</tr>
<tr>
<td>$\tau_{INT, Max}$</td>
<td>Maximum INT Pulse Width</td>
<td>$C_{PDT} = 1500pF$, INT Asserted → INT Released</td>
<td>●</td>
<td>35</td>
<td>43.5</td>
<td>54.5</td>
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</table>

μP Handshake Pins (KILL, INT)

<table>
<thead>
<tr>
<th>SYMBOL</th>
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<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{KILL(TH)}$</td>
<td>KILL Input Threshold Voltage</td>
<td>KILL Falling</td>
<td>●</td>
<td>0.57</td>
<td>0.6</td>
<td>0.63</td>
</tr>
<tr>
<td>$V_{KILL(HYST)}$</td>
<td>KILL Input Threshold Hysteresis</td>
<td>●</td>
<td>10</td>
<td>30</td>
<td>50</td>
<td>mV</td>
</tr>
<tr>
<td>$I_{KILL(PW)}$</td>
<td>KILL Minimum Pulse Width</td>
<td>●</td>
<td>30</td>
<td>μs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{KILL(PD)}$</td>
<td>KILL Propagation Delay</td>
<td>KILL Falling → Enable Released</td>
<td>●</td>
<td>30</td>
<td>μs</td>
<td></td>
</tr>
<tr>
<td>$I_{KILL, ON BLANK}$</td>
<td>Kill Turn On Blanking (Note 5)</td>
<td>KILL = Low, Enable Asserted → Enable Released</td>
<td>●</td>
<td>400</td>
<td>512</td>
<td>650</td>
</tr>
<tr>
<td>$I_{KILL(LKG)}$</td>
<td>KILL Leakage Current</td>
<td>$V_{KILL} = 0.6V$</td>
<td>●</td>
<td>±0.1</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>$I_{INT(LKG)}$</td>
<td>INT Leakage Current</td>
<td>$V_{INT} = 3V$</td>
<td>●</td>
<td>±0.1</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>$V_{INT(VOL)}$</td>
<td>INT Output Voltage Low</td>
<td>$I_{INT} = 3mA$</td>
<td>●</td>
<td>0.11</td>
<td>0.4</td>
<td>V</td>
</tr>
</tbody>
</table>

Power Fail and Voltage Monitor Pins (PFI, PF0, UVLO, VM, RST)

<table>
<thead>
<tr>
<th>SYMBOL</th>
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<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{PFI(TH)}$</td>
<td>PFI Input Threshold Voltage</td>
<td>Falling</td>
<td>●</td>
<td>492</td>
<td>500</td>
<td>508</td>
</tr>
<tr>
<td>$V_{UVLO(TH)}$</td>
<td>UVLO Input Threshold Voltage</td>
<td>Falling</td>
<td>●</td>
<td>492</td>
<td>500</td>
<td>508</td>
</tr>
<tr>
<td>$V_{VM(TH)}$</td>
<td>Adjustable Reset Threshold</td>
<td>Falling/Rising</td>
<td>●</td>
<td>492</td>
<td>500</td>
<td>508</td>
</tr>
<tr>
<td>$\Delta V_{TH}$</td>
<td>PFI-UVLO Threshold Mismatch</td>
<td>●</td>
<td>–5</td>
<td>0</td>
<td>5</td>
<td>mV</td>
</tr>
<tr>
<td>$V_{PFH(HYST)}$</td>
<td>PFI Input Hysteresis</td>
<td>●</td>
<td>2</td>
<td>4</td>
<td>10</td>
<td>mV</td>
</tr>
<tr>
<td>$V_{UVLO(HYST)}$</td>
<td>UVLO Input Hysteresis</td>
<td>●</td>
<td>30</td>
<td>50</td>
<td>70</td>
<td>mV</td>
</tr>
<tr>
<td>$V_{PF0(VOL)}$</td>
<td>PF0 Output Voltage Low</td>
<td>$I_{PF0} = 500μA$</td>
<td>●</td>
<td>0.11</td>
<td>0.4</td>
<td>V</td>
</tr>
<tr>
<td>$V_{RST(VOL)}$</td>
<td>RST Output Voltage Low</td>
<td>$I = 3mA$</td>
<td>●</td>
<td>0.11</td>
<td>0.4</td>
<td>V</td>
</tr>
</tbody>
</table>
**ELECTRICAL CHARACTERISTICS**  The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ C$. $V_{IN} = 2.7V$ to $27V$, unless otherwise noted (Note 2).

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<th><strong>TYP</strong></th>
<th><strong>MAX</strong></th>
<th><strong>UNITS</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{PFI(LKG)}$</td>
<td>PFI Leakage Current</td>
<td>$V_{PFI} = 0.5V$ $V_{PFI} = 27V$</td>
<td>●</td>
<td>2</td>
<td>±10</td>
<td>nA</td>
</tr>
<tr>
<td>$I_{PFO(LKG)}$</td>
<td>PFO Leakage Current</td>
<td>$V_{PFO} = 1V$ $V_{PFO} = 40V$</td>
<td>●</td>
<td>2</td>
<td>±10</td>
<td>μA</td>
</tr>
<tr>
<td>$I_{UVLO(LKG)}$</td>
<td>UVLO Leakage Current</td>
<td>$V_{UVLO} = 0.5V$ $V_{UVLO} = 27V$</td>
<td>●</td>
<td>2</td>
<td>±10</td>
<td>μA</td>
</tr>
<tr>
<td>$I_{VM(LKG)}$</td>
<td>VM Input Leakage Current</td>
<td>$VM = 0.5V$</td>
<td>●</td>
<td>2</td>
<td>±10</td>
<td>nA</td>
</tr>
<tr>
<td>$I_{RST(LKG)}$</td>
<td>RST Output Leakage Current</td>
<td>$V_{RST} = 3V$</td>
<td>●</td>
<td>±0.1</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>$t_{PFI}$</td>
<td>PFI Delay to PFO</td>
<td></td>
<td>●</td>
<td>40</td>
<td>100</td>
<td>200</td>
</tr>
<tr>
<td>$t_{RST}$</td>
<td>Reset Timeout Period</td>
<td></td>
<td>●</td>
<td>140</td>
<td>200</td>
<td>260</td>
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<tr>
<td>$t_{UV}$</td>
<td>VM Under Voltage Detect to RST</td>
<td>VM Less Than VM(TH) By More Than 1%</td>
<td></td>
<td>250</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** All currents into pins are positive; all voltages are referenced to GND unless otherwise noted.

**Note 3:** The Enable Lock Out time is designed to allow an application to properly power down such that the next power up sequence starts from a consistent powered down configuration. PB is ignored during this lock out time. This time delay does not include $t_{DB, ON}$.

**Note 4:** To manually force a release of the EN/IGN pin, either PB or UVLO must be held low for at least $t_{PD, Min}$ (internal default power down timer) + $t_{PDT}$ (adjustable by placing external capacitor at PDT pin).

**Note 5:** The KILL turn on blanking timer period ($t_{KILL, ON BLANK}$) is the waiting period immediately after enable output is asserted. This blanking time allows sufficient time for the DC/DC converter and the μP to perform power up tasks. The KILL, PB and UVLO inputs are ignored during this period. If KILL remains low at the end of this blanking period, the enable output is released, thus turning off system power.
TEMPERATURE (°C) -50 –25 0 25 50

IVIN (μA) 10 15 20

VIN = 27V
VIN = 3.3V
VIN = 2.7V

TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Temperature

Supply Current vs Supply Voltage

Turn On Debounce Time (tDB, ON) vs VIN

Turn Off Interrupt Debounce Time (tDB, OFF) vs VIN

Forced Power Down Delay Time (tPD, MIN + tPDT) vs PDT External Capacitance

PDT Pull-Down Current vs Temperature

PDT Pull-Up Current vs Temperature

PB Current vs PB Voltage

PB Voltage vs External PB Resistance to Ground

PB VOLTAGE (mV) 0 50 100 150 200

EXTERNAL PB RESISTANCE TO GROUND (kΩ) 0 10 20 30

VOUT = 3.3V

TA = 100°C

TA = –45°C

TA = 25°C
TYPICAL PERFORMANCE CHARACTERISTICS

EN (LTC2953-1) Voltage vs $V_{IN}$

$T_A = 25^\circ C$
100k PULL-UP FROM EN TO $V_{IN}$

EN (LTC2953-2) Voltage vs $V_{IN}$

$T_A = 25^\circ C$
100k PULL-UP FROM EN TO $V_{IN}$

PFO Voltage vs $V_{IN}$

$T_A = 25^\circ C$
PFI = 1V
100k PULL-UP FROM PFO TO $V_{IN}$

RST Voltage vs $V_{IN}$

$T_A = 25^\circ C$
VM = 1V
100k PULL-UP FROM RST TO $V_{IN}$

RST, INT $V_{OL}$ vs Current Load

$T_A = 25^\circ C$
$V_{IN} = 3.3V$

Threshold Voltage (VM, PFI, UVLO) vs Temperature

$V_{IN} = 3.3V$

EN/EN, PFO $V_{OL}$ vs Current Load

$T_A = 25^\circ C$
$V_{IN} = 3.3V$
PIN FUNCTIONS

**GND (Pin 1):** Ground.

**VM (Pin 2):** Voltage Monitor Input. Input to an accurate comparator with a 0.5V threshold. VM controls the state of the RST output pin and is independent of PB, PFI and UVLO status. A voltage below 0.5V on this pin asserts RST low. Connect to GND if unused.

**KILL (Pin 3):** KILL Input. Forcing KILL low releases the enable output. During system turn on, this pin is blanked by a 512ms internal timer (tKILL, ON BLANK) to allow the system to pull KILL high. This pin has an accurate 0.6V threshold and can be used as a power kill voltage monitor. Set the pin voltage above its threshold if unused.

**PDT (Pin 4):** Power Down Time Input. A capacitor to ground determines the additional time (6.4 seconds/µF) that PB or UVLO must be held low before releasing the EN/EN and INT outputs. If this pin is left open, the power down delay time defaults to 64ms.

**PB (Pin 5):** Push Button Input. Connecting PB to ground through a momentary switch provides On/Off control via the EN/EN and INT outputs. An internal 100k pull-up resistor connects to an internal 1.9V bias voltage. The rugged PB input withstands ±10kV ESD HBM and can be pulled up to 27V externally without consuming extra current. Voltages below ground will not damage the pin.

**VIN (Pin 6):** Power Supply Input: 2.7V to 27V.

**UVLO (Pin 7):** UVLO Comparator Input. When UVLO drops below its falling threshold (0.5V) for more than 32ms, the LTC2953 asserts INT low, thereby requesting a system power down. If UVLO remains below its falling threshold (0.5V) for longer than the adjustable power down delay, the enable output is released. Additionally, UVLO provides a PB lock out feature that prevents the user from asserting the enable output when UVLO falls below its threshold. Connect to VIN if unused.

**PFI (Pin 8):** Power Fail Comparator Input. Input to an accurate comparator with a 0.5V falling threshold and 4mV of hysteresis. PFI controls the state of the PFO output pin and is independent of PB, VM and UVLO status. Connect to GND if unused.

**PFO (Pin 9):** Power Fail Output. This pin is a high voltage open drain pull-down. PFO pulls low when PFI is below 0.5V. Open circuit when unused.

**RST (Pin 10):** Reset Output. This pin is an open drain pull-down. Pulls low when VM input is below 0.5V and is held low for 200ms after VM input is above 0.5V. Open circuit when unused.

**EN (LTC2953-1, Pin 11):** Open Drain Enable Output. This output is intended to enable system power. EN is asserted high after a valid PB turn on event (tDB, ON). EN is released low if: a) KILL is not driven high (by μP) within 512ms of the initial valid PB power turn on event, b) KILL is driven low during normal operation, c) PB or UVLO is asserted and held low (t > tPD, Min + tPDT) during normal operation.

**EN (LTC2953-2, Pin 11):** Open Drain Enable Output. This output is intended to enable system power. EN is asserted high after a valid PB turn on event (tDB, ON). EN is released low if: a) KILL is not driven high (by μP) within 512ms of the initial valid PB power turn on event, b) KILL is driven low during normal operation, c) PB or UVLO is asserted and held low (t > tPD, Min + tPDT) during normal operation.

**INT (Pin 12):** Open Drain Interrupt Output. After a turn off event is detected (tDB, OFF) from PB or UVLO, the LTC2953 interrupts the system (μP) by asserting INT low. The μP would perform power down and housekeeping tasks and then assert the KILL pin low, thus releasing the enable output. The INT pulse width is a minimum of 32ms and stays low as long as PB is asserted. If PB is asserted for longer than tPD, Min + tPDT, however, the INT and EN/EN outputs are immediately released. Open circuit when unused.

**Exposed Pad (Pin 13):** Exposed Pad may be left open or connected to ground.
TIMING DIAGRAMS

Figure 1. Power On Timing (UVLO > 0.55V)

Figure 2. PB Interrupt Pulse: PB Low for $t_{DB, OFF} < t < (t_{PD, Min} + t_{PDT})$ (Enable Remains Active)
Figure 3. UVLO Interrupt Pulse: UVLO Low for \( t_{DB,OFF} < t < (t_{PD,\text{Min}} + t_{PDT}) \) (Enable Remains Active)

Figure 4. Push Button Power Down Timing: \( \overline{PB} \) Pressed and Held Low for \( t > (t_{PD,\text{Min}} + t_{PDT}) \)
Figure 5. UVLO Power Down Timing: UVLO Low for $t > (t_{PD, \text{Min}} + t_{PDT})$

Figure 6. Voltage Monitor Reset Timing

Figure 7. Power Fail Comparator Timing

Figure 8. KILL Minimum Pulse Width and Propagation Delay
The LTC2953 is a push button On/Off controller with dual function input and output supply monitors. The part contains all the circuitry needed to debounce a push button input and provides a simple \( \mu \)P handshake protocol for reliable toggling of system power. The LTC2953 operates over a wide 2.7V to 27V input voltage range and draws only 14\( \mu \)A of current.

The LTC2953 features dual function supply monitoring: a power fail comparator generates an early warning and an under voltage lock-out comparator initiates a controlled system power down.

**Push Button Controller**

The push button input controls the enable and interrupt outputs. The enable output toggles system power while the interrupt output provides debounced push button status. The interrupt output can be used in menu driven applications to request a system power down. A power kill input allows a microprocessor or other logic to release the enable output, thus immediately powering down the system.

To assert the enable output (turn on system power), press the push button (\( \bar{P}_B \)) input and hold for at least 32ms. See Figure 1.

Once system power has been enabled, a user can request a system power down by again pressing the push button for at least 32ms and releasing it before the PDT timer counts 16 cycles. The LTC2953 then asserts the interrupt output and the \( \mu \)P subsequently sets the KILL input low to turn off system power. Note that the UVLO input can also assert the interrupt output. See Figure 2 and Figure 3 and Dual Function Supply Monitors section.

In the event that the \( \mu \)P does not respond to the interrupt request, the user can force release of the enable output by pressing and holding down the push button (or UVLO) until the PDT timer times out. See Figure 4 and Figure 5.

**Dual Function Supply Monitors**

An uncommitted power fail comparator provides real time supply threshold information. The power fail input (PFI) is compared against an accurate internal 0.5V reference and the comparison result is passed directly to the power fail output (PF0) pin. The operation of the power fail comparator is de-coupled from all other functionality and is always active. See Figure 7.

The under voltage lockout comparator provides the user with another method to initiate a controlled system power down. If the UVLO pin voltage falls below its falling threshold (0.5V) for longer than 32ms, the interrupt output is asserted for a minimum of 32ms. If the UVLO pin voltage remains below its threshold (0.5V) for an additional time given by the PDT external capacitor, then the enable pin is automatically released (thus powering down the system). See Figure 3 and Figure 5.

This comparator also serves as an under voltage lockout. If system power is off (enable released) and UVLO < 0.5V, the UVLO comparator prevents the push button from turning on system power (asserting enable output).

**Voltage Supervisor with 200ms \( \mu \)P Reset**

The LTC2953 provides a single adjustable supply monitor with a nominal 200ms reset delay. When the VM input voltage drops below 0.5V, the RST output is pulled low. RST remains low for 200ms after the VM input has risen above 0.5V. The input 0.5V threshold has a guaranteed accuracy of \( \pm 1.5\% \) over temperature and process. The operation of the supply monitor is de-coupled from all other functionality and is always active. See Figure 6.
APPLICATIONS INFORMATION

PUSH BUTTON CONTROL

Power On Sequence

To enable system power, the push button input (PB) must be held low continuously for 32ms (tDB, ON). Once the enable output (EN/EN) is asserted, the LTC2953 starts a 512ms internal timer (tKILL, ON BLANK). The KILL input must be driven high within this 512ms window. This blanking time represents the maximum time allowed for the system to power up and initialize the circuits driving the KILL input. If KILL remains low at the end of the blanking period, the enable output is released (see “Aborted Power On Sequence” section). Figure 9 shows a normal power on sequence.

Figure 9. Power On Timing (UVLO > 0.55V)

Note that only the push button input can enable system power. The LTC2953 provides two enable output polarities to allow DC/DC converter control (LTC2953-1) and external power PFET control (LTC2953-2).

Short Pulse Interrupt

To interrupt the μP, either PB or UVLO must be low for at least 32ms (tDB, OFF). This signals the μP either that a user has pressed the push button or that the supply is running low. The μP would then perform power down and housekeeping tasks and assert KILL low when done. This in turn releases the enable output, thus shutting off system power. See Figure 10.

Note that either PB or UVLO can control the power down sequence, but not both at the same time. For example, if both PB and UVLO are high and the user presses the push button, PB will be active and UVLO will be ignored until PB is released or the power down sequence is complete.

Forced Power Off Sequence

The LTC2953 provides a failsafe feature that allows a user to manually force a system power down. For cases when the μP fails to respond to the interrupt signal, the user can force a power down by pressing and holding either the push button or the UVLO inputs low.

The length of time required to release the enable output is given by a fixed internal 64ms delay (tPD, Min) plus an adjustable power down timer delay (tPDT). The adjustable delay is set by placing an external capacitor on the PDT pin. Use the following equation to calculate the capacitance for the desired extra delay. CPDT is the PDT pin external capacitor:

\[ CPDT = 1.56E-4 \, \mu F/\text{ms} \times (t_{PDT} - 1\,\text{ms}) \]

See Figure 11.

Figure 10. Power Off Interrupt Timing

Figure 11. Forced Power Off Timing with Adjustable Delay

(See Figure 5 for More Details)
APPLICATIONS INFORMATION

Aborted Power On Sequence

The LTC2953 provides an internal 512ms timer to detect when a system fails to power on properly. A power on sequence begins by debouncing the PB input. After the enable pin is subsequently asserted, the LTC2953 starts the 512ms blanking timer (tKILL, ON BLANK). If the KILL input is not driven high within this 512ms time window, the enable pin is immediately released, thus turning off system power. This failsafe feature prevents a user from turning on the device when the circuits driving the KILL input do not respond within 512ms after enable has been asserted. See Figure 12.

μP Turns Off System Power During Normal Operation

Once the system has powered on and is operating normally, the μP can turn off power by asserting the KILL input low. See Figure 13.

DUAL FUNCTION BATTERY SUPERVISOR

The LTC2953 provides two comparators for battery monitoring: an uncommitted power fail comparator and a latched low battery comparator with μP interrupt. The application shown in Figure 14 monitors a 2 cell Li-Ion battery stack.

Power Fail Comparator

This comparator provides real time threshold information and can serve as the first warning of a decaying battery or supply. The PFO output is driven low when the PFI input voltage drops below its falling threshold (0.5V) and is high impedance when PFI rises above its rising threshold (0.504V). The low leakage, high voltage PFI input (10nA, maximum) allows the use of large valued external resistors, which lowers system current consumption.

UVLO Comparator

The under voltage lockout comparator performs three functions: a) interrupts the μP when a supply glitch drives the UVLO voltage below its falling threshold (0.5V) for longer than 32ms, followed by b) forces system power off when the UVLO voltage falls below its falling threshold (0.5V) for tPD, Min + tPDT, c) locks out the enable (prevents system power on) output if UVLO voltage is below its falling threshold (0.5V) during system power on. See Figures 15A and 15B.

The low leakage (10nA, maximum), high voltage UVLO input allows the use of large valued external resistors. See Figure 14.
Which Input Initiated Power Down: PB or UVLO?

The circuit in Figure 14 determines whether a power down was initiated by a user pressing the push button or by a battery drooping too low. If both INT and PFO outputs are low, then a low battery condition initiated a power down.

PFI and UVLO Thresholds

The circuit depicted in Figure 14 uses one resistive divider network for both power fail and low battery comparators. The power fail comparator trips at a higher battery voltage than the low battery comparator, thus providing a battery warning before a power down sequence is initiated. Due to the low offset architecture of the comparators, the UVLO and PFI thresholds can be set to as close as ±5mV apart. The trip thresholds of the circuit of Figure 14 are 6.04V and 5.40V for the power fail and low battery (UVLO) comparators, respectively.

Push Button Lockout

The LTC2953 provides a push button lock out feature that prevents a user from turning on a system with a dead battery. The push button input is ignored when the UVLO input voltage is less than the falling threshold (0.5V). See Figure 15B.
TYPICAL APPLICATIONS

Push Button Buffer

The circuit of Figure 16 shows the power fail comparator sensing the push button input. The PFO output toggles each time the push button crosses 0.5V. This application provides an early warning of push button activity.

![Figure 16. Push Button Buffer](image)

Disconnect Input Resistive Divider To Save Power

In order to prolong battery life when system power has been turned off, the LTC2953-2 power fail comparator can be used to disconnect the external battery monitor resistive divider. The circuit in Figure 18 connects PFI to EN and PFO to the bottom end of the resistive divider.

![Figure 18. Disconnect Input Resistive Divider to Save Power](image)

Power Path Switching

The high voltage EN output of the LTC2953-2 is designed to switch On/Off an external power PFET. This allows a user to connect/disconnect a power supply (or battery) to its load by toggling the PB pin. Figure 17 shows the LTC2953-2 in a 12V wall adapter application.

![Figure 17. Power Path Switching](image)

When the user presses the push button to turn on system power (EN low), the output of the power fail comparator asserts PFO low. The low battery external resistive divider is thus enabled to monitor the input supply. If the voltage on the UVLO input falls to less than 0.5V, a system power down sequence is initiated. Note that the IR drop across the internal NFET is typically less than 0.2mV when the UVLO pin voltage is 0.5V.

Once system power has been turned off (EN high), the external resistive divider is disconnected and thus consumes zero DC current.
TYPICAL APPLICATIONS

Push Button Controlled μP Reset

The circuit of Figure 19 can be used to keep a μP in reset for 200ms after the push button has enabled system power. After system power has stabilized, the voltage monitor input continues to monitor the supply at the load end.

![Figure 19. Push Button Controlled μP Reset](image)

Push Button Controlled Supply Sequencing

The circuit in Figure 20 uses the LTC2953-2 to sequence 3 supply rails. Power on sequencing begins by pressing the push button for 32ms. This asserts the EN output low, which turns on the V1 supply. 200ms after V1 reaches 80% of its final value (2.66V), the V2 supply is enabled. When the V2 DC voltage reaches 80% of its final value (2V), the V3 supply is enabled. Note that there is no internal delay from the PFI input to the PFO output and so V3 is enabled at the same time V2 rises above 2V.

A power down supply sequence begins when any of these inputs is asserted: PB, UVLO or KILL. When EN pulls up to V_IN, V1 disconnects first. When V1 decays to 2.66V, V2 is immediately disabled (there is no 200ms delay from VM to RST during power down). When V2 decays to 2V, V3 is immediately disabled. See Figure 21 timing diagram.

![Figure 20. Push Button Controlled Supply Sequencing](image)

![Figure 21. Push Button Controlled Supply Sequence Timing](image)
TYPICAL APPLICATIONS

Dual Supply Monitor with μP Reset

The circuit of Figure 22 monitors two supplies and provides a μP reset. When either the PFI or the VM input voltage falls below its threshold (0.5V), the RST output is asserted low. RST remains low for 200ms after both inputs rise above 0.5V. The low leakage PFO output allows for large valued external resistors.

![Figure 22. Dual Supply Monitor with μP Reset](image)

Reverse Battery Protection

To protect the LTC2953 from a reverse battery connection, place a 1k resistor (R8) in series with the VIN pin. See Figure 23.

![Figure 23. Reverse Battery Protection Using R8](image)

Operation with Supply Transients over 40V

The application circuit of Figure 24 operates from a 24V nominal supply, but can withstand supply transients as high as 40V.

The high voltage EN output of the LTC2953-2 has an absolute maximum rating of 50V, which makes it suitable for driving the gate of the external power PFET. The external 30V Zener diode (Z1) and the 10k current limiting resistor (RZ) protect the VIN supply pin of the LTC2953-2. Note that under normal 24V operation, the external Zener diode does not conduct any current. The voltage drop across RZ should be kept below 1V. Z2 should have a breakdown voltage smaller than the PFET’s gate-to-source breakdown voltage.

![Figure 24. Operation with 40V Supply Transients](image)

Power Path Controller with Low Battery Detect

The application in Figure 25 uses the push button to completely disconnect the load from the battery. If the battery voltage falls below the user specified threshold, the push button is prevented from turning on system power (asserting the enable output).

![Figure 25. Power Path Controller with Low Battery Detect](image)
PACKAGE DESCRIPTION

DD Package
12-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1725 Rev A)

RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD AND TIE BARS SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE
TYPICAL APPLICATION

![PowerPath Controller with Low Battery Detect](image)

Figure 25. PowerPath Controller with Low Battery Detect

### RELATED PARTS

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>LTC2900</td>
<td>Programmable Quad Supply Monitor</td>
<td>Adjustable Reset, 10-Lead MSOP and 3mm × 3mm DFN Packages</td>
</tr>
<tr>
<td>LTC2904/LTC2905</td>
<td>Pin-Programmable Dual Supply Monitors</td>
<td>Adjustable Reset and Tolerance, 8-Lead SOT-23 and 3mm × 2mm DFN Packages</td>
</tr>
<tr>
<td>LTC2909</td>
<td>Precision Tripple/Dual Input UV, OV and Negative Voltage Monitor</td>
<td>6.5V Shunt Regulator for High Voltage Operation</td>
</tr>
<tr>
<td>LTC2912</td>
<td>Single UV/OV Monitor</td>
<td>3mm × 2mm DFN, 8-Pin ThinSOT Packages</td>
</tr>
<tr>
<td>LTC2950/LTC2951</td>
<td>Push Button On/Off Controllers</td>
<td>High Voltage, Low Power Push Button Controller</td>
</tr>
<tr>
<td>LTC2952</td>
<td>Push Button Power Path Controller with Supervisor</td>
<td>Automatic Low Loss Switchover Between DC Sources</td>
</tr>
<tr>
<td>LTC2954</td>
<td>Push Button On/Off Controller with μP Interrupt</td>
<td>Allow Controlled Software System Shutdown</td>
</tr>
<tr>
<td>LTC4055</td>
<td>USB Power Controller and Li-Ion Charger</td>
<td>Automatic Switchover, Charges 1-Cell Li-Ion Batteries</td>
</tr>
<tr>
<td>LTC4411</td>
<td>2.6A Low Loss Ideal Diode in ThinSOT</td>
<td>No External MOSFET, Automatic Switching Between DC Sources</td>
</tr>
<tr>
<td>LTC4412HV</td>
<td>PowerPath Controller in ThinSOT</td>
<td>Efficient Diode-ORing, Automatic Switching Between DC Sources, 3V to 36V</td>
</tr>
</tbody>
</table>