**FEATURES**
- Monitors Four Voltages Simultaneously
- Adjustable UV and OV Trip Values
- Guaranteed Threshold Accuracy: ±1.5% of Monitored Voltage over Temperature
- Input Glitch Rejection
- Monitors up to Two Negative Voltages
- Buffered 1V Reference Output
- Adjustable Reset Timeout with Timeout Disable
- 62μA Quiescent Current
- Open-Drain OV and UV Outputs
- Guaranteed OV and UV for VCC ≥ 1V
- Available in 16-Lead SSOP and 16-Lead (5mm × 3mm) DFN Packages

**APPLICATIONS**
- Desktop and Notebook Computers
- Network Servers
- Core, I/O Voltage Monitors

**DESCRIPTION**

The **LTC2914** is a quad input voltage monitor intended for monitoring multiple voltages in a variety of applications. Dual inputs for each monitored voltage allow monitoring four separate undervoltage (UV) conditions and four separate overvoltage (OV) conditions. All monitors share a common undervoltage output and a common overvoltage output. The LTC2914-1 has latching capability for the overvoltage output. The LTC2914-2 has functionality to disable both the overvoltage and undervoltage outputs.

Polarity selection and a buffered reference allow monitoring up to two separate negative voltages. A three-state input pin allows setting the polarity of two inputs without requiring any external components. Glitch filtering ensures reliable reset operation without false or noisy triggering.

The LTC2914 provides a precise, versatile, space-conscious, micropower solution for voltage monitoring.

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**TYPICAL APPLICATION**

Quad UV/OV Supply Monitor, 10% Tolerance, 5V, 3.3V, 2.5V, 1.8V

---

**Entering Power Supplies**

**Input Threshold Voltage vs Temperature**

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**ABSOLUTE MAXIMUM RATINGS** *(Notes 1, 2)*

Terminal Voltages

- \( V_{CC} \) (Note 3) ........................................ –0.3V to 6V
- \( OV, UV \) .............................................. –0.3V to 16V
- \( TMR \) ............................................. –0.3V to \((V_{CC} + 0.3V)\)
- \( VL_n, VH_n, LATCH, DIS, SEL \) .................. –0.3V to 7.5V

Terminal Currents

- \( I_{VCC} \) ........................................... 10mA
- Reference Load Current \((I_{REF})\) ............. ±1mA
- \( I_{UV}, I_{OV} \) ........................................ 10mA

Operating Temperature Range

- LTC2914C ........................................ 0°C to 70°C
- LTC2914I ........................................ –40°C to 85°C
- LTC2914H ........................................ –40°C to 125°C

Storage Temperature Range ......................... –65°C to 150°C

Lead Temperature (Soldering, 10 sec) SSOP ................... 300°C

---

**ORDER INFORMATION**

<table>
<thead>
<tr>
<th>LEAD FREE FINISH</th>
<th>TAPE AND REEL</th>
<th>PART MARKING*</th>
<th>PACKAGE DESCRIPTION</th>
<th>TEMPERATURE RANGE</th>
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<td>LTC2914CDHC-1#TRPBF</td>
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<td>0°C to 70°C</td>
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<td>LTC2914IGN-1#TRPBF</td>
<td>291411</td>
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<td>LTC2914HG1N-1#PBF</td>
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<td>2914H1</td>
<td>16-Lead Plastic SSOP</td>
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</table>

For more information www.linear.com/LTC2914
## ORDER INFORMATION

<table>
<thead>
<tr>
<th>LEAD FREE FINISH</th>
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<th>PACKAGE DESCRIPTION</th>
<th>TEMPERATURE RANGE</th>
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<td>LTC2914CGN-2#TRPBF</td>
<td>29142</td>
<td>16-Lead Plastic SSOP</td>
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<tr>
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<td>2914H2</td>
<td>16-Lead Plastic SSOP</td>
<td>–40°C to 125°C</td>
</tr>
</tbody>
</table>

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: [http://www.linear.com/leadfree/](http://www.linear.com/leadfree/)

For more information on tape and reel specifications, go to: [http://www.linear.com/tapeandreel/](http://www.linear.com/tapeandreel/)

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. $V_{CC} = 3.3V$, $V_{Ln} = 0.45V$, $V_{Hn} = 0.55V$, $V_{LATCH} = V_{CC}$, $SEL = V_{CC}$, $DIS = Open$ unless otherwise noted. (Note 2)

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{SHUNT}$</td>
<td>$V_{CC}$ Shunt Regulator Voltage</td>
<td>$I_{CC} = 5mA$</td>
<td>● 6.2</td>
<td>6.6</td>
<td>6.9</td>
<td>V</td>
</tr>
<tr>
<td>$\Delta V_{SHUNT}$</td>
<td>$V_{CC}$ Shunt Regulator Load Regulation</td>
<td>$I_{CC} = 2mA$ to $10mA$</td>
<td>● 200</td>
<td>300</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>$V_{CC}$</td>
<td>Supply Voltage (Note 3)</td>
<td>$I_{CC} = 5mA$</td>
<td>● 2.3</td>
<td>$V_{SHUNT}$</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{CCR(MIN)}$</td>
<td>Minimum $V_{CC}$ Output Valid</td>
<td>$DIS = 0V$</td>
<td>● 1</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{CC(UVLO)}$</td>
<td>Supply Undervoltage Lockout</td>
<td>$V_{CC}$ Rising, $DIS = 0V$</td>
<td>● 1.9</td>
<td>2</td>
<td>2.1</td>
<td>V</td>
</tr>
<tr>
<td>$\Delta V_{CC(UVHYST)}$</td>
<td>Supply Undervoltage Lockout Hysteresis</td>
<td>$DIS = 0V$</td>
<td>● 5</td>
<td>25</td>
<td>50</td>
<td>mV</td>
</tr>
<tr>
<td>$I_{CC}$</td>
<td>Supply Current</td>
<td>$V_{CC} = 2.3V$ to $6V$</td>
<td>● 62</td>
<td>100</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>$V_{REF}$</td>
<td>Reference Output Voltage</td>
<td>$I_{REF} = \pm 1mA$</td>
<td>● 0.985</td>
<td>1</td>
<td>1.015</td>
<td>V</td>
</tr>
<tr>
<td>$V_{UOT}$</td>
<td>Undervoltage/Overvoltage Voltage Threshold</td>
<td>$V_{CC} = 2.3V$ to $6V$</td>
<td>● 6</td>
<td>8.5</td>
<td>12.5</td>
<td>ms</td>
</tr>
<tr>
<td>$t_{UOD}$</td>
<td>Undervoltage/Overvoltage Voltage Threshold to Output Delay</td>
<td>$V_{Hn} = V_{UOT} - 5mV$ or $V_{Ln} = V_{UOT} + 5mV$</td>
<td>● 50</td>
<td>125</td>
<td>500</td>
<td>µs</td>
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<tr>
<td>$I_{VH}$</td>
<td>$V_{Hn, VLn}$ Input Current</td>
<td>$-40°C &lt; T_A &lt; 125°C$</td>
<td>●</td>
<td>±15</td>
<td>nA</td>
<td></td>
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<tr>
<td>$I_{UOT}$</td>
<td>$V_{Hn, VLn}$ Input Current</td>
<td>$-40°C &lt; T_A &lt; 125°C$</td>
<td>●</td>
<td>±30</td>
<td>nA</td>
<td></td>
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<tr>
<td>$I_{UOT}$</td>
<td>UV/UV Time-Out Period</td>
<td>$C_{TMR} = 1nF$</td>
<td>● 6</td>
<td>8.5</td>
<td>12.5</td>
<td>ms</td>
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<tr>
<td>$V_{LATCH(IH)}$</td>
<td>OV Latch Clear Input High</td>
<td>$-40°C &lt; T_A &lt; 125°C$</td>
<td>● 6</td>
<td>8.5</td>
<td>14</td>
<td>ms</td>
</tr>
<tr>
<td>$V_{LATCH(IL)}$</td>
<td>OV Latch Clear Threshold Input Low</td>
<td>$-40°C &lt; T_A &lt; 125°C$</td>
<td>● 6</td>
<td>8.5</td>
<td>14</td>
<td>ms</td>
</tr>
<tr>
<td>$I_{LATCH}$</td>
<td>LATCH Input Current</td>
<td>$V_{LATCH} &gt; 0.5V$</td>
<td>●</td>
<td>±1</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>$I_{DIS(IH)}$</td>
<td>DIS Input High</td>
<td>$V_{DIS} &gt; 0.5V$</td>
<td>● 1</td>
<td>2</td>
<td>3</td>
<td>µA</td>
</tr>
<tr>
<td>$I_{DIS(IL)}$</td>
<td>DIS Input Low</td>
<td>$V_{DIS} &gt; 0.5V$</td>
<td>● 0.8</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{DIS}$</td>
<td>DIS Input Current</td>
<td>$V_{DIS} &gt; 0.5V$</td>
<td>● 1</td>
<td>2</td>
<td>3</td>
<td>µA</td>
</tr>
<tr>
<td>$I_{TMR(UP)}$</td>
<td>TMR Pull-Up Current</td>
<td>$V_{TMR} = 0V$</td>
<td>● –1.3</td>
<td>–2.1</td>
<td>–2.8</td>
<td>µA</td>
</tr>
<tr>
<td>$I_{TMR(DOWN)}$</td>
<td>TMR Pull-Down Current</td>
<td>$V_{TMR} = 1.6V$</td>
<td>● 1.3</td>
<td>2.1</td>
<td>2.8</td>
<td>µA</td>
</tr>
</tbody>
</table>

For more information [www.linear.com/LTC2914](http://www.linear.com/LTC2914)
**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ C$. $V_{CC} = 3.3V$, $VLn = 0.45V$, $VHn = 0.55V$, $LATCH = V_{CC}$, $SEL = V_{CC}$, $DIS = \text{Open unless otherwise noted. (Note 2)}$

<table>
<thead>
<tr>
<th>SYMBOL</th>
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<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{TMR(DIS)}$</td>
<td>Timer Disable Voltage</td>
<td>Referenced to $V_{CC}$</td>
<td>●</td>
<td>180</td>
<td>270</td>
<td>mV</td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>Output Voltage High $\overline{U}V/\overline{O}V$</td>
<td>$V_{CC} = 2.3V$, $I_{UV/OV} = \pm 1\mu A$</td>
<td>●</td>
<td>1</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Output Voltage Low $\overline{U}V/\overline{O}V$</td>
<td>$V_{CC} = 2.3V$, $I_{UV/OV} = 2.5mA$</td>
<td>●</td>
<td>0.1</td>
<td>0.3</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{CC} = 1V$, $I_{UV} = 100\mu A$</td>
<td>●</td>
<td>0.01</td>
<td>0.15</td>
<td>V</td>
</tr>
</tbody>
</table>

**Three-State Input SEL**

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IL}$</td>
<td>Low Level Input Voltage</td>
<td>●</td>
<td>0.4</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>High Level Input Voltage</td>
<td>●</td>
<td>1.4</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_Z$</td>
<td>Pin Voltage when Left in Hi-Z State</td>
<td>$I_{SEL} = \pm 10\mu A$</td>
<td>0.7</td>
<td>0.9</td>
<td>1.1</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$-40^\circ C &lt; T_A &lt; 125^\circ C$</td>
<td>●</td>
<td>0.6</td>
<td>0.9</td>
<td>1.2</td>
</tr>
<tr>
<td>$I_{SEL}$</td>
<td>SEL High, Low Input Current</td>
<td>●</td>
<td>±30</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>$I_{SEL(MAX)}$</td>
<td>Maximum SEL Input Current</td>
<td>SEL Tied to Either $V_{CC}$ or GND</td>
<td>●</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>$t_{PW}$</td>
<td>Latch Clear Pulse Width</td>
<td>(Note 4)</td>
<td>2</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
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</table>

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** All currents into pins are positive; all voltages are referenced to GND unless otherwise noted.

**Note 3:** $V_{CC}$ maximum pin voltage is limited by input current. Since the $V_{CC}$ pin has an internal 6.5V shunt regulator, a low impedance supply that exceeds 6V may exceed the rated terminal current. Operation from higher voltage supplies requires a series dropping resistor. See Applications Information.

**Note 4:** Guaranteed by design, not subject to test.
**TIMING DIAGRAMS**

**VHn Monitor Timing**

**VHn Monitor Timing (TMR Pin Strapped to VCC)**

**VLn Monitor Timing**

**VLn Monitor Timing (TMR Pin Strapped to VCC)**

**NOTE:** WHEN AN INPUT IS CONFIGURED AS A NEGATIVE SUPPLY MONITOR, VHn WILL TRIGGER AN OV CONDITION AND VLn WILL TRIGGER A UV CONDITION

---

**TYPICAL PERFORMANCE CHARACTERISTICS**

Specifications are at $T_A = 25^\circ \text{C}$, $V_{CC} = 3.3\text{V}$ unless otherwise noted.

**Input Threshold Voltage vs Temperature**

**Supply Current vs Temperature**

**$V_{CC}$ Shunt Voltage vs Temperature**

For more information [www.linear.com/LTC2914](http://www.linear.com/LTC2914)
TYPICAL PERFORMANCE CHARACTERISTICS
Specifications are at $T_A = 25°C$, $V_{CC} = 3.3V$ unless otherwise noted.

- $V_{CC}$ Shunt Voltage vs $I_{CC}$
- Buffered Reference Voltage vs Temperature
- Transient Duration vs Comparator Overdrive

- Reset Timeout Period vs Temperature
- UV Output Voltage vs $V_{CC}$
- UV Output Voltage vs $V_{CC}$

- UV, $I_{SINK}$ vs $V_{CC}$
- UV/OV Voltage Output Low vs Output Sink Current
- Reset Timeout Period vs Capacitance

For more information www.linear.com/LTC2914
**PIN FUNCTIONS**

**DIS (Pin 13, LTC2914-2):** Output Disable Input. Disables the OV and UV output pins. When DIS is pulled high, the OV and UV pins are not asserted except during a UVLO condition. Pin has a weak (2µA) internal pull-down to GND. Leave pin open if unused.

**Exposed Pad (Pin 17, DFN Package):** Exposed Pad may be left open or connected to device ground.

**GND (Pin 9):** Device Ground

**LATCH (Pin 13, LTC2914-1):** OV Latch Clear/Bypass Input. When pulled low, OV is latched when asserted. When pulled high, OV latch is cleared. While held high, OV has the same delay and output characteristics as UV.

**OV (Pin 11):** Overvoltage Logic Output. Asserts low when any positive polarity input voltage is above threshold or any negative polarity input voltage is below threshold. Latched low (LTC2914-1). Held low for an adjustable delay time after all inputs are valid (LTC2914-2). Pin has a weak pull-up to VCC and may be pulled above VCC using an external pull-up. Leave pin open if unused.

**REF (Pin 10):** Buffered Reference Output. 1V reference used for the offset of negative-monitoring applications. The buffered reference sources and sinks up to 1mA. The reference drives capacitive loads up to 1nF. Larger capacitive loads may cause instability. Leave pin open if unused.

**SEL (Pin 14):** Input Polarity Select Three-State Input. Connect to VCC, GND or leave unconnected in open state to select one of three possible input polarity combinations (refer to Table 1).

**TMR (Pin 15):** Reset Delay Timer. Attach an external capacitor (CTMR) of at least 10pF to GND to set a reset delay time of 9ms/nF. A 1nF capacitor will generate an 8.5ms reset delay time. Tie pin to VCC to bypass timer.

**UV (Pin 12):** Undervoltage Logic Output. Asserts low when any positive polarity input voltage is below threshold or any negative polarity input voltage is above threshold. Held low for an adjustable delay time after all voltage inputs are valid. Pin has a weak pull-up to VCC and may be pulled above VCC using an external pull-up. Leave pin open if unused.

**VCC (Pin 16):** Supply Voltage. Bypass this pin to GND with a 0.1µF (or greater) capacitor. Operates as a direct supply input for voltages up to 6V. Operates as a shunt regulator for supply voltages greater than 6V and must have a resistance between the pin and the supply to limit input current to no greater than 10mA. When used without a current-limiting resistance, pin voltage must not exceed 6V.

**VH1/VH2 (Pin 1/Pin 3):** Voltage High Inputs 1 and 2. When the voltage on this pin is below 0.5V, an undervoltage condition is triggered. Tie pin to VCC if unused.

**VH3/VH4 (Pin 5/Pin 7):** Voltage High Inputs 3 and 4. The polarity of the input is selected by the state of the SEL pin (refer to Table 1). When the monitored input is configured as a positive voltage, an undervoltage condition is triggered when the pin is below 0.5V. When the monitored input is configured as a negative voltage, an overvoltage condition is triggered when the pin is above 0.5V. Tie pin to VCC if unused.

**VL1/VL2 (Pin 2/Pin 4):** Voltage Low Inputs 1 and 2. When the voltage on this pin is above 0.5V, an overvoltage condition is triggered. Tie pin to GND if unused.

**VL3/VL4 (Pin 6/Pin 8):** Voltage Low Inputs 3 and 4. The polarity of the input is selected by the state of the SEL pin (refer to Table 1). When the monitored input is configured as a positive voltage, an overvoltage condition is triggered when the pin is above 0.5V. When the monitored input is configured as a negative voltage, an undervoltage condition is triggered when the pin is above 0.5V. Tie pin to GND if unused.
Voltage Monitoring

The LTC2914 is a low power quad voltage monitoring circuit with four undervoltage and four overvoltage inputs. A timeout period that holds OV or UV asserted after all faults have cleared is adjustable using an external capacitor and is externally disabled.

Each voltage monitor has two inputs (VHn and VLn) for detecting undervoltage and overvoltage conditions. When configured to monitor a positive voltage \( V_n \) using the 3-resistor circuit configuration shown in Figure 1, VHn is connected to the high-side tap of the resistive divider and VLn is connected to the low-side tap of the resistive divider. If an input is configured as a negative voltage monitor, the outputs UVn and OVn in Figure 1 are swapped internally. \( V_n \) is then connected as shown in Figure 2. Note, VHn is still connected to the high-side tap and VLn is still connected to the low-side tap.

Polarity Selection

The three-state polarity-select pin (SEL) selects one of three possible polarity combinations for the input thresholds, as described in Table 1. When an input is configured for negative supply monitoring, VHn is configured to trigger an overvoltage condition and VLn is configured to trigger an undervoltage condition. With this configuration, an OV condition occurs when the supply voltage is more negative than the configured threshold and a UV condition occurs when the voltage is less negative than the configured threshold.

Table 1. Voltage Polarity Programming (\( V_{UOT} = 0.5V \) Typical)

<table>
<thead>
<tr>
<th>SEL</th>
<th>V3 INPUT</th>
<th>V4 INPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Positive</td>
<td>VH3 &lt; ( V_{UOT} ) → UV</td>
<td>VH4 &lt; ( V_{UOT} ) → UV</td>
</tr>
<tr>
<td>Open</td>
<td>Positive</td>
<td>Negative</td>
</tr>
<tr>
<td>GND</td>
<td>Negative</td>
<td>Negative</td>
</tr>
</tbody>
</table>

3-Step Design Procedure

The following 3-step design procedure allows selecting appropriate resistances to obtain the desired UV and OV trip points for the positive voltage monitor circuit in Figure 1 and the negative voltage monitor circuit in Figure 2. 1% resistor tolerances are suggested to maintain the ±1.5% threshold accuracy.

![Figure 1. 3-Resistor Positive UV/OV Monitoring Configuration](image1)

![Figure 2. 3-Resistor Negative UV/OV Monitoring Configuration](image2)
APPLICATIONS INFORMATION

For positive supply monitoring, $V_n$ is the desired nominal operating voltage, $I_{nd}$ is the desired nominal current through the resistive divider, $I_{na}$ is the resistive divider current calculated using the 1% resistor $R_A$. $V_{OV}$ is the desired overvoltage trip point and $V_{UV}$ is the desired undervoltage trip point.

For negative supply monitoring, to compensate for the 1V reference, 1V must be subtracted from $V_n$, $V_{OV}$ and $V_{UV}$ before using each in the following equations.

1A. Choose $R_A$ to obtain the desired OV trip point

$R_A$ is chosen to set the desired trip point for the overvoltage monitor.

$$R_A = \frac{0.5V \cdot V_n}{I_{na} \cdot V_{OV}}$$ (1)

1B. Calculate $I_{na}$

$$I_{na} = \frac{0.5V \cdot V_n}{R_A \cdot V_{OV}}$$

2. Choose $R_B$ to obtain the desired UV trip point

Once $R_A$ is known, $R_B$ is chosen to set the desired trip point for the undervoltage monitor.

$$R_B = \frac{0.5V \cdot V_n}{I_{na} \cdot V_{UV}} - R_A$$ (2)

3. Choose $R_C$ to Complete the Design

Once $R_A$ and $R_B$ are known, $R_C$ is determined by:

$$R_C = \frac{V_n}{I_{na}} - R_A - R_B$$ (3)

If any of the variables $V_n$, $I_{na}$, $I_{nd}$, $V_{UV}$ or $V_{OV}$ change, then each step must be recalculated.

Positive Voltage Monitor Example

A positive voltage monitor application is shown in Figure 3. The monitored voltage is a 5V ±10% supply. Nominal current in the resistive divider is 10µA.

1A. Find $R_A$ to set the OV trip point of the monitor.

$$R_A = \frac{0.5V \cdot 5V}{10\mu A \cdot 5.5V} = 45.3k$$

1B. Calculate $I_{na}$

$$I_{na} = \frac{0.5V \cdot 5V}{45.3k \cdot 5.5V} = 10.034\mu A$$

2. Find $R_B$ to set the UV trip point of the monitor.

$$R_B = \frac{0.5V \cdot 5V}{10.034\mu A \cdot 4.5V} - 45.3k \approx 10k$$

3. Determine $R_C$ to complete the design.

$$R_C = \frac{5V}{10.034\mu A} - 45.3k - 10k = 442k$$

Negative Voltage Monitor Example 1

A negative voltage monitor application is shown in Figure 4. The monitored voltage is a −5V ±10% supply. Nominal current in the resistive divider is 10µA. For the negative case, 1V is subtracted from $V_n$, $V_{OV}$ and $V_{UV}$.

1A. Find $R_A$ to set the OV trip point of the monitor.

$$R_A = \frac{0.5V \cdot -5V - 1V}{10\mu A \cdot -5.5V - 1V} = 46.4k$$

1B. Calculate $I_{na}$

$$I_{na} = \frac{0.5V \cdot -5V - 1V}{46.4k \cdot -5.5V - 1V} = 9.947\mu A$$

2. Find $R_B$ to set the UV trip point of the monitor.

$$R_B = \frac{0.5V \cdot -5V - 1V}{9.947\mu A \cdot -4.5V - 1V} - 46.4k \approx 8.45k$$
APPLICATIONS INFORMATION

3. Determine $R_C$ to complete the design.

$$R_C = \frac{-5V - 1V}{9.947\mu A} - 46.4k - 8.45k = 549k$$

Figure 4. Negative Supply Monitor

Negative Voltage Monitoring Example 2

Negative voltage monitoring applications with wide operating voltage ranges such that:

$$\left|2 \cdot V_{UV}\right| < \left|V_{OV}\right|$$

create situations where the VH or VL pins exceeds the −0.3V absolute maximum voltage ratings. To ensure that the LTC2914 operates within its design specifications, utilize the equations shown below to determine proper resistor sizing for the circuit in Figure 5. In the following example, the undervoltage trip point is −6V. The overvoltage trip point is −30V.

1A. Find $R_{AUV}$ and $R_{BUV}$ and let node A be a virtual ground, which ensures that the diode current will not affect the voltage monitor threshold accuracy. Let the resistive divider current $I_{nd} = 10\mu A$.

$$R_{AUV} = \left|\frac{V_{REF} - 0.5V}{I_{nd}}\right| = \left|\frac{1V - 0.5V}{10\mu A}\right| = 49.9k$$

$$R_{AUV} = R_{BUV}$$

1B. Calculate $I_{na}$ using the resistor values chosen above.

$$I_{na} = \left|\frac{V_{REF} - 0.5V}{R_{AUV}}\right| = \left|\frac{1V - 0.5V}{R_{AUV}}\right| = 10.020\mu A$$

2. Calculate $R_{CUV}$ based on the desired undervoltage trip point of −6V.

$$R_{CUV} = (R_{AUV} + R_{BUV}) \cdot \frac{V_{UV}}{V_{REF}} = (49.9k + 49.9k) \cdot \frac{-6V - 1V}{1V} = 698k$$

3. Calculate $R_{AOV}$ and $I_{na}$

$$R_{AOV} = \left|\frac{V_{REF} - 0.5V}{I_{na}}\right| = \left|\frac{1V - 0.5V}{10\mu A}\right| = 49.9k$$

$I_{na} \approx 10.020\mu A$

4. Calculate $R_{BOV}$ for a desired overvoltage trip point of −30V.

$$R_{BOV} = \left|\frac{0.5V - V_{OV}}{I_{na}}\right| = \left|\frac{0.5V - 30 - 1}{10.020\mu A}\right| = 3.01M$$

Figure 5. Negative Supply Monitor for Wide Operating Range

Power-Up/Power-Down

As soon as $V_{CC}$ reaches 1V during power-up, the $V_{UV}$ output asserts low and the $V_{OV}$ output weakly pulls to $V_{CC}$.

The LTC2914 is guaranteed to assert $V_{UV}$ low and $V_{OV}$ high under conditions of low $V_{CC}$, down to $V_{CC} = 1V$. Above $V_{CC} = 2V$ (2.1V maximum) the VH and VL inputs take control.

Once all VH inputs and $V_{CC}$ become valid an internal timer is started. After an adjustable delay time, $V_{UV}$ weakly pulls high.
Threshold Accuracy
Reset threshold accuracy is important in a supply-sensitive system. Ideally, such a system resets only if supply voltages fall outside the exact thresholds for a specified margin. All LTC2914 inputs have a relative threshold accuracy of ±1.5% over the full operating temperature range.

For example, when the LTC2914 is programmed to monitor a 5V input with a 10% tolerance, the desired UV trip point is 4.5V. Because of the ±1.5% relative accuracy of the LTC2914, the UV trip point is between 4.433V and 4.567V which is 4.5V ±1.5%.

Likewise, the accuracy of the resistances chosen for RA, RB and RC affect the UV and OV trip points as well. Using the example just given, if the resistances used to set the UV trip point have 1% accuracy, the UV trip range is between 4.354V and 4.650V. This is illustrated in the following calculations.

The UV trip point is given as:

\[ V_{UV} = 0.5V \left(1 + \frac{RC}{RA + RB}\right) \]

The two extreme conditions, with a relative accuracy of 1.5% and resistance accuracy of 1%, result in:

\[ V_{UV(MIN)} = 0.5V \cdot 0.985 \cdot \left(1 + \frac{RC \cdot 0.99}{(RA + RB) \cdot 1.01}\right) \]

and

\[ V_{UV(MAX)} = 0.5V \cdot 1.015 \cdot \left(1 + \frac{RC \cdot 1.01}{(RA + RB) \cdot 0.99}\right) \]

For a desired trip point of 4.5V, \( \frac{RC}{RA + RB} = 8 \).

Therefore,

\[ V_{UV(MIN)} = 0.5V \cdot 0.985 \cdot \left(1 + 8 \cdot \frac{0.99}{1.01}\right) = 4.354V \]

and

\[ V_{UV(MAX)} = 0.5V \cdot 1.015 \cdot \left(1 + 8 \cdot \frac{1.01}{0.99}\right) = 4.650V \]

Glitch Immunity
In any supervisory application, noise riding on the monitored DC voltage causes spurious resets. To solve this problem without adding hysteresis, which causes a new error term in the trip voltage, the LTC2914 lowpass filters the output of the first stage comparator at each input. This filter integrates the output of the comparator before asserting the UV or OV logic. A transient at the input of the comparator of sufficient magnitude and duration triggers the output logic. The Typical Performance Characteristics section shows a graph of the Transient Duration vs Comparator Overdrive.

UV/OV Timing
The LTC2914 has an adjustable timeout period (\( t_{UOTO} \)) that holds OV or UV asserted after all faults have cleared. This assures a minimum reset pulse width allowing a settling time delay for the monitored voltage after it has entered the valid region of operation.

When any VH input drops below its designed threshold, the UV pin asserts low. When all inputs recover above their designed thresholds, the UV output timer starts. If all inputs remain above their designed thresholds when the timer finishes, the UV pin weakly pulls high. However, if any input falls below its designed threshold during this time-out period, the timer resets and restarts when all inputs are above the designed thresholds. The OV output behaves as the UV output when LATCH is high (LTC2914-1).

Selecting the UV/OV Timing Capacitor
The UV and OV timeout period (\( t_{UOTO} \)) for the LTC2914 is adjustable to accommodate a variety of applications. Connecting a capacitor, \( C_{TMR} \), between the TMR pin and ground sets the timeout period. The value of capacitor needed for a particular timeout period is:

\[ C_{TMR} = t_{UOTO} \cdot 115 \cdot 10^{-9} (\text{F/s}) \]

The Reset Timeout Period vs Capacitance graph found in the Typical Performance Characteristics shows the desired delay time as a function of the value of the timer capacitor that must be used. The TMR pin must have a minimum of 10pF or be tied to VCC. For long timeout periods, the only limitation is the availability of a large value capacitor with
APPLICATIONS INFORMATION

low leakage. Capacitor leakage current must not exceed the minimum TMR charging current of 1.3µA. Tying the TMR pin to VCC bypasses the timeout period.

Undervoltage Lockout

When VCC falls below 2V, the LTC2914 asserts an undervoltage lockout (UVLO) condition. During UVLO, UV is asserted and pulled low while OV is cleared and blocked from asserting. When VCC rises above 2V, UV follows the same timing procedure as an undervoltage condition on any input.

Shunt Regulator

The LTC2914 has an internal shunt regulator. The VCC pin operates as a direct supply input for voltages up to 6V. Under this condition, the quiescent current of the device remains below a maximum of 100µA. For VCC voltages higher than 6V, the device operates as a shunt regulator and must have a resistance RZ between the supply and the VCC pin to limit the current to no greater than 10mA.

When choosing this resistance value, choose an appropriate location on the I-V curve shown in the Typical Performance Characteristics section to accommodate variations in VCC due to changes in current through RZ.

UV and OV Output Characteristics

The DC characteristics of the UV and OV pull-up and pull-down strength are shown in the Typical Performance Characteristics section. Each pin has a weak internal pull-up to VCC and a strong pull-down to ground. This arrangement allows these pins to have open-drain behavior while possessing several other beneficial characteristics. The weak pull-up eliminates the need for an external pull-up resistor when the rise time on the pin is not critical. On the other hand, the open-drain configuration allows for wired-OR connections and is useful when more than one signal needs to pull down on the output. VCC of 1V guarantees a maximum VOL = 0.15V at UV.

At VCC = 1V, the weak pull-up current on OV is barely turned on. Therefore, an external pull-up resistor of no more than 100kΩ is recommended on the OV pin if the state and pull-up strength of the OV pin is crucial at very low VCC.

Note however, by adding an external pull-up resistor, the pull-up strength on the OV pin is increased. Therefore, if it is connected in a wired-OR connection, the pull-down strength of any single device must accommodate this additional pull-up strength.

Output Rise and Fall Time Estimation

The UV and OV outputs have strong pull-down capability. The following formula estimates the output fall time (90% to 10%) for a particular external load capacitance (CLOAD):

\[ t_{\text{FALL}} \approx 2.2 \cdot R_{PD} \cdot C_{LOAD} \]

Note however, by adding an external pull-up resistor, the pull-up strength on the OV pin is increased. Therefore, if it is connected in a wired-OR connection, the pull-down strength of any single device must accommodate this additional pull-up strength.

Output Rise and Fall Time Estimation

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\[ t_{\text{FALL}} \approx 2.2 \cdot R_{PD} \cdot C_{LOAD} \]

where RPD is the on-resistance of the internal pull-down transistor, typically 50Ω at VCC > 1V and at room temperature (25°C). CLOAD is the external load capacitance on the pin. Assuming a 150pF load capacitance, the fall time is 16.5ns.

The rise time on the UV and OV pins is limited by a 400kΩ pull-up resistance to VCC. A similar formula estimates the output rise time (10% to 90%) at the UV and OV pins:

\[ t_{\text{RISE}} \approx 2.2 \cdot R_{PU} \cdot C_{LOAD} \]

where RPU is the pull-up resistance.

OV Latch (LTC2914-1)

With the LATCH pin held low, the OV pin latches low when an OV condition is detected. The latch is cleared by raising the LATCH pin high. If an OV condition changes while LATCH is held high, the latch is bypassed and the OV pin behaves the same as the UV pin with a similar timeout period at the output. If LATCH is pulled low while the timeout period is active, the OV pin latches as before.

Disable (LTC2914-2)

The LTC2914-2 allows disabling the UV and OV outputs via the DIS pin. Pulling DIS high forces both outputs to remain weakly pulled high, regardless of any faults that occur on the inputs. However, if a UVLO condition occurs, UV asserts and pulls low, but the timeout function is bypassed. UV pulls high as soon as the UVLO condition is cleared.

DIS has a weak 2µA (typical) internal pull-down current guaranteeing normal operation with the pin left open.

For more information www.linear.com/LTC2914
Quad UV/OV Supply Monitor, 10% Tolerance, 5V, 3.3V, 2.5V, 1.8V

Dual Positive and Dual Negative UV/OV Supply Monitor, 10% Tolerance, 5V, 3.3V, –5V, –3.3V

For more information www.linear.com/LTC2914
TYPICAL APPLICATIONS

Triple UV/OV Supply Monitor Powered from 48V, 10% Tolerance, 48V, 5V, 2.5V

For more information www.linear.com/LTC2914
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DHC Package
16-Lead Plastic DFN (5mm × 3mm)
(Reference LTC DWG # 05-08-1706 Rev B)

RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WJED-1) IN JEDEC
   PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE
   TOP AND BOTTOM OF PACKAGE

GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641 Rev B)

RECOMMENDED SOLDER PAD LAYOUT

NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING NOT TO SCALE
4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE
   *DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH
   SHALL NOT EXCEED 0.005" (0.127mm) PER SIDE
   **DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD
   FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

For more information www.linear.com/LTC2914
## Revision History

(Revision history begins at Rev B)

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<td>10/10</td>
<td>Added $I_{PW}$ and Note 4 to Electrical Characteristics section</td>
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<td></td>
<td></td>
<td>Updated equations and added Negative Voltage Monitoring Example 2 to Applications Information section</td>
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<tr>
<td>C</td>
<td>12/13</td>
<td>Corrected LATCH/DIS label in Pin Configuration section</td>
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Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.
Quad UV/OV Supply Monitor with LED Undervoltage and Overvoltage Indicator and Manual Undervoltage Reset Button, 10% Tolerance, 12V, 5V, 3.3V, 2.5V

**RELATED PARTS**

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<td>4.725V, 3.118V, 1V Threshold (±0.75%)</td>
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