 FEATURES

- Program or Pin-Strap Six Output Ranges
  0V to 5V, 0V to 10V, −2.5V to 7.5V, ±2.5V, ±5V, ±10V
- Maximum 16-Bit INL Error: ±1 LSB over Temperature
- Guaranteed Monotonic over Temperature
- Low Glitch Impulse 0.26nV•s (3V), 1.25nV•s (5V)
- Serial Readback of All On-Chip Registers
- Low 1μA Maximum Supply Current
- 2.7V to 5.5V Single-Supply Operation
- 16-Bit Settling Time: 2μs
- Voltage-Controlled Offset and Gain Trims
- Clear and Power-On-Reset to 0V Regardless of Output Range
- 52-Pin 7mm × 8mm QFN Package

 APPLICATIONS

- High Resolution Offset and Gain Adjustment
- Process Control and Industrial Automation
- Automatic Test Equipment
- Data Acquisition Systems

 DESCRIPTION

The LTC®2754 is a family of quad 12- and 16-bit multiplying serial-input, current-output digital-to-analog converters. They operate from a single 3V to 5V supply and are guaranteed monotonic over temperature. The LTC2754A-16 provides full 16-bit performance (±1LSB INL and DNL, max) over temperature without any adjustments. These SoftSpan™ DACs offer six output ranges (up to ±10V) that can be programmed through the 3-wire SPI serial interface, or pinstrapped for operation in a single range.

The content of any on-chip register (including DAC output-range settings) can be verified in just one instruction cycle; and if you change any register, that register will be automatically read back during the next instruction cycle.

Voltage-controlled offset and gain adjustments are also provided; and the power-on reset circuit and CLR pin both reset the DAC outputs to 0V regardless of output range.

 L T, LT, LTC, LTM, Linear Technology and the Linear logo are registered trademarks of Linear Technology Corporation. SoftSpan is a trademark of Linear Technology Corporation. All other trademarks are the property of their respective owners. Protected by U.S. Patents, including 5481178.
ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

- I\textsubscript{OUT1X}, I\textsubscript{OUT2X} to GND: \pm 0.3V
- R\textsubscript{INX}, R\textsubscript{COMX}, R\textsubscript{EXF}, R\textsubscript{FBX}, R\textsubscript{OFSX}, V\textsubscript{OSADJX}, GEADJX to GND: \pm 18V
- V\textsubscript{DD} to GND: \pm 0V to 7V
- Digital Inputs and Outputs to GND: \pm 0V to V\textsubscript{DD}+0.3V (max 7V)
- Operating Temperature Range
  - LTC2754C: 0°C to 70°C
  - LTC2754I: –40°C to 85°C
- Maximum Junction Temperature: 150°C
- Storage Temperature Range: –65°C to 150°C

ORDER INFORMATION

<table>
<thead>
<tr>
<th>LEAD FREE FINISH</th>
<th>TAPE AND REEL</th>
<th>PART MARKING*</th>
<th>PACKAGE DESCRIPTION</th>
<th>TEMPERATURE RANGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>LTC2754CUKG-12#PBF</td>
<td>LTC2754CUKG-12#TRPBF</td>
<td>LTC2754UKG-12</td>
<td>52-Lead (7mm \times 8mm) Plastic QFN</td>
<td>0°C to 70°C</td>
</tr>
<tr>
<td>LTC2754IUKG-12#PBF</td>
<td>LTC2754IUKG-12#TRPBF</td>
<td>LTC2754UKG-12</td>
<td>52-Lead (7mm \times 8mm) Plastic QFN</td>
<td>–40°C to 85°C</td>
</tr>
<tr>
<td>LTC2754BCUKG-16#PBF</td>
<td>LTC2754BCUKG-16#TRPBF</td>
<td>LTC2754UKG-16</td>
<td>52-Lead (7mm \times 8mm) Plastic QFN</td>
<td>0°C to 70°C</td>
</tr>
<tr>
<td>LTC2754IUKG-16#PBF</td>
<td>LTC2754IUKG-16#TRPBF</td>
<td>LTC2754UKG-16</td>
<td>52-Lead (7mm \times 8mm) Plastic QFN</td>
<td>–40°C to 85°C</td>
</tr>
<tr>
<td>LTC2754ACUKG-16#PBF</td>
<td>LTC2754ACUKG-16#TRPBF</td>
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<td>0°C to 70°C</td>
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<tr>
<td>LTC2754AIUKG-16#PBF</td>
<td>LTC2754AIUKG-16#TRPBF</td>
<td>LTC2754UKG-16</td>
<td>52-Lead (7mm \times 8mm) Plastic QFN</td>
<td>–40°C to 85°C</td>
</tr>
</tbody>
</table>

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: [http://www.linear.com/leadfree/](http://www.linear.com/leadfree/)

For more information on tape and reel specifications, go to: [http://www.linear.com/tapeandreel/](http://www.linear.com/tapeandreel/)
### ELECTRICAL CHARACTERISTICS

V\(_{DD}\) = 5V, V\(_{REF}\) = 5V unless otherwise specified. The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at TA = 25°C.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>LTC2754-12</th>
<th>LTC2754B-16</th>
<th>LTC2754A-16</th>
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<tbody>
<tr>
<td></td>
<td></td>
<td>MIN</td>
<td>TYP</td>
<td>MAX</td>
<td>MIN</td>
</tr>
<tr>
<td></td>
<td></td>
<td>UNITS</td>
<td>Bits</td>
<td>Bits</td>
<td>LSB</td>
</tr>
<tr>
<td>Static Performance</td>
<td></td>
<td></td>
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<tr>
<td>Resolution</td>
<td>●</td>
<td>12</td>
<td>16</td>
<td>16</td>
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<tr>
<td>Monotonicity</td>
<td>●</td>
<td>12</td>
<td>16</td>
<td>16</td>
<td></td>
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<tr>
<td>DNL</td>
<td>Differential Nonlinearity</td>
<td>●</td>
<td>±1</td>
<td>±1</td>
<td>±0.2</td>
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<tr>
<td>INL</td>
<td>Integral Nonlinearity</td>
<td>●</td>
<td>±1</td>
<td>±2</td>
<td>±0.4</td>
</tr>
<tr>
<td>GE</td>
<td>Gain Error</td>
<td>All Output Ranges</td>
<td>●</td>
<td>±0.5</td>
<td>±2</td>
</tr>
<tr>
<td></td>
<td>Gain Error Temperature Coefficient</td>
<td>ΔGain/ΔTemp</td>
<td>●</td>
<td>±1</td>
<td>±1</td>
</tr>
<tr>
<td>BZE</td>
<td>Bipolar Zero Error</td>
<td>All Bipolar Ranges</td>
<td>●</td>
<td>±0.2</td>
<td>±1</td>
</tr>
<tr>
<td></td>
<td>Bipolar Zero Temperature Coefficient</td>
<td></td>
<td></td>
<td>±0.5</td>
<td>±0.5</td>
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<tr>
<td>PSR</td>
<td>Power Supply Rejection</td>
<td>V(_{DD}) = 5V, ±10%</td>
<td>●</td>
<td>±0.025</td>
<td>±0.06</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V(_{DD}) = 3V, ±10%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>I(_{LKG})</td>
<td>I(_{OUT1}) Leakage Current</td>
<td>TA = 25°C</td>
<td>●</td>
<td>±0.05</td>
<td>±2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TMIN to TMAX</td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>

V\(_{DD}\) = 5V, V\(_{REF}\) = 5V unless otherwise specified. The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at TA = 25°C.

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS | |
|--------|-----------|------------|-----|-----|-----|-------| |
| Analog Pins | | Reference Inverting Resistors (Note 4) | ● | 16 | 20 | kΩ | |
| | | DAC Input Resistance | | 8 | 10 | kΩ | |
| | | Feedback Resistors (Note 3) | ● | 8 | 10 | kΩ | |
| | | Bipolar Offset Resistors (Note 3) | ● | 16 | 20 | kΩ | |
| | | Offset Adjust Resistors | ● | 1024 | 1280 | kΩ | |
| | | Gain Adjust Resistors | ● | 2048 | 2560 | kΩ | |
| | | Output Capacitance | Full-Scale | 75 | | pF | |
| | | | Zero-SCALE | 45 | | | |
| Dynamic Performance | | Output Settling Time | 0V to 10V Range, 10V Step. To ±0.0015% FS (Note 5) | 2 | | μs | |
| | | Glitch Impulse | V\(_{DD}\) = 5V (Note 6) | 1.25 | 0.26 | nV•s | |
| | | | V\(_{DD}\) = 3V (Note 6) | | | | |
| | | Digital-to-Analog Glitch Impulse (Note 7) | 2 | | nV•s | |
| | | Reference Multiplying BW | 0V to 5V Range, V\(_{REF}\) = 3VRMS. Code = Full Scale, –3dB BW | 2 | | MHz | |
| | | Multiplying Feedthrough Error | 0V to 5V Range, V\(_{REF}\) = ±10V, 10kHz Sine Wave | 0.5 | | mV | |
| | | Analog Crosstalk (Note 8) | | | | | dB | |
| | | THD | Total Harmonic Distortion (Note 9) Multiplying | | | | | dB | |
| | | Output Noise Voltage Density (Note 10) at I\(_{OUT1}\) | | | | | 13 | nV/√Hz | |
## ELECTRICAL CHARACTERISTICS

$V_{DD} = 5V, V_{REF} = 5V$ unless otherwise specified. The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ C$.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD}$</td>
<td>Supply Voltage</td>
<td>●</td>
<td>2.7</td>
<td>5.5</td>
<td>V</td>
<td></td>
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<tr>
<td>$I_{DD}$</td>
<td>Supply Current, $V_{DD}$</td>
<td>●</td>
<td>0.5</td>
<td>1</td>
<td>μA</td>
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### Digital Inputs

<table>
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<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IH}$</td>
<td>Digital Input High Voltage</td>
<td>$3.3V \leq V_{DD} \leq 5.5V$</td>
<td>●</td>
<td>2.4</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Digital Input Low Voltage</td>
<td>$4.5V &lt; V_{DD} \leq 5.5V$</td>
<td>●</td>
<td>0.8</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Digital Input Low Voltage</td>
<td>$2.7V \leq V_{DD} \leq 4.5V$</td>
<td>●</td>
<td>0.6</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{IN}$</td>
<td>Digital Input Current</td>
<td>$V_{IN} = GND$ to $V_{DD}$</td>
<td>●</td>
<td>±1</td>
<td></td>
<td>μA</td>
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<tr>
<td>$C_{IN}$</td>
<td>Digital Input Capacitance</td>
<td>$V_{IN} = 0V$ (Note 11)</td>
<td>●</td>
<td>6</td>
<td></td>
<td>pF</td>
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### Digital Outputs

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OH}$</td>
<td>$I_{OH} = 200\mu A$</td>
<td>$2.7V \leq V_{DD} \leq 5.5V$</td>
<td>●</td>
<td>$V_{DD} - 0.4$</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>$I_{OL} = 200\mu A$</td>
<td>$2.7V \leq V_{DD} \leq 5.5V$</td>
<td>●</td>
<td>0.4</td>
<td></td>
<td>V</td>
</tr>
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</table>

## TIMING CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ C$.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
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<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD} = 4.5V$ to $5.5V$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_1$</td>
<td>SDI Valid to SCK Set-Up</td>
<td>●</td>
<td>7</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_2$</td>
<td>SDI Valid to SCK Hold</td>
<td>●</td>
<td>7</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_3$</td>
<td>SCK High Time</td>
<td>●</td>
<td>11</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_4$</td>
<td>SCK Low Time</td>
<td>●</td>
<td>11</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_5$</td>
<td>$CS/LD$ Pulse Width</td>
<td>●</td>
<td>9</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_6$</td>
<td>LSB SCK High to $CS/LD$ High</td>
<td>●</td>
<td>4</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_7$</td>
<td>$CS/LD$ Low to SCK Positive Edge</td>
<td>●</td>
<td>4</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_8$</td>
<td>$CS/LD$ High to SCK Positive Edge</td>
<td>●</td>
<td>4</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_9$</td>
<td>SRO Propagation Delay</td>
<td>$C_{LOAD} = 10pF$</td>
<td>●</td>
<td>18</td>
<td></td>
<td>ns</td>
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<tr>
<td>$t_{10}$</td>
<td>CLR Pulse Width Low</td>
<td>●</td>
<td>36</td>
<td></td>
<td>ns</td>
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</tr>
<tr>
<td>$t_{11}$</td>
<td>LDAC Pulse Width Low</td>
<td>●</td>
<td>15</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_{12}$</td>
<td>CLR Low to RFLAG Low</td>
<td>$C_{LOAD} = 10pF$ (Note 11)</td>
<td>●</td>
<td>50</td>
<td></td>
<td>ns</td>
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<tr>
<td>$t_{13}$</td>
<td>$CS/LD$ High to RFLAG High</td>
<td>$C_{LOAD} = 10pF$ (Note 11)</td>
<td>●</td>
<td>40</td>
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<td>ns</td>
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<tr>
<td></td>
<td>SCK Frequency</td>
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<tr>
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<td></td>
<td></td>
<td></td>
<td></td>
<td>50% Duty Cycle (Note 12)</td>
<td>●</td>
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<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
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<tbody>
<tr>
<td>$V_{DD} = 2.7V$ to $3.3V$</td>
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<tr>
<td>$t_1$</td>
<td>SDI Valid to SCK Set-Up</td>
<td>(Note 11)</td>
<td>9</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_2$</td>
<td>SDI Valid to SCK Hold</td>
<td></td>
<td>9</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_3$</td>
<td>SCK High Time</td>
<td>$C_L = 10pF$</td>
<td>●</td>
<td>15</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_4$</td>
<td>SCK Low Time</td>
<td></td>
<td>15</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_5$</td>
<td>$CS/LD$ Pulse Width</td>
<td></td>
<td>12</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_6$</td>
<td>LSB SCK High to $CS/LD$ High</td>
<td></td>
<td>5</td>
<td></td>
<td>ns</td>
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</table>
**TIMING CHARACTERISTICS**

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ C$.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_7$</td>
<td>CS/LD Low to SCK Positive Edge</td>
<td>●</td>
<td>5 ns</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>$t_8$</td>
<td>CS/LD High to SCK Positive Edge</td>
<td>●</td>
<td>5 ns</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_9$</td>
<td>SRO Propagation Delay</td>
<td>$C_{LOAD} = 10pF$</td>
<td>●</td>
<td>26 ns</td>
<td></td>
<td></td>
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<tr>
<td>$t_{10}$</td>
<td>CLR Pulse Width Low</td>
<td>●</td>
<td>60 ns</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>$t_{11}$</td>
<td>LDAC Pulse Width Low</td>
<td>●</td>
<td>20 ns</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{12}$</td>
<td>CLR Low to RFLAG Low</td>
<td>$C_{LOAD} = 10pF$ (Note 11)</td>
<td>●</td>
<td>70 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{13}$</td>
<td>CS/LD High to RFLAG high</td>
<td>$C_{LOAD} = 10pF$ (Note 11)</td>
<td>●</td>
<td>60 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SCK Frequency</td>
<td>50% Duty Cycle (Note 12)</td>
<td>●</td>
<td>25 MHz</td>
<td></td>
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<td></td>
</tr>
</tbody>
</table>

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** Continuous operation above the specified maximum operating junction temperature may impair device reliability.

**Note 3:** Because of the proprietary SoftSpan switching architecture, the measured resistance looking into each of the specified pins is constant for all output ranges if the $I_{OUT1X}$ and $I_{OUT2X}$ pins are held at ground.

**Note 4:** Input resistors measured from $R_{INX}$ to $R_{COMX}$; feedback resistors measured from $R_{COMX}$ to $REFX$.

**Note 5:** Using LT1469 with $C_{FEEDBACK} = 15pF$. A ±0.0015% settling time of 1.7 μs can be achieved by optimizing the time constant on an individual basis. See Application Note 74, Component and Measurement Advances Ensure 16-Bit DAC Settling Time.

**Note 6:** Measured at the major carry transition, 0V to 5V range. Output amplifier: LT1469; $C_{FB} = 27pF$.

**Note 7:** Full-scale transition; $REF = 0V$.

**Note 8:** Analog Crosstalk is defined as the AC voltage ratio $V_{OUTB}/V_{REFA}$, expressed in dB. $REFB$ is grounded, and DAC B is set to 0V-5V span and zero-, mid- or full- scale code. $V_{REFA}$ is a 3VRMS, 1kHz sine wave. Crosstalk between other DAC channels is similar or better.

**Note 9:** $REF = 6V_{RMS}$ at 1kHz. 0V to 5V range. DAC code = FS. Output amplifier = LT1469.

**Note 10:** Calculation from $V_n = \sqrt{4kTRB}$, where $k = 1.38E-23$ J/°K (Boltzmann constant), $R = $ resistance (Ω), $T = $ temperature (°K), and $B = $ bandwidth (Hz). 0V to 5V Range; zero-, mid-, or full- scale.

**Note 11:** Guaranteed by design, not subject to test.

**Note 12:** When using SRO, maximum SCK frequency $f_{MAX}$ is limited by SRO propagation delay $t_9$ as follows:

$$f_{MAX} = \left(\frac{1}{2(t_9 + t_S)}\right),$$

where $t_S$ is the setup time of the receiving device.

---

**TYPICAL PERFORMANCE CHARACTERISTICS**

$T_A = 25^\circ C$, unless otherwise noted.

**LTC2754-16**

![Intrinsic Nonlinearity (INL)](image)

![Differential Nonlinearity (DNL)](image)

![INL vs Temperature](image)
TYPICAL PERFORMANCE CHARACTERISTICS

$V_{DD} = 5V$

$V_{REF} = 5V$

$\pm5V$ RANGE

$-1.0$ INL (LSB)

$-0.8$

$-0.4$

$-0.2$

$0.0$

$1.0$

$0.4$

$0.6$

$0.8$

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$-1.0$

$-0.6$

$-0.4$

$-0.2$

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$-0.2$

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$1.0$

$0.4$

$0.6$

$0.8$

$1.0$
### LTC2754

**TYPICAL PERFORMANCE CHARACTERISTICS**  \( T_A = 25^\circ C, \text{unless otherwise noted.} \)

#### LTC2754-12

**Integral Nonlinearity (INL)**
- \( V_{DD} = 5V, V_{REF} = 5V, \pm 10V \text{ RANGE} \)

**Differential Nonlinearity (DNL)**
- \( V_{DD} = 5V, V_{REF} = 5V, \pm 10V \text{ RANGE} \)

### Supply Current vs Logic Input Voltage

- **CLR, LDAC, SDL, SCK, CS/LD TIED TOGETHER**
- \( V_{DD} = 5V, V_{DD} = 2V \)

### Logic Threshold vs Supply Voltage

- **RISING, FALLING**
- \( V_{DD} = 5V, V_{DD} = 3V \)

### Supply Current vs Clock Frequency

- \( V_{DD} = 5V, V_{DD} = 3V \)
- \( 100 \text{kHz} \) to \( 100 \text{MHz} \)

### Midscale Glitch

- \( CS/LD, 2V/DIV \)
- \( 0.26nV/\mu\text{s TYP} \)
- \( V_{OUT} = 5mV/DIV \)
- \( V_{DD} = 3V, V_{REF} = 5V, 5V \text{ RANGE} \)
- \( \text{LT1468 OUTPUT AMPLIFIER} \)
- \( C_{\text{FEEDBACK}} = 27pF \)
- **RISING MAJOR CARRY TRANSITION. FALLING TRANSITION IS SIMILAR OR BETTER**

### Midscale Glitch

- \( CS/LD, 5V/DIV \)
- \( 1.25nV/\mu\text{s TYP} \)
- \( V_{OUT} = 5mV/DIV \)
- \( V_{DD} = 5V, V_{REF} = 5V, 5V \text{ RANGE} \)
- \( \text{LT1468 OUTPUT AMPLIFIER} \)
- \( C_{\text{FEEDBACK}} = 27pF \)
- **RISING MAJOR CARRY TRANSITION. FALLING TRANSITION IS SIMILAR OR BETTER**

### Settling 0V to 10V

- **USING LT1469 AMP**
- \( C_{\text{FEEDBACK}} = 12pF, 0V \text{ TO } 10V \text{ STEP} \)
- \( 500\mu\text{s/DIV} \)
**PIN FUNCTIONS**

**GEADJA (Pin 1):** Gain Adjust Pin for DAC A. This control pin can be used to null gain error or to compensate for reference errors. Nominal adjustment range is ±512 LSB (LTC2754-16) for a voltage input range of ±V_{RINA} (i.e., ±5V for a 5V reference input). Tie to ground if not used.

**R_{INA} (Pin 2):** Input Resistor for Reference Inverting Amplifier. The 20k input resistor is connected internally from R_{INA} to R_{COMA}. For normal operation tie R_{INA} to the external reference voltage V_{REFA} (see Typical Applications). Any or all of these precision-matched resistor sets (Each set comprising R_{INX}, R_{COMX} and REFX) may be used to invert one or more positive reference voltages to the negative voltages needed by the DACs. Typically 5V; accepts up to ±15V.

**I_{OUT2A} (Pin 3):** DAC A Current Output Complement. Tie I_{OUT2A} to ground.

**GND (Pin 4):** Ground; provides shielding for I_{OUT2A}. Tie to ground.

**CS/LD (Pin 5):** Synchronous Chip Select and Load Pin.

**SDI (Pin 6):** Serial Data Input. Data is clocked in on the rising edge of the serial clock (SCK) when CS/LD is low.

**SCK (Pin 7):** Serial Clock.

**SRO (Pin 8):** Serial Readback Output. Data is clocked out on the falling edge of SCK. Readback data begins clocking out after the last address bit A0 is clocked in. SRO is an active output only when the chip is selected (i.e., when CS/LD is low). Otherwise SRO presents a high-impedance output in order to allow other parts to control the bus.

**SROGND (Pin 9):** Ground pin for SRO. Tie to ground.

**V_{DD} (Pin 10):** Positive Supply Input; 2.7V ≤ V_{DD} ≤ 5.5V. By-pass with a 0.1μF low-ESR ceramic capacitor to ground.

**GND (Pin 11):** Ground. Tie to ground.

**I_{OUT2D} (Pin 12):** DAC D Current Output Complement. Tie I_{OUT2D} to ground.

**R_{IND} (Pin 13):** Input Resistor for Reference Inverting Amplifier. The 20k input resistor is connected internally from R_{IND} to R_{COMD}. For normal operation tie R_{IND} to the external reference voltage V_{REFD} (see Typical Applications). Any or all of these precision-matched resistor sets (Each set comprising R_{INX}, R_{COMX} and REFX) may be used to invert one or more positive reference voltages to the negative voltages needed by the DACs. Typically 5V; accepts up to ±15V.

**GEADJD (Pin 14):** Gain Adjust Pin for DAC D. This control pin can be used to null gain error or to compensate for reference errors. Nominal adjustment range is ±512 LSB (LTC2754-16) for a voltage input range of ±V_{RIND} (i.e., ±5V for a 5V reference input). Tie to ground if not used.

**R_{COMD} (Pin 15):** Center Tap Point for Reference Amplifier Inverting Resistors. The 20k reference inverting resistors are connected internally from R_{IND} to R_{COMD} and from R_{COMD} to REFD, respectively (see Block Diagram). For normal operation tie R_{COMD} to the negative input of external reference inverting amplifier (see Typical Applications).

**REFD (Pin 16):** Inverted Reference Voltage for DAC D, with internal connection to the reference inverting resistor. The 20k resistor is connected internally from R_{IND} to R_{COMD} and from R_{COMD} to REFD, respectively (see Block Diagram). For normal operation tie R_{COMD} to the negative input of external reference inverting amplifier (see Typical Applications). Typically –5V; accepts up to ±15V. The impedance looking into this pin is 10k to ground (R_{IND} and R_{COMD} floating).

**R_{OFSD} (Pin 17):** Bipolar Offset Network for DAC D. This pin provides the translation of the output voltage range for bipolar spans. Accepts up to ±15V; for normal operation tie to the positive reference voltage at R_{IND} (Pin 13). The impedance looking into this pin is 20k to ground.

**R_{FBD} (Pin 18):** DAC D Feedback Resistor. For normal operation tie to the output of the I/V converter amplifier for DAC D (see Typical Applications). The DAC output current from I_{OUT1D} flows through the feedback resistor to the R_{FBD} pin. The impedance looking into this pin is 10k to ground.

**I_{OUT1D} (Pin 19):** DAC D Current Output. This pin is a virtual ground when the DAC is operating and should reside at 0V. For normal operation tie to the negative input of the I/V converter amplifier for DAC D (see Typical Applications).
PIN FUNCTIONS

VOSADJD (Pin 20): DAC D Offset Adjust Pin. This control pin can be used to null unipolar offset or bipolar zero error. The offset voltage delta is inverted and attenuated such that a 5V control voltage applied to VOSADJD produces ΔVOS = -512 LSB (LTC2754-16) in any output range (assumes a 5V reference voltage at RIND). Tie to ground if not used.

VOSADJC (Pin 21): DAC C Offset Adjust Pin. This control pin can be used to null unipolar offset or bipolar zero error. The offset voltage delta is inverted and attenuated such that a 5V control voltage applied to VOSADJC produces ΔVOS = -512 LSB (LTC2754-16) in any output range (assumes a 5V reference voltage at RINC). Tie to ground if not used.

IOUT1C (Pin 22): DAC C Current Output. This pin is a virtual ground when the DAC is operating and should reside at 0V. For normal operation tie to the negative input of the I/V converter amplifier for DAC C (see Typical Applications).

RFBC (Pin 23): DAC C Feedback Resistor. For normal operation tie to the output of the I/V converter amplifier for DAC C (see Typical Applications). The DAC output current from IOUT1D flows through the feedback resistor to the RFBC pin. The impedance looking into this pin is 10k to ground.

ROFSC (Pin 24): Bipolar Offset Network for DAC C. This pin provides the translation of the output voltage range for bipolar spans. Accepts up to ±15V; for normal operation tie to the positive reference voltage at RINC (Pin 28). The impedance looking into this pin is 20k to ground.

REFC (Pin 25): Inverted Reference Voltage for DAC C, with internal connection to the reference inverting resistor. The 20k resistor is connected internally from REFC to RCOMC. For normal operation tie this pin to the output of reference inverting amplifier (see Typical Applications). Typically –5V; accepts up to ±15V. The impedance looking into this pin is 10k to ground (RINC and RCOMC floating).

RCOMC (Pin 26): Center Tap Point for Reference Amplifier Inverting Resistors. The 20k reference inverting resistors are connected internally from RINC to RCOMC and from RCOMC to REFC, respectively (see Block Diagram). For normal operation tie RCOMC to the negative input of external reference inverting amplifier (see Typical Applications).

GEADJC (Pin 27): Gain Adjust Pin for DAC C. This control pin can be used to null gain error or to compensate for reference errors. Nominal adjustment range is ±512 LSB (LTC2754-16) for a voltage input range of ±VRINC (i.e., ±5V for a 5V reference input). Tie to ground if not used.

RINC (Pin 28): Input Resistor for Reference Inverting Amplifier. The 20k input resistor is connected internally from RINC to RCOMC. For normal operation tie RINC to the external reference voltage VREFC (see Typical Applications). Any or all of these precision-matched resistor sets (Each set comprising RINX, RCOMX and REFX) may be used to invert one or more positive reference voltages to the negative voltages needed by the DACs. Typically 5V; accepts up to ±15V.

IOUT2C (Pin 29): DAC C Current Output Complement. Tie IOUT2C to ground.

CLR (Pin 30): Asynchronous Clear Pin. When this pin is low, all DAC registers (both code and span) are cleared to zero. All DAC outputs are cleared to zero volts.

RFLAG (Pin 31): Reset Flag Pin. An active low output is asserted when there is a power-on reset or a clear event. Returns high when an Update command is executed.

M-SPAN (Pin 32): Manual Span Control Pin. M-SPAN is used in conjunction with pins S2, S1 and S0 (Pins 33, 34 and 35) to configure all DACs for operation in a single, fixed output range.

To configure the part for manual-span use, tie M-SPAN directly to VDD. The active output range is then set via hardware pin strapping of pins S2, S1 and S0 (rather than through the SPI port); and Write and Update commands have no effect on the active output span.

To configure the part for SoftSpan use, tie M-SPAN directly to GND. The output ranges are then individually and dynamically controllable through the SPI port; and pins S2, S1 and S0 have no effect.

See ‘Manual Span Configuration’ in the Operation section. M-SPAN must be connected either directly to GND (SoftSpan configuration) or to VDD (manual-span configuration).
**PIN FUNCTIONS**

**S0 (Pin 33):** Span Bit 0. In Manual Span mode (M-SPAN tied to VDD), Pins S0, S1 and S2 are pin-strapped to select a single fixed output range for all DACs. These pins should be tied to either GND or VDD even if they are unused.

**S1 (Pin 34):** Span Bit 1. In Manual Span mode (M-SPAN tied to VDD), Pins S0, S1 and S2 are pin-strapped to select a single fixed output range for all DACs. These pins should be tied to either GND or VDD even if they are unused.

**S2 (Pin 35):** Span Bit 2. In Manual Span mode (M-SPAN tied to VDD), Pins S0, S1 and S2 are pin-strapped to select a single fixed output range for all DACs. These pins should be tied to either GND or VDD even if they are unused.

**LDAC (Pin 36):** Asynchronous DAC Load Input. When LDAC is a logic low, all DACs are updated (CS/LD must be high).

**GND (Pin 37):** Ground; provides shielding for IOUT2B. Tie to ground.

**IOUT2B (Pin 38):** DAC B Current Output Complement. Tie IOUT2B to ground.

**RINB (Pin 39):** Input Resistor for Reference Inverting Amplifier. The 20k input resistor is connected internally from RINB to RCOMB. For normal operation tie RINB to the external reference voltage VREFB (see Typical Applications). Any or all of these precision-matched resistor sets (Each set comprising RINX, RCOMX and REFX) may be used to invert one or more positive reference voltages to the negative voltages needed by the DACs. Typically 5V; accepts up to ±15V.

**GEADJB (Pin 40):** Gain Adjust Pin for DAC B. This control pin can be used to null gain error or to compensate for reference errors. Nominal adjustment range is ±512 LSB (LTC2754-16) for a voltage input range of ±VRINB (i.e., ±5V for a 5V reference input). Tie to ground if not used.

**RCOMB (Pin 41):** Center Tap Point for Reference Amplifier Inverting Resistors. The 20k reference inverting resistors are connected internally from RINB to RCOMB and from RCOMB to RFB, respectively (see Block Diagram). For normal operation tie RCOMB to the negative input of external reference inverting amplifier (see Typical Applications).

**REFB (Pin 42):** Inverted Reference Voltage for DAC B, with internal connection to the reference inverting resistor. The 20k resistor is connected internally from REFB to RCOMB. For normal operation tie this pin to the output of reference inverting amplifier (see Typical Applications). Typically –5V; accepts up to ±15V. The impedance looking into this pin is 10k to ground (RINB and RCOMB floating).

**RREFB (Pin 43):** Bipolar Offset Network for DAC B. This pin provides the translation of the output voltage range for bipolar spans. Accepts up to ±15V; for normal operation tie to the positive reference voltage at RINB (Pin 39). The impedance looking into this pin is 20k to ground.

**RFBB (Pin 44):** DAC B Feedback Resistor. For normal operation tie to the output of the I/V converter amplifier for DAC B (see Typical Applications). The DAC output current from IOUT1B flows through the feedback resistor to the RFBB pin. The impedance looking into this pin is 10k to ground.

**IOUT1B (Pin 45):** DAC B Current Output. This pin is a virtual ground when the DAC is operating and should reside at 0V. For normal operation tie to the negative input of the I/V converter amplifier for DAC B (see Typical Applications).

**VOSADJB (Pin 46):** DAC B Offset Adjust Pin. This control pin can be used to null unipolar offset or bipolar zero error. The offset-voltage delta is inverted and attenuated such that a 5V control voltage applied to VOSADJB produces ΔVOS = –512 LSB (LTC2754-16) in any output range (assumes a 5V reference voltage at RINB). Tie to ground if not used.

**VOSADJA (Pin 47):** DAC A Offset Adjust Pin. This control pin can be used to null unipolar offset or bipolar zero error. The offset-voltage delta is inverted and attenuated such that a 5V control voltage applied to VOSADJA produces ΔVOS = –512 LSB (LTC2754-16) in any output range (assumes a 5V reference voltage at RINA). Tie to ground if not used.

**RFBA (Pin 49):** DAC A Feedback Resistor. For normal operation tie to the output of the I/V converter amplifier for DAC A (see Typical Applications). The DAC output current from IOUT1A flows through the feedback resistor to the RFBA pin. The impedance looking into this pin is 10k to ground.
**PIN FUNCTIONS**

**ROFSA (Pin 50):** Bipolar Offset Network for DAC A. This pin provides the translation of the output voltage range for bipolar spans. Accepts up to ±15V; for normal operation tie to the positive reference voltage at RINA (Pin 2). The impedance looking into this pin is 20k to ground.

**REFA (Pin 51):** Inverted Reference Voltage for DAC A, with internal connection to the reference inverting resistor. The 20k resistor is connected internally from REFA to RCOMA. For normal operation tie this pin to the output of reference inverting amplifier (see Typical Applications). Typically –5V; accepts up to ±15V. The impedance looking into this pin is 10k to ground (RINA and RCOMA floating).

**RCOMA (Pin 52):** Center Tap Point for Reference Amplifier Inverting Resistors. The 20k reference inverting resistors are connected internally from RINA to RCOMA and from RCOMA to REFA, respectively (see Block Diagram). For normal operation tie RCOMA to the negative input of external reference inverting amplifier (see Typical Applications).

**Exposed Pad (Pin 53):** Ground. The Exposed Pad must be soldered to the PCB.

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**BLOCK DIAGRAM**

![Block Diagram of LTC2754](image-url)
Output Ranges

The LTC2754 is a quad, current-output, serial-input precision multiplying DAC with selectable output ranges. Ranges can either be programmed in software for maximum flexibility—each of the four DACs can be programmed to any one of six output ranges—or hardwired through pin-strapping. Two unipolar ranges are available (0V to 5V and 0V to 10V), and four bipolar ranges (±2.5V, ±5V, ±10V and –2.5V to 7.5V). These ranges are obtained when an external precision 5V reference is used. When a reference voltage of 2V is used, the ranges become: 0V to 2V, 0V to 4V, ±1V, ±2V, ±4V and –1V to 3V. The output ranges are linearly scaled for other reference voltages.

Manual Span Configuration

Multiple output ranges are not needed in some applications. To configure the LTC2754 to operate in a single span without additional operational overhead, tie the M-SPAN pin directly to V<sub>DD</sub>. The active output range for all four DACs is then set via hardware pin strapping of pins S2, S1 and S0 (rather than through the SPI port); and Write and Update commands have no effect on the active output span. See Figure 1 and Table 3.

Tie the M-SPAN pin to ground for normal SoftSpan operation.
**OPERATION**

**Input and DAC Registers**

The LTC2754 has 5 internal registers for each DAC, a total of 20 registers (see Block Diagram). Each DAC channel has two sets of double-buffered registers—one set for the code data, and one for the output range of the DAC—plus one readback register. Double buffering provides the capability to simultaneously update the span (output range) and code, which allows smooth voltage transitions when changing output ranges. It also permits the simultaneous updating of multiple DACs.

Each set of double-buffered registers comprises an Input register and a DAC register.

Input register: The Write operation shifts data from the SDI pin into a chosen Input register. The Input registers are holding buffers; Write operations do not affect the DAC outputs.

DAC register: The Update operation copies the contents of an Input register to its associated DAC register. The contents of a DAC register directly updates the associated DAC output voltage or output range.

Note that updates always include both Data and Span registers; but the values held in the DAC registers will only change if the associated Input register values have previously been changed via a Write operation.

**Serial Interface**

When the CS/LD pin is taken low, the data on the SDI pin is loaded into the shift register on the rising edge of the clock (SCK pin). The minimum (24-bit wide) loading sequence required for the LTC2754 is a 4-bit command word (C3 C2 C1 C0), followed by a 4-bit address word (A3 A2 A1 A0) and 16 data (span or code) bits, MSB first. Figure 2 shows the SDI input word syntax to use when writing code or span. If a 32-bit input sequence is used, the first eight bits must be zeros, followed by the same sequence as for a 24-bit wide input. Figure 3 shows the loading and readback sequences.

In the data field (D15-D0) of any non-read instruction cycle, SRO shifts out the contents of the buffer that was specified in the preceding command. This “rolling readback” default mode of operation can dramatically reduce the number of instruction cycles needed, since any command can be verified during succeeding commands with no additional overhead. See Figure 4. Table 1 shows the storage location (‘readback pointer’) of the data which will be output from SRO during the next instruction.

For Read commands, the data is shifted out during the Read instruction itself (on the 16 falling SCK edges immediately after the last address bit is shifted in on SDI). When checking the span of a DAC using SRO, the span bits are the last four bits shifted out, corresponding to their sequence and positions when writing a span. See Figure 3.
### Table 1. Command Codes

<table>
<thead>
<tr>
<th>CODE</th>
<th>COMMAND</th>
<th>READBACK POINTER—CURRENT INPUT WORD W₀</th>
<th>READBACK POINTER—NEXT INPUT WORD W₁,₁</th>
</tr>
</thead>
<tbody>
<tr>
<td>C₀ C₁ C₂ C₃</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 0 1 0</td>
<td>Write Span DAC n</td>
<td>Set by Previous Command</td>
<td>Input Span Register DAC n</td>
</tr>
<tr>
<td>0 0 1 1</td>
<td>Write Code DAC n</td>
<td>Set by Previous Command</td>
<td>Input Code Register DAC n</td>
</tr>
<tr>
<td>0 1 0 0</td>
<td>Update DAC n</td>
<td>Set by Previous Command</td>
<td>DAC Span Register DAC n</td>
</tr>
<tr>
<td>0 1 0 1</td>
<td>Update All DACs</td>
<td>Set by Previous Command</td>
<td>DAC Code Register DAC A</td>
</tr>
<tr>
<td>0 1 1 0</td>
<td>Write Span DAC n Update DAC n</td>
<td>Set by Previous Command</td>
<td>DAC Span Register DAC n</td>
</tr>
<tr>
<td>0 1 1 1</td>
<td>Write Code DAC n Update DAC n</td>
<td>Set by Previous Command</td>
<td>DAC Code Register DAC n</td>
</tr>
<tr>
<td>1 0 0 0</td>
<td>Write Span DAC n Update All DACs</td>
<td>Set by Previous Command</td>
<td>DAC Span Register DAC n</td>
</tr>
<tr>
<td>1 0 0 1</td>
<td>Write Code DAC n Update All DACs</td>
<td>Set by Previous Command</td>
<td>DAC Code Register DAC n</td>
</tr>
<tr>
<td>1 0 1 0</td>
<td>Read Input Span Register DAC n</td>
<td>Input Span Register DAC n</td>
<td></td>
</tr>
<tr>
<td>1 0 1 1</td>
<td>Read Input Code Register DAC n</td>
<td>Input Code Register DAC n</td>
<td></td>
</tr>
<tr>
<td>1 1 0 0</td>
<td>Read DAC Span Register DAC n</td>
<td>DAC Span Register DAC n</td>
<td></td>
</tr>
<tr>
<td>1 1 0 1</td>
<td>Read DAC Code Register DAC n</td>
<td>DAC Code Register DAC n</td>
<td></td>
</tr>
<tr>
<td>1 1 1 1</td>
<td>No Operation</td>
<td>Set by Previous Command</td>
<td>DAC Code Register DAC n</td>
</tr>
<tr>
<td>–</td>
<td>–</td>
<td>–</td>
<td>DAC Span Register DAC A</td>
</tr>
<tr>
<td>–</td>
<td>Initial Power-Up or Power Interrupt</td>
<td>–</td>
<td>DAC Span Register DAC A</td>
</tr>
</tbody>
</table>

Codes not shown are reserved—do not use.

### Table 2. Address Codes

<table>
<thead>
<tr>
<th>A₀ A₁ A₂ A₃</th>
<th>n</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 0 ×</td>
<td>DAC A</td>
<td></td>
</tr>
<tr>
<td>0 0 1 ×</td>
<td>DAC B</td>
<td></td>
</tr>
<tr>
<td>0 1 0 ×</td>
<td>DAC C</td>
<td></td>
</tr>
<tr>
<td>0 1 1 ×</td>
<td>DAC D</td>
<td></td>
</tr>
<tr>
<td>1 1 1 ×</td>
<td>All DACs (Note 1)</td>
<td></td>
</tr>
</tbody>
</table>

Codes not shown are reserved—do not use. × = Don’t Care.

**Note 1.** If readback is taken using the All DACs address, the LTC2754 defaults to DAC A.

### Table 3. Span Codes

<table>
<thead>
<tr>
<th>S₀ S₁ S₂ S₃</th>
<th>SPAN</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>× 0 0 0</td>
<td>Unipolar 0V to 5V</td>
<td></td>
</tr>
<tr>
<td>× 0 0 1</td>
<td>Unipolar 0V to 10V</td>
<td></td>
</tr>
<tr>
<td>× 0 1 0</td>
<td>Bipolar −5V to 5V</td>
<td></td>
</tr>
<tr>
<td>× 0 1 1</td>
<td>Bipolar −10V to 10V</td>
<td></td>
</tr>
<tr>
<td>× 1 0 0</td>
<td>Bipolar −2.5V to 2.5V</td>
<td></td>
</tr>
<tr>
<td>× 1 0 1</td>
<td>Bipolar −2.5V to 7.5V</td>
<td></td>
</tr>
</tbody>
</table>

Codes not shown are reserved—do not use. × = Don’t Care.
OPERATION

Readback in M-Span Configuration

If the part is in M-Span configuration and a DAC Span register is specified for readback, then the data shifted out of SRO will reflect the actual active span. The hardware-configured output range is therefore software detectable and available for use in programming.

Examples

1. Using a 24-bit instruction, load DAC A with the unipolar range of 0V to 10V, output at zero volts and all other DACs with the bipolar range of ±10V, outputs at zero volts. Note all DAC outputs should change at the same time.

   a) \(\overline{CS}/LD\downarrow\)
      Clock SDI = 0010 1111 0000 0000 0000 0011
   b) \(\overline{CS}/LD\uparrow\)
      Input register- Range of all DACs set to bipolar ±10V.
   c) \(\overline{CS}/LD\downarrow\)
      Clock SDI = 0010 0000 0000 0000 0000 0001
   d) \(\overline{CS}/LD\uparrow\)
      Input register- Range of DAC A set to unipolar 0V to 10V.
   e) \(\overline{CS}/LD\downarrow\)
      Clock SDI = 0011 1111 1000 0000 0000 0000
   f) \(\overline{CS}/LD\uparrow\)
      Input register- Code of all DACs set to midscale.
   g) \(\overline{CS}/LD\downarrow\)
      Clock SDI = 0011 0000 0000 0000 0000 0000
   h) \(\overline{CS}/LD\uparrow\)
      Input register- Code of DAC A set to zero code.
   i) \(\overline{CS}/LD\downarrow\)
      Clock SDI = 0100 1111 XXXX XXXX XXXX XXXX
   j) \(\overline{CS}/LD\uparrow\)
      Update all DACs for both Code and Range.
   k) Alternatively steps i and j could be replaced with LDAC "\(\uparrow\)".

2. Using a 32-bit load sequence, load DAC C with bipolar ±2.5V and its output at zero volts. Use readback to check Input register contents before updating the DAC output (i.e., before copying Input register contents into DAC register).

   a) \(\overline{CS}/LD\downarrow\) (Note that after power-on, the code in Input register is zero)
      Clock SDI = 0000 0000 0011 0100 1000 0000 0000 0000
   b) \(\overline{CS}/LD\uparrow\)
      Input register- Code of DAC C set to midscale setting.
   c) \(\overline{CS}/LD\downarrow\)
      Clock SDI = 0000 0000 0010 0100 0000 0000 0000 0100
      Data out on SRO = 1000 0000 0000 0000 Verifies that Input register- Code DAC C is at midscale setting.
   d) \(\overline{CS}/LD\uparrow\)
      Input register- Range of DAC C set to Bipolar ±2.5V range.
   e) \(\overline{CS}/LD\downarrow\)
      Clock SDI = 0000 0000 1010 0100 xxxx xxxx xxxx xxxx
      Data Out on SRO = 0000 0000 0000 0100 Verifies that Input register- range of DAC C set to Bipolar ±2.5V Range.
   f) \(\overline{CS}/LD\uparrow\)
   g) \(\overline{CS}/LD\downarrow\)
      Clock SDI = 0000 0000 0100 0100 xxxx xxxx xxxx xxxx
      Update DAC C for both Code and Range.
   h) Alternatively steps f and g could be replaced with LDAC "\(\uparrow\)".
OPERATION

System Offset and Reference Adjustments

The LTC2754 has individual offset- and gain- adjust pins (VOSADJX and GEADJX, respectively) for each of its four DACs.

Many systems require compensation for overall system offset. This may be an order of magnitude or more greater than the offset of the LTC2754, which is so low as to be dominated by external output amplifier errors even when using the most precise op amps.

The offset adjust pins VOSADJX can be used to null unipolar offset or bipolar zero error. The offset-voltage delta is inverted and attenuated such that a 5V control voltage applied to VOSADJX produces ∆VOS = −512 LSB (LTC2754-16) in any output range (assumes a 5V reference voltage at RINX).

In voltage terms, the offset delta is attenuated by a factor of 32, 64 or 128, depending on the output range. (These functions hold regardless of reference voltage.)

\[
\Delta V_{OS} = -(1/128)V_{OSADJX} \quad [0V \text{ to } 5V, \pm 2.5V \text{ spans}]
\]

\[
\Delta V_{OS} = -(1/64)V_{OSADJX} \quad [0V \text{ to } 10V, \pm 5V, -2.5V \text{ to } 7.5V \text{ spans}]
\]

\[
\Delta V_{OS} = -(1/32)V_{OSADJX} \quad [\pm 10V \text{ span}]
\]

The gain error adjust pins GEADJX can be used to null gain error or to compensate for reference errors. Nominal adjustment range is ±512 LSB (LTC2754-16) for a voltage input range of ±VRINX (i.e., ±5V for a 5V reference input). The gain-error delta is non-inverting for positive reference voltages.

Note that these pins compensate the gain by altering the inverted reference voltage VREFX. In voltage terms, the VREFX delta is inverted and attenuated by a factor of 128.

\[
\Delta V_{REFX} = -(1/128)GE_{ADJX}
\]

The nominal input range of these pins is ±5V; other voltages of up to ±15V may be used if needed. However, do not use voltages divided down from power supplies; reference-quality, low-noise inputs are required to maintain the performance of which the part is capable.

The VOSADJX pins have an input impedance of 1.28MΩ. These pins should be driven with a Thevenin-equivalent impedance of 10k or less to preserve the settling performance of the LTC2754. They should be shorted to GND if not used.

The GEADJX pins have an input impedance of 2.56MΩ, and are intended for use with fixed reference voltages only. They should be shorted to GND if not used. If the reference inverting resistors are not used for that channel, then GEADJX, RCOMX and RINX should all be shorted to REFX.

Power-On Reset and Clear

When power is first applied to the LTC2754, all DACs power-up in unipolar 5V mode (S3S2S1S0 = 0000). All internal DAC registers are reset to 0 and the DAC outputs initialize to zero volts.

If the part is configured for manual span operation, all four DACs will be set into the pin-strapped range at the first Update command. This allows the user to simultaneously update span and code for a smooth voltage transition into the chosen output range.

When the CLR pin is taken low, a system clear results. The DAC buffers are reset to 0 and the DAC outputs are all reset to zero volts. The Input buffers are left intact, so that any subsequent Update command (including the use of LDAC) restores the addressed DACs to their respective previous states.

If CLR is asserted during an instruction, i.e., when CS/LD is low, the instruction is aborted. Integrity of the relevant Input buffers is not guaranteed under these conditions, therefore the contents should be checked using readback or replaced.

The RFLAG pin is used as a flag to notify the system of a loss of data integrity. The RFLAG output is asserted low at power-up, system clear, or if the supply VDD dips below approximately 2V; and stays asserted until any valid Update command is executed.
OPERATION

Figure 2. Serial Input Write Sequence
Figure 3a. 24-Bit Instruction Sequence

Figure 3b. 32-Bit Instruction Sequence
Figure 4. Rolling Readback
Op Amp Selection

Because of the extremely high accuracy of the 16-bit LTC2754-16, careful thought should be given to op amp selection in order to achieve the exceptional performance of which the part is capable. Fortunately, the sensitivity of INL and DNL to op amp offset has been greatly reduced compared to previous generations of multiplying DACs.

Tables 4 and 5 contain equations for evaluating the effects of op amp parameters on the LTC2754’s accuracy when programmed in a unipolar or bipolar output range. These are the changes the op amp can cause to the INL, DNL, unipolar offset, unipolar gain error, bipolar zero and bipolar gain error. Tables 4 and 5 can also be used to determine the effects of op amp parameters on the LTC2754-12. However, the results obtained from Tables 4 and 5 are in 16-bit LSBs. Divide these results by 16 to obtain the correct LSB sizing.

Table 6 contains a partial list of LTC precision op amps recommended for use with the LTC2754. The easy-to-use design equations simplify the selection of op amps to meet

### Table 4. Coefficients for the Equations in Table 5

<table>
<thead>
<tr>
<th>OUTPUT RANGE</th>
<th>A1</th>
<th>A2</th>
<th>A3</th>
<th>A4</th>
<th>A5</th>
</tr>
</thead>
<tbody>
<tr>
<td>5V</td>
<td>1.1</td>
<td>2</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>±10V</td>
<td>2.2</td>
<td>3</td>
<td>0.5</td>
<td>1</td>
<td>1.5</td>
</tr>
<tr>
<td>±5V</td>
<td>2</td>
<td>2</td>
<td>1</td>
<td>1</td>
<td>1.5</td>
</tr>
<tr>
<td>±10V</td>
<td>4</td>
<td>4</td>
<td>0.83</td>
<td>1</td>
<td>2.5</td>
</tr>
<tr>
<td>±2.5V</td>
<td>1</td>
<td>1</td>
<td>1.4</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>–2.5V to 7.5V</td>
<td>1.9</td>
<td>3</td>
<td>0.7</td>
<td>0.5</td>
<td>1.5</td>
</tr>
</tbody>
</table>

### Table 5. Easy-to-Use Equations Determine Op Amp Effects on DAC Accuracy in All Output Ranges (Circuit of Page 1). Subscript 1 Refers to Output Amp, Subscript 2 Refers to Reference Inverting Amp.

<table>
<thead>
<tr>
<th>OP AMP</th>
<th>INL (LSB)</th>
<th>DNL (LSB)</th>
<th>UNIPOLAR OFFSET (LSB)</th>
<th>BIPOLAR ZERO ERROR (LSB)</th>
<th>UNIPOLAR GAIN ERROR (LSB)</th>
<th>BIPOLAR GAIN ERROR (LSB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>VOS1 (mV)</td>
<td>VOS1 • 3.2 • 5V</td>
<td>VOS1 • 0.82 • 5V</td>
<td>A3 • VOS1 + 13.2 • 5V</td>
<td>A3 • VOS1 + 19.8 • 5V</td>
<td>VOS1 • 13.2 • 5V</td>
<td>VOS1 • 13.2 • 5V</td>
</tr>
<tr>
<td>I81 (nA)</td>
<td>I81 • 0.0003 • 5V</td>
<td>I81 • 0.00008 • 5V</td>
<td>I81 • 0.13 • 5V</td>
<td>I81 • 0.13 • 5V</td>
<td>I81 • 0.0018 • 5V</td>
<td>I81 • 0.0018 • 5V</td>
</tr>
<tr>
<td>AVOL1 (V/V)</td>
<td>A1 • 16.5k AVOL1</td>
<td>A2 • 1.5k AVOL1</td>
<td>0</td>
<td>0</td>
<td>A5 • 131k AVOL1</td>
<td>A5 • 131k AVOL1</td>
</tr>
<tr>
<td>VOS2 (mV)</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>A4 • VOS2 • 13.1 • 5V</td>
<td>VOS2 • 26.2 • 5V</td>
<td>VOS2 • 26.2 • 5V</td>
</tr>
<tr>
<td>I82 (mV)</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>A4 • I82 • 0.13 • 5V</td>
<td>I82 • 0.26 • 5V</td>
<td>I82 • 0.26 • 5V</td>
</tr>
<tr>
<td>AVOL2 (V/V)</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>A4 • 66k AVOL2</td>
<td>131k AVOL2</td>
<td>131k AVOL2</td>
</tr>
</tbody>
</table>

### Table 6. Partial List of LTC Precision Amplifiers Recommended for Use with the LTC2754 with Relevant Specifications

<table>
<thead>
<tr>
<th>AMPLIFIER</th>
<th>VOS</th>
<th>I8</th>
<th>AVOL</th>
<th>VOLTAGE NOISE</th>
<th>CURRENT NOISE</th>
<th>SLEW RATE</th>
<th>GAIN BANDWIDTH</th>
<th>SETTLING TIME</th>
<th>POWER DISSIPATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>LT1001</td>
<td>25</td>
<td>2</td>
<td>800</td>
<td>10</td>
<td>0.12</td>
<td>0.25</td>
<td>0.8</td>
<td>120</td>
<td>46</td>
</tr>
<tr>
<td>LT1097</td>
<td>50</td>
<td>0.35</td>
<td>1000</td>
<td>14</td>
<td>0.008</td>
<td>0.2</td>
<td>0.7</td>
<td>120</td>
<td>11</td>
</tr>
<tr>
<td>LT1112 (Dual)</td>
<td>60</td>
<td>0.25</td>
<td>1500</td>
<td>14</td>
<td>0.008</td>
<td>0.16</td>
<td>0.75</td>
<td>115</td>
<td>10.5/Op Amp</td>
</tr>
<tr>
<td>LT1124 (Dual)</td>
<td>70</td>
<td>20</td>
<td>4000</td>
<td>2.7</td>
<td>0.3</td>
<td>4.5</td>
<td>12.5</td>
<td>19</td>
<td>69/Op Amp</td>
</tr>
<tr>
<td>LT1468</td>
<td>75</td>
<td>10</td>
<td>5000</td>
<td>5</td>
<td>0.6</td>
<td>22</td>
<td>90</td>
<td>2</td>
<td>117</td>
</tr>
<tr>
<td>LT1469 (Dual)</td>
<td>125</td>
<td>10</td>
<td>2000</td>
<td>5</td>
<td>0.6</td>
<td>22</td>
<td>90</td>
<td>2</td>
<td>123/Op Amp</td>
</tr>
</tbody>
</table>
APPLICATIONS INFORMATION

the system's specified error budget. Select the amplifier from Table 6 and insert the specified op amp parameters in Table 5. Add up all the errors for each category to determine the effect the op amp has on the accuracy of the part. Arithmetic summation gives an (unlikely) worst-case effect. A root-sum-square (RMS) summation produces a more realistic estimate.

Op amp offset will contribute mostly to output offset and gain error, and has minimal effect on INL and DNL. For example, for the LTC2754-16 with a 5V reference in 5V unipolar mode, a 250μV op amp offset will cause a 3.3LSB zero-scale error and a 3.3LSB gain error; but only 0.8LSB of INL degradation and 0.2LSB of DNL degradation.

While not directly addressed by the simple equations in Tables 4 and 5, temperature effects can be handled just as easily for unipolar and bipolar applications. First, consult an op amp's data sheet to find the worst-case $V_{\text{OS}}$ and $I_B$ over temperature. Then, plug these numbers into the $V_{\text{OS}}$ and $I_B$ equations from Table 5 and calculate the temperature-induced effects.

For applications where fast settling time is important, Application Note 74, “Component and Measurement Advances Ensure 16-Bit DAC Settling Time,” offers a thorough discussion of 16-bit DAC settling time and op amp selection.

Precision Voltage Reference Considerations

Much in the same way selecting an operational amplifier for use with the LTC2754 is critical to the performance of the system, selecting a precision voltage reference also requires due diligence. The output voltage of the LTC2754 is directly affected by the voltage reference; thus, any voltage reference error will appear as a DAC output voltage error.

There are three primary error sources to consider when selecting a precision voltage reference for 16-bit applications: output voltage initial tolerance, output voltage temperature coefficient and output voltage noise.

Initial reference output voltage tolerance, if uncorrected, generates a full-scale error term. Choosing a reference with low output voltage initial tolerance, like the LT1236 (±0.05%), minimizes the gain error caused by the reference; however, a calibration sequence that corrects for system zero- and full-scale error is always recommended.

A reference's output voltage temperature coefficient affects not only the full-scale error, but can also affect the circuit's apparent INL and DNL performance. If a reference is chosen with a loose output voltage temperature coefficient, then the DAC output voltage along its transfer characteristic will be very dependent on ambient conditions. Minimizing the error due to reference temperature coefficient can be achieved by choosing a precision reference with a low output voltage temperature coefficient and/or tightly controlling the ambient temperature of the circuit to minimize temperature gradients.

Table 7. Partial List of LTC Precision References Recommended for Use with the LTC2754 with Relevant Specifications

<table>
<thead>
<tr>
<th>REFERENCE</th>
<th>INITIAL TOLERANCE</th>
<th>TEMPERATURE DRIFT</th>
<th>0.1Hz to 10Hz NOISE</th>
</tr>
</thead>
<tbody>
<tr>
<td>LT1019A-5, LT1019A-10</td>
<td>±0.05%</td>
<td>5ppm/°C</td>
<td>12μV_pP</td>
</tr>
<tr>
<td>LT1236A-5, LT1236A-10</td>
<td>±0.05%</td>
<td>5ppm/°C</td>
<td>3μV_pP</td>
</tr>
<tr>
<td>LT1460A-5, LT1460A-10</td>
<td>±0.075%</td>
<td>10ppm/°C</td>
<td>20μV_pP</td>
</tr>
<tr>
<td>LT1790A-2.5</td>
<td>±0.05%</td>
<td>10ppm/°C</td>
<td>12μV_pP</td>
</tr>
<tr>
<td>LTC6652A-2.048</td>
<td>±0.05%</td>
<td>5ppm/°C</td>
<td>2.1ppm_pP</td>
</tr>
<tr>
<td>LTC6652A-2.5</td>
<td></td>
<td></td>
<td>2.1ppm_pP</td>
</tr>
<tr>
<td>LTC6652A-3</td>
<td></td>
<td></td>
<td>2.1ppm_pP</td>
</tr>
<tr>
<td>LTC6652A-3.3</td>
<td></td>
<td></td>
<td>2.2ppm_pP</td>
</tr>
<tr>
<td>LTC6652A-4.096</td>
<td></td>
<td></td>
<td>2.3ppm_pP</td>
</tr>
<tr>
<td>LTC6652A-5</td>
<td></td>
<td></td>
<td>2.8ppm_pP</td>
</tr>
</tbody>
</table>
APPLICATIONS INFORMATION

As precision DAC applications move to 16-bit and higher performance, reference output voltage noise may contribute a dominant share of the system's noise floor. This in turn can degrade system dynamic range and signal-to-noise ratio. Care should be exercised in selecting a voltage reference with as low an output noise voltage as practical for the system resolution desired. Precision voltage references, like the LT1236, produce low output noise in the 0.1Hz to 10Hz region, well below the 16-bit LSB level in 5V or 10V full-scale systems. However, as the circuit bandwidths increase, filtering the output of the reference may be required to minimize output noise.

Grounding

As with any high resolution converter, clean grounding is important. A low impedance analog ground plane and star grounding techniques should be used. IOUT2 must be tied to the star ground with as low a resistance as possible. When it is not possible to locate star ground close to IOUT2, a low resistance trace should be used to route this pin to star ground. This minimizes the voltage drop from this pin to ground caused by the code-dependent current flowing to ground. When the resistance of this circuit board trace becomes greater than 1Ω, a force/sense amplifier configuration should be used to drive this pin (see Figure 5). This preserves the excellent accuracy (1LSB INL and DNL) of the LTC2754-16.

Layout

Figures 6, 7, 8, and 9 show the layout for the LTC2754 evaluation board, DC1546. This shows how to route the digital signals around the device without interfering with the reference and output op amps. Complete demo board documentation is available in the DC1546 “Quick Start Guide.”
Figure 5. Optional Circuits for Driving IOUT2 from GND with a Force/Sense Amplifier.
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Figure 6. LTC2754 Evaluation Board DC1546. Layer 1, Top Layer (Component Side)

Figure 7. LTC2754 Evaluation Board DC1546. Layer 2, GND Plane
APPLICATIONS INFORMATION

Figure 8. LTC2754 Evaluation Board DC1546. Layer 3, Power Traces

Figure 9. LTC2754 Evaluation Board DC1546. Layer 4, Bottom Layer (Solder Side)
Digitally Controlled Offset and Gain Trim Circuit. Powering VDD from LT1236 Ensures Quiet Supply
Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.
## RELATED PARTS

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>LT1027</td>
<td>Precision Reference</td>
<td>1ppm/°C Maximum Drift</td>
</tr>
<tr>
<td>LT1236A-5</td>
<td>Precision Reference</td>
<td>0.05% Maximum Tolerance, 1ppm 0.1Hz to 10Hz Noise</td>
</tr>
<tr>
<td>LT1468</td>
<td>16-Bit Accurate Op-Amp</td>
<td>90MHz GBW, 22V/μs Slew Rate</td>
</tr>
<tr>
<td>LT1469</td>
<td>Dual 16-Bit Accurate Op-Amp</td>
<td>90MHz GBW, 22V/μs Slew Rate</td>
</tr>
<tr>
<td>LTC1588/LTC1589/ LTC1592</td>
<td>Serial 12-/14-/16-Bit IOUT Single DAC</td>
<td>Software-Selectable (SoftSpan) Ranges, ±1LSB INL, DNL, 16-Lead SSOP Package</td>
</tr>
<tr>
<td>LTC1591/LTC1597</td>
<td>Parallel 14-/16-Bit IOUT Single DAC</td>
<td>Integrated 4-Quadrant Resistors</td>
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<td>Serial 12-/14-/16-Bit VOUT Quad DACs</td>
<td>Software-Selective (SoftSpan) Ranges, Integrated Amplifiers, ±1LSB INL</td>
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<td>±1LSB INL, DNL, Software-Selectable (SoftSpan) Ranges, 5mm × 7mm QFN-38 Package</td>
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<td>±1LSB INL, DNL, Software-Selectable (SoftSpan) Ranges, 9mm × 9mm QFN-64 Package</td>
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