DS26528
T1/E1/J1 Octal Transceiver

REVISION A3 ERRATA

The errata listed below describe situations where DS26528 revision A3 components perform differently than expected or differently than described in the data sheet. Dallas Semiconductor intends to correct these errata in subsequent die revisions.

This errata sheet only applies to DS26528 revision A3 components. Revision A3 components are branded on the topside of the package with a six-digit code in the form yywwA3, where yy and ww are two-digit numbers representing the year and workweek of manufacture, respectively. To obtain an errata sheet on another DS26528 die revision, visit our website at www.maxim-ic.com/errata.

1. FAILURE TO DETECT J1 LFA (YELLOW ALARM) IN ESF MODE

Description:
The DS26528 does not identify the J1 LFA (also called Yellow or RAI) alarms correctly. In J1 ESF mode, the DS26528 will not report the LFA alarm when the Japanese JT-G704 LFA pattern of '11111111 11111111' is present in the facilities data link. The DS26528 will only respond to the normal G.704 LFA pattern of '11111111 00000000.'

Work Around:
To transmit the Japanese ESF LFA alarm, which is 0xFFFF in the FDL, the following can be done. Set the TFDL register to 0xFF and set the TFDLS bit to a 0. The TFDLS bit is located in the TCR2 register.

To receive the Japanese ESF LFA alarm, which is 0xFFFF, the software must monitor the RFDL register. The RFDL register is updated regularly and the RFDLF status bit indicates an update. The RFDLF status bit is located in the SR8 register. Since the Japanese ESF LFA alarm pattern is 2 bytes long, the RFDL register must be read on two consecutive updates for a complete pattern. When 16 consecutive patterns of 0xFFFF appear in the FDL, the alarm is set. If 14 or fewer patterns of 0xFFFF out of 16 possible appear in the FDL, the alarm is cleared.

2. PROGRAMMABLE CHANNEL BLANKING MAY LEAD TO DROPPED DATA UNDER CERTAIN IBO OPERATING MODES

Description:
When the part is programmed for channel blanking with channel 1 and channel 2 blanked at the same time, data can be dropped if T1 rate data is being mapped onto an E1 rate backplane in byte-interleaved IBO mode.

Work Around:
None.

3. ERROR COUNT REGISTERS COULD ROLL OVER AT 0xFFFFh IN MANUAL UPDATE MODE

Description:
The error count registers can roll over after the counters have saturated in manual update mode (ERCNT.MCUS = 0). This rollover will not occur when the error count registers are not set to be updated manually; they will saturate as stated in the data sheet.

Work Around:
Ensure that the manual error counter update bit is set (ERCNT.MECU = 1) before the registers are allowed to saturate.

4. WHEN PROCESSING AN SLC-96 MESS5 MESSAGE, THE INFORMATION REPORTED MAY BECOME CORRUPT

Description:
When a SLC-96 MESS5 message is received and the first six bits of the message are ‘000111,’ the information reported can become corrupt. A normal SLC-96 datastream format is '000111000111ccccccccccc010mmmaassss1.' If the “c” bits at the start of the message are ‘000111,’ the SLC-96 message will not be reported correctly because the synchronizer will resync to those six bits. A MESS5 message starts with ‘000111’ per BellCore TR-TSY-000008 and Telcordia GR-8.

Work Around:
None.

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