LTC2484

24-Bit ΔΣ ADC with Easy Drive Input Current Cancellation

FEATURES

- Easy Drive Technology Enables Rail-to-Rail Inputs with Zero Differential Input Current
- Directly Digitizes High Impedance Sensors with Full Accuracy
- 600nV RMS Noise
- GND to VCC Input/Reference Common Mode Range
- Programmable 50Hz, 60Hz or Simultaneous 50Hz/60Hz Rejection Mode
- 2ppm INL, No Missing Codes
- 1ppm Offset and 15ppm Total Unadjusted Error
- Selectable 2× Speed Mode (15Hz Using Internal Oscillator)
- No Latency: Digital Filter Settles in a Single Cycle
- Single Supply 2.7V to 5.5V Operation
- Internal Oscillator
- Available in a Tiny (3mm × 3mm) 10-Lead DFN Package

APPLICATIONS

- Direct Sensor Digitizer
- Weight Scales
- Direct Temperature Measurement
- Strain Gauge Transducers
- Instrumentation
- Industrial Process Control
- DVMs and Meters

DESCRIPTION

The LTC®2484 combines a 24-bit No Latency ΔΣ™ analog-to-digital converter with patented Easy Drive™ technology. The patented sampling scheme eliminates dynamic input current errors and the shortcomings of on-chip buffering through automatic cancellation of differential input current. This allows large external source impedances and input signals with rail-to-rail input range to be directly digitized while maintaining exceptional DC accuracy.

The LTC2484 includes an on-chip oscillator. The LTC2484 can be configured to reject line frequencies. 50Hz, 60Hz or simultaneous 50Hz/60Hz line frequency rejection can be selected as well as a 2× speed-up mode.

The LTC2484 allows a wide common mode input range (0V to VCC) independent of the reference voltage. The reference can be as low as 100mV or can be tied directly to VCC. The LTC2484 includes an on-chip trimmed oscillator, eliminating the need for external crystals or oscillators. Absolute accuracy and low drift are automatically maintained through continuous, transparent, offset and full-scale calibration.

LT, LTC and LTM, Linear Technology and the Linear logo are registered trademarks and No Latency ΔΣ and Easy Drive are trademarks of Linear Technology Corporation. All other trademarks are the property of their respective owners. Patents pending.

+FS Error vs RSOURCE at IN+ and IN−

For more information www.linear.com/LTC2484
ABSOLUTE MAXIMUM RATINGS
(Note 1)
Supply Voltage \((V_{CC})\) to GND ................. –0.3V to 6V
Analog Input Voltage to GND .......... –0.3V to \((V_{CC} + 0.3V)\)
Reference Input Voltage to GND .. –0.3V to \((V_{CC} + 0.3V)\)
Digital Input Voltage to GND ....... –0.3V to \((V_{CC} + 0.3V)\)
Digital Output Voltage to GND...... –0.3V to \((V_{CC} + 0.3V)\)
Operating Temperature Range
LTC2484C .......................................... 0°C to 70°C
LTC2484I ...........................................–40°C to 85°C
Storage Temperature Range ........... –65°C to 125°C

ORDER INFORMATION

LEAD FREE FINISH | TAPE AND REEL | PART MARKING* | PACKAGE DESCRIPTION | TEMPERATURE RANGE
--- | --- | --- | --- | ---
LTC2484CDD#PBF | LTC2484CDD#TRPB | LBSS | 10-Lead (3mm × 3mm) Plastic DFN | 0°C to 70°C
LTC2484IDD#PBF | LTC2484IDD#TRPB | LBSS | 10-Lead (3mm × 3mm) Plastic DFN | –40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. * The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS (NORMAL SPEED) The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at \(T_{A} = 25°C\). (Notes 3, 4)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution (No Missing Codes)</td>
<td>(0.1 \leq V_{\text{REF}} \leq V_{CC}, -FS \leq V_{IN} \leq +FS) (Note 5)</td>
<td>●</td>
<td>24</td>
<td></td>
<td>Bits</td>
</tr>
<tr>
<td>Integral Nonlinearity</td>
<td>(5V \leq V_{CC} \leq 5.5V, V_{\text{REF}} = 5V, V_{\text{IN(CM)}} = 2.5V) (Note 6) (2.7V \leq V_{CC} \leq 5.5V, V_{\text{REF}} = 2.5V, V_{\text{IN(CM)}} = 1.25V) (Note 6)</td>
<td>●</td>
<td>2</td>
<td>10</td>
<td>ppm of (V_{\text{REF}}) ppm of (V_{\text{REF}})</td>
</tr>
<tr>
<td>Offset Error</td>
<td>(2.5V \leq V_{\text{REF}} \leq V_{CC}, GND \leq IN^+ = IN^- \leq V_{CC}) (Note 14)</td>
<td>●</td>
<td>0.5</td>
<td>2.5</td>
<td>µV</td>
</tr>
<tr>
<td>Offset Error Drift</td>
<td>(2.5V \leq V_{\text{REF}} \leq V_{CC}, GND \leq IN^+ = IN^- \leq V_{CC})</td>
<td></td>
<td>10</td>
<td></td>
<td>nV/°C</td>
</tr>
<tr>
<td>Positive Full-Scale Error</td>
<td>(2.5V \leq V_{\text{REF}} \leq V_{CC}, IN^+ = 0.75V_{\text{REF}}, IN^- = 0.25V_{\text{REF}})</td>
<td>●</td>
<td>25</td>
<td></td>
<td>ppm of (V_{\text{REF}})</td>
</tr>
<tr>
<td>Positive Full-Scale Error Drift</td>
<td>(2.5V \leq V_{\text{REF}} \leq V_{CC}, IN^+ = 0.75V_{\text{REF}}, IN^- = 0.25V_{\text{REF}})</td>
<td></td>
<td>0.1</td>
<td></td>
<td>ppm of (V_{\text{REF}})</td>
</tr>
<tr>
<td>Negative Full-Scale Error</td>
<td>(2.5V \leq V_{\text{REF}} \leq V_{CC}, IN^+ = 0.75V_{\text{REF}}, IN^- = 0.25V_{\text{REF}})</td>
<td>●</td>
<td>25</td>
<td></td>
<td>ppm of (V_{\text{REF}})</td>
</tr>
<tr>
<td>Negative Full-Scale Error Drift</td>
<td>(2.5V \leq V_{\text{REF}} \leq V_{CC}, IN^+ = 0.75V_{\text{REF}}, IN^- = 0.25V_{\text{REF}})</td>
<td></td>
<td>0.1</td>
<td></td>
<td>ppm of (V_{\text{REF}})</td>
</tr>
<tr>
<td>Total Unadjusted Error</td>
<td>(5V \leq V_{CC} \leq 5.5V, V_{\text{REF}} = 2.5V, V_{\text{IN(CM)}} = 1.25V) (5V \leq V_{CC} \leq 5.5V, V_{\text{REF}} = 5V, V_{\text{IN(CM)}} = 2.5V) (2.7V \leq V_{CC} \leq 5.5V, V_{\text{REF}} = 2.5V, V_{\text{IN(CM)}} = 1.25V)</td>
<td></td>
<td>15</td>
<td></td>
<td>ppm of (V_{\text{REF}}) ppm of (V_{\text{REF}}) ppm of (V_{\text{REF}})</td>
</tr>
<tr>
<td>Output Noise</td>
<td>(5V \leq V_{CC} \leq 5.5V, V_{\text{REF}} = 5V, GND \leq IN^+ = IN^- \leq V_{CC}) (Note 13)</td>
<td></td>
<td>0.6</td>
<td></td>
<td>µVRMS</td>
</tr>
<tr>
<td>Internal PTAT Signal</td>
<td>(T_{A} = 27°C)</td>
<td></td>
<td>390</td>
<td>450</td>
<td>mV</td>
</tr>
</tbody>
</table>

For more information go to: www.linear.com/LTC2484
### ELECTRICAL CHARACTERISTICS (2X SPEED)

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. (Notes 3, 4)

<table>
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<tr>
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<tbody>
<tr>
<td>Resolution (No Missing Codes)</td>
<td>$0.1 \leq V_{REF} \leq V_{CC}, -FS \leq V_{IN} \leq +FS$ (Note 5)</td>
<td>●</td>
<td>24</td>
<td>Bits</td>
<td></td>
</tr>
<tr>
<td>Integral Nonlinearity</td>
<td>$5V \leq V_{CC} \leq 5.5V, V_{REF} = 5V, V_{IN(CM)} = 2.5V$ (Note 6)</td>
<td>●</td>
<td>2</td>
<td>10 ppm of $V_{REF}$</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$2.7V \leq V_{CC} \leq 5.5V, V_{REF} = 2.5V, V_{IN(CM)} = 1.25V$ (Note 6)</td>
<td></td>
<td></td>
<td>ppm of $V_{REF}$</td>
<td></td>
</tr>
<tr>
<td>Offset Error</td>
<td>$2.5V \leq V_{REF} \leq V_{CC}, GND \leq IN^* = IN^- \leq V_{CC}$ (Note 14)</td>
<td>●</td>
<td>0.5</td>
<td>2 mV</td>
<td></td>
</tr>
<tr>
<td>Offset Error Drift</td>
<td>$2.5V \leq V_{REF} \leq V_{CC}, GND \leq IN^* = IN^- \leq V_{CC}$</td>
<td>100</td>
<td>ppm of $V_{REF}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Positive Full-Scale Error</td>
<td>$2.5V \leq V_{REF} \leq V_{CC}, IN^* = 0.75V_{REF}, IN^- = 0.25V_{REF}$</td>
<td>●</td>
<td>25</td>
<td>ppm of $V_{REF}$</td>
<td></td>
</tr>
<tr>
<td>Positive Full-Scale Error Drift</td>
<td>$2.5V \leq V_{REF} \leq V_{CC}, IN^* = 0.75V_{REF}, IN^- = 0.25V_{REF}$</td>
<td>●</td>
<td>0.1</td>
<td>ppm of $V_{REF}$</td>
<td></td>
</tr>
<tr>
<td>Negative Full-Scale Error</td>
<td>$2.5V \leq V_{REF} \leq V_{CC}, IN^* = 0.75V_{REF}, IN^- = 0.25V_{REF}$</td>
<td>●</td>
<td>25</td>
<td>ppm of $V_{REF}$</td>
<td></td>
</tr>
<tr>
<td>Negative Full-Scale Error Drift</td>
<td>$2.5V \leq V_{REF} \leq V_{CC}, IN^* = 0.75V_{REF}, IN^- = 0.25V_{REF}$</td>
<td>●</td>
<td>0.1</td>
<td>ppm of $V_{REF}$</td>
<td></td>
</tr>
<tr>
<td>Output Noise</td>
<td>$5V \leq V_{CC} \leq 5.5V, V_{REF} = 5V, GND \leq IN^* = IN^- \leq V_{CC}$ (Note 13)</td>
<td>0.84</td>
<td>$\mu$VRMS</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. (Notes 3, 4)

<table>
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<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Common Mode Rejection DC</td>
<td>$2.5V \leq V_{REF} \leq V_{CC}, GND \leq IN^* = IN^- \leq V_{CC}$ (Note 5)</td>
<td>●</td>
<td>140</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>Input Common Mode Rejection 50Hz ±2%</td>
<td>$2.5V \leq V_{REF} \leq V_{CC}, GND \leq IN^* = IN^- \leq V_{CC}$ (Note 5)</td>
<td>●</td>
<td>140</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>Input Common Mode Rejection 60Hz ±2%</td>
<td>$2.5V \leq V_{REF} \leq V_{CC}, GND \leq IN^* = IN^- \leq V_{CC}$ (Note 5)</td>
<td>●</td>
<td>140</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>Input Normal Mode Rejection 50Hz ±2%</td>
<td>$2.5V \leq V_{REF} \leq V_{CC}, GND \leq IN^* = IN^- \leq V_{CC}$ (Notes 5, 7)</td>
<td>●</td>
<td>110</td>
<td>120 dB</td>
<td></td>
</tr>
<tr>
<td>Input Normal Mode Rejection 60Hz ±2%</td>
<td>$2.5V \leq V_{REF} \leq V_{CC}, GND \leq IN^* = IN^- \leq V_{CC}$ (Notes 5, 8)</td>
<td>●</td>
<td>110</td>
<td>120 dB</td>
<td></td>
</tr>
<tr>
<td>Input Normal Mode Rejection 50Hz/60Hz ±2%</td>
<td>$2.5V \leq V_{REF} \leq V_{CC}, GND \leq IN^* = IN^- \leq V_{CC}$ (Notes 5, 9)</td>
<td>●</td>
<td>87</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>Reference Common Mode Rejection DC</td>
<td>$2.5V \leq V_{REF} \leq V_{CC}, GND \leq IN^* = IN^- \leq V_{CC}$ (Note 5)</td>
<td>●</td>
<td>120</td>
<td>140 dB</td>
<td></td>
</tr>
<tr>
<td>Power Supply Rejection DC</td>
<td>$V_{REF} = 2.5V, IN^* = IN^- = GND$</td>
<td>120</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power Supply Rejection, 50Hz ±2%</td>
<td>$V_{REF} = 2.5V, IN^* = IN^- = GND$ (Note 7)</td>
<td>120</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power Supply Rejection, 60Hz ±2%</td>
<td>$V_{REF} = 2.5V, IN^* = IN^- = GND$ (Note 8)</td>
<td>120</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### ANALOG INPUT AND REFERENCE

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. (Note 3)

<table>
<thead>
<tr>
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</thead>
<tbody>
<tr>
<td>IN*</td>
<td>Absolute/Common Mode IN* Voltage</td>
<td>GND – 0.3V</td>
<td>$V_{CC} + 0.3V$</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IN*</td>
<td>Absolute/Common Mode IN* Voltage</td>
<td>GND – 0.3V</td>
<td>$V_{CC} + 0.3V$</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>FS</td>
<td>Full-Scale of the Differential Input (IN* – IN*)</td>
<td>●</td>
<td>0.5$V_{REF}$</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LSB</td>
<td>Least Significant Bit of the Output Code</td>
<td>●</td>
<td>$FS/2^{24}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IN}$</td>
<td>Input Differential Voltage Range (IN* – IN*)</td>
<td>●</td>
<td>–$FS$</td>
<td>+$FS$</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{REF}$</td>
<td>Reference Voltage Range</td>
<td>●</td>
<td>0.1</td>
<td>$V_{CC}$</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>
### ANALOG INPUT AND REFERENCE

The • denotes the specifications which apply over the full operating temperature range, otherwise specifications are at \( T_A = 25°C \). (Note 3)

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<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>( C_S (IN^+) )</td>
<td>( \text{IN}^+ ) Sampling Capacitance</td>
<td>Sleep Mode, ( \text{IN}^+ = \text{GND} )</td>
<td>•</td>
<td>–10</td>
<td>1</td>
<td>10</td>
</tr>
<tr>
<td>( C_S (IN^-) )</td>
<td>( \text{IN}^- ) Sampling Capacitance</td>
<td>Sleep Mode, ( \text{IN}^- = \text{GND} )</td>
<td>•</td>
<td>–10</td>
<td>1</td>
<td>10</td>
</tr>
<tr>
<td>( C_S (V_{REF}) )</td>
<td>( V_{REF} ) Sampling Capacitance</td>
<td>Sleep Mode, ( V_{REF} = V_{CC} )</td>
<td>•</td>
<td>–100</td>
<td>1</td>
<td>100</td>
</tr>
</tbody>
</table>

### DIGITAL INPUTS AND DIGITAL OUTPUTS

The • denotes the specifications which apply over the full operating temperature range, otherwise specifications are at \( T_A = 25°C \). (Note 3)

<table>
<thead>
<tr>
<th>SYMBOL</th>
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<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{IH} )</td>
<td>High Level Input Voltage</td>
<td>( 2.7V \leq V_{CC} \leq 5.5V ) (Note 16)</td>
<td>•</td>
<td>( V_{CC} – 0.5 )</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( V_{IL} )</td>
<td>Low Level Input Voltage</td>
<td>( 2.7V \leq V_{CC} \leq 5.5V )</td>
<td>•</td>
<td>0.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( V_{IH} )</td>
<td>High Level Input Voltage</td>
<td>( 2.7V \leq V_{CC} \leq 5.5V ) (Note 10)</td>
<td>•</td>
<td>( V_{CC} – 0.5 )</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( V_{IL} )</td>
<td>Low Level Input Voltage</td>
<td>( 2.7V \leq V_{CC} \leq 5.5V ) (Note 10)</td>
<td>•</td>
<td>0.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( I_{IN} )</td>
<td>Digital Input Current</td>
<td>( 0V \leq V_{IN} \leq V_{CC} )</td>
<td>•</td>
<td>–10</td>
<td>10</td>
<td>µA</td>
</tr>
<tr>
<td>( I_{IN} )</td>
<td>Digital Input Current</td>
<td>( 0V \leq V_{IN} \leq V_{CC} ) (Note 10)</td>
<td>•</td>
<td>–10</td>
<td>10</td>
<td>µA</td>
</tr>
<tr>
<td>( C_{IN} )</td>
<td>Digital Input Capacitance</td>
<td>( 25°C )</td>
<td>10</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>( C_{IN} )</td>
<td>Digital Input Capacitance</td>
<td>( 25°C )</td>
<td>10</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>( V_{OH} )</td>
<td>High Level Output Voltage</td>
<td>( I_{O} = –800\mu A )</td>
<td>•</td>
<td>( V_{CC} – 0.5 )</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( V_{OL} )</td>
<td>Low Level Output Voltage</td>
<td>( I_{O} = 1.6mA )</td>
<td>•</td>
<td>0.4</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( V_{DH} )</td>
<td>High Level Output Voltage</td>
<td>( I_{O} = –800\mu A )</td>
<td>•</td>
<td>( V_{CC} – 0.5 )</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( V_{DL} )</td>
<td>Low Level Output Voltage</td>
<td>( I_{O} = 1.6mA )</td>
<td>•</td>
<td>0.4</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( I_{OZ} )</td>
<td>Hi-Z Output Leakage</td>
<td></td>
<td>•</td>
<td>–10</td>
<td>10</td>
<td>µA</td>
</tr>
</tbody>
</table>

### POWER REQUIREMENTS

The • denotes the specifications which apply over the full operating temperature range, otherwise specifications are at \( T_A = 25°C \). (Note 3)

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</tr>
</thead>
<tbody>
<tr>
<td>( V_{CC} )</td>
<td>Supply Voltage</td>
<td></td>
<td>•</td>
<td>2.7</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>( I_{CC} )</td>
<td>Supply Current</td>
<td>Conversion Mode (Note 12)</td>
<td>•</td>
<td>160</td>
<td>250</td>
<td>µA</td>
</tr>
<tr>
<td>( I_{CC} )</td>
<td>Supply Current</td>
<td>Sleep Mode (Note 12)</td>
<td>•</td>
<td>1</td>
<td>2</td>
<td>µA</td>
</tr>
</tbody>
</table>
### Timing Characteristics

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. (Note 3)

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</tr>
</thead>
<tbody>
<tr>
<td>$f_{EOSC}$</td>
<td>External Oscillator Frequency Range</td>
<td>(Note 15)</td>
<td>●</td>
<td>10</td>
<td>1000</td>
<td>kHz</td>
<td></td>
</tr>
<tr>
<td>$f_{HEO}$</td>
<td>External Oscillator High Period</td>
<td></td>
<td>●</td>
<td>0.125</td>
<td>100</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>$f_{LEO}$</td>
<td>External Oscillator Low Period</td>
<td></td>
<td>●</td>
<td>0.125</td>
<td>100</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>$t_{CONV,1}$</td>
<td>Conversion Time for 1x Speed Mode</td>
<td>50Hz Mode</td>
<td>●</td>
<td>157.2</td>
<td>160.3</td>
<td>163.5</td>
<td>ms</td>
</tr>
<tr>
<td></td>
<td></td>
<td>60Hz Mode</td>
<td>●</td>
<td>131.0</td>
<td>133.6</td>
<td>136.3</td>
<td>ms</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Simultaneous 50Hz/60Hz Mode</td>
<td></td>
<td>144.1</td>
<td>146.9</td>
<td>149.9</td>
<td>ms</td>
</tr>
<tr>
<td></td>
<td></td>
<td>External Oscillator</td>
<td></td>
<td>41036/$f_{EOSC}$ (in kHz)</td>
<td></td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>$t_{CONV,2}$</td>
<td>Conversion Time for 2x Speed Mode</td>
<td>50Hz Mode</td>
<td>●</td>
<td>78.7</td>
<td>80.3</td>
<td>81.9</td>
<td>ms</td>
</tr>
<tr>
<td></td>
<td></td>
<td>60Hz Mode</td>
<td>●</td>
<td>65.6</td>
<td>66.9</td>
<td>68.2</td>
<td>ms</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Simultaneous 50Hz/60Hz Mode</td>
<td></td>
<td>72.2</td>
<td>73.6</td>
<td>75.1</td>
<td>ms</td>
</tr>
<tr>
<td></td>
<td></td>
<td>External Oscillator</td>
<td></td>
<td>20556/$f_{EOSC}$ (in kHz)</td>
<td></td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>$f_{ISCK}$</td>
<td>Internal SCK Frequency</td>
<td>Internal Oscillator (Note 10)</td>
<td>●</td>
<td>38.4</td>
<td></td>
<td></td>
<td>kHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>External Oscillator (Notes 10, 11)</td>
<td></td>
<td>$f_{EOSC}$/8</td>
<td></td>
<td></td>
<td>kHz</td>
</tr>
<tr>
<td>$D_{ISCK}$</td>
<td>Internal SCK Duty Cycle</td>
<td>(Note 10)</td>
<td>●</td>
<td>45</td>
<td>55</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>$f_{ESCK}$</td>
<td>External SCK Frequency Range</td>
<td>(Note 10)</td>
<td>●</td>
<td>4000</td>
<td></td>
<td></td>
<td>kHz</td>
</tr>
<tr>
<td>$t_{LESC}$</td>
<td>External SCK Low Period</td>
<td>(Note 10)</td>
<td>●</td>
<td>125</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{HESC}$</td>
<td>External SCK High Period</td>
<td>(Note 10)</td>
<td>●</td>
<td>125</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{DOUT-ISCK}$</td>
<td>Internal SCK 32-Bit Data Output Time</td>
<td>Internal Oscillator (Notes 10, 12)</td>
<td>●</td>
<td>0.81</td>
<td>0.83</td>
<td>0.85</td>
<td>ms</td>
</tr>
<tr>
<td></td>
<td></td>
<td>External Oscillator (Notes 10, 11)</td>
<td></td>
<td>256/$f_{EOSC}$ (in kHz)</td>
<td></td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>$t_{DOUT-ESCK}$</td>
<td>External SCK 32-Bit Data Output Time</td>
<td>(Note 10)</td>
<td>●</td>
<td>32/$f_{ESCK}$ (in kHz)</td>
<td></td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>$t_1$</td>
<td>$CS\downarrow$ to SDO Low</td>
<td></td>
<td>●</td>
<td>0</td>
<td>200</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_2$</td>
<td>$CS\uparrow$ to SDO Hi-Z</td>
<td></td>
<td>●</td>
<td>0</td>
<td>200</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_3$</td>
<td>$CS\downarrow$ to SCK↓</td>
<td>(Note 10)</td>
<td>●</td>
<td>0</td>
<td>200</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_4$</td>
<td>$CS\uparrow$ to SCK↑</td>
<td>(Note 10)</td>
<td>●</td>
<td>50</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{KQMAX}$</td>
<td>SCK↓ to SDO Valid</td>
<td>(Note 5)</td>
<td>●</td>
<td>15</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{KQMIN}$</td>
<td>SDO Hold After SCK↓</td>
<td>(Note 5)</td>
<td>●</td>
<td>50</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_5$</td>
<td>SCK Set-Up Before $CS\downarrow$</td>
<td></td>
<td>●</td>
<td>50</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_6$</td>
<td>SCK Hold After $CS\uparrow$</td>
<td></td>
<td>●</td>
<td>100</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_7$</td>
<td>SDI Setup Before SCK↑</td>
<td>(Note 5)</td>
<td>●</td>
<td>100</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_8$</td>
<td>SDI Hold After SCK↑</td>
<td>(Note 5)</td>
<td>●</td>
<td>100</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** All voltage values are with respect to GND.

**Note 3:** $V_{CC} = 2.7V$ to 5.5V unless otherwise specified. 
$V_{REFCM} = V_{REF}/2$, $FS = 0.5\cdot V_{REF}$
$V_{IN} = IN^* - IN^*$, $V_{IN(cm)} = (IN^* + IN^*)/2$

**Note 4:** Use internal conversion clock or external conversion clock source with $f_{EOSC} = 307.2kHz$ unless otherwise specified.

**Note 5:** Guaranteed by design, not subject to test.

**Note 6:** Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

**Note 7:** $50Hz$ mode (internal oscillator) or $f_{EOSC} = 256kHz \pm 2\%$ (external oscillator).

**Note 8:** $60Hz$ mode (internal oscillator) or $f_{EOSC} = 307.2kHz \pm 2\%$ (external oscillator).

**Note 9:** Simultaneous $50Hz/60Hz$ mode (internal oscillator) or $f_{EOSC} = 280kHz \pm 2\%$ (external oscillator).

**Note 10:** The SCK can be configured in external SCK mode or internal SCK mode. In external SCK mode, the SCK pin is used as digital input and the driving clock is $f_{ESCK}$. In internal SCK mode, the SCK pin is used as digital output and the output clock signal during the data output is $f_{ISCK}$.

**Note 11:** The external oscillator is connected to the $f_{O}$ pin. The external oscillator frequency, $f_{EOSC}$, is expressed in kHz.

**Note 12:** The converter uses the internal oscillator.

**Note 13:** The output noise includes the contribution of the internal calibration operations.

**Note 14:** Guaranteed by design and test correlation.

**Note 15:** Refer to Applications Information section for performance vs data rate graphs.

**Note 16:** For $V_{CC} < 3V$, $V_{IH}$ is 2.5V for pin $f_{O}$.
TYPICAL PERFORMANCE CHARACTERISTICS

Integral Nonlinearity  
(V\text{CC} = 5V, \text{V\text{REF}} = 5V)

Integral Nonlinearity  
(V\text{CC} = 5V, \text{V\text{REF}} = 2.5V)

Integral Nonlinearity  
(V\text{CC} = 2.7V, \text{V\text{REF}} = 2.5V)

Total Unadjusted Error  
(V\text{CC} = 5V, \text{V\text{REF}} = 5V)

Total Unadjusted Error  
(V\text{CC} = 5V, \text{V\text{REF}} = 2.5V)

Total Unadjusted Error  
(V\text{CC} = 2.7V, \text{V\text{REF}} = 2.5V)

Noise Histogram (6.8sps)  
10,000 CONSECUTIVE READINGS  
V\text{CC} = 5V, \text{V\text{REF}} = 5V, \text{VIN} = 0V, \text{TA} = 25°C  
RMS = 0.60\mu V  
AVERAGE = 0.69\mu V

Noise Histogram (7.5sps)  
10,000 CONSECUTIVE READINGS  
V\text{CC} = 2.7V, \text{V\text{REF}} = 2.5V, \text{VIN} = 0V, \text{VIN(CM)} = 2.5V  
RMS = 0.59\mu V  
AVERAGE = -0.19\mu V

Long-Term ADC Readings  
V\text{CC} = 5V, \text{V\text{REF}} = 5V, \text{VIN} = 0V, \text{VIN(CM)} = 2.5V  
\text{TA} = 25°C, RMS NOISE = 0.60\mu V
**TYPICAL PERFORMANCE CHARACTERISTICS**

### RMS Noise vs Input Differential Voltage

- $V_{CC} = 5V$
- $V_{REF} = 5V$
- $V_{IN(CM)} = 2.5V$
- $T_A = 25^\circ C$

### RMS Noise vs $V_{IN(CM)}$

- $V_{CC} = 5V$
- $V_{REF} = 5V$
- $V_{IN} = 0V$
- $V_{IN(CM)} = GND$
- $T_A = 25^\circ C$

### RMS Noise vs Temperature ($T_A$)

- $V_{CC} = 5V$
- $V_{REF} = 5V$
- $V_{IN} = 0V$
- $V_{IN(CM)} = GND$

### RMS Noise vs $V_{CC}$

- $V_{REF} = 2.5V$
- $V_{IN} = 0V$
- $V_{IN(CM)} = GND$
- $T_A = 25^\circ C$

### Offset Error vs $V_{IN(CM)}$

- $V_{CC} = 5V$
- $V_{REF} = 5V$
- $V_{IN} = 0V$
- $V_{IN(CM)} = GND$
- $T_A = 25^\circ C$

### Offset Error vs Temperature

- $V_{CC} = 5V$
- $V_{REF} = 5V$
- $V_{IN} = 0V$
- $V_{IN(CM)} = GND$
- $T_A = 25^\circ C$

### Offset Error vs $V_{REF}$

- $V_{CC} = 5V$
- $V_{REF} = 5V$
- $V_{IN} = 0V$
- $V_{IN(CM)} = GND$
- $T_A = 25^\circ C$
TYPICAL PERFORMANCE CHARACTERISTICS

Integral Nonlinearity (2x Speed Mode; $V_{CC} = 5V$, $V_{REF} = 2.5V$)

Integral Nonlinearity (2x Speed Mode; $V_{CC} = 2.7V$, $V_{REF} = 2.5V$)

Noise Histogram (2x Speed Mode)

RMS Noise vs $V_{REF}$ (2x Speed Mode)

Offset Error vs $V_{IN(CM)}$ (2x Speed Mode)

Offset Error vs $V_{CC}$ (2x Speed Mode)

Offset Error vs $V_{REF}$ (2x Speed Mode)

PSRR vs Frequency at $V_{CC}$ (2x Speed Mode)

For more information www.linear.com/LTC2484
PIN FUNCTIONS

SDI (Pin 1): Serial Data Input. This pin is used to select the line frequency rejection, input, temperature sensor and 2x speed mode. Data is shifted into the SDI pin on the rising edge of serial clock (SCK).

VCC (Pin 2): Positive Supply Voltage. Bypass to GND (Pin 8) with a 1µF tantalum capacitor in parallel with 0.1µF ceramic capacitor as close to the part as possible.

VREF (Pin 3): Positive Reference Input. The voltage on this pin can have any value between 0.1V and VCC. The negative reference input is GND (Pin 8).

IN+ (Pin 4), IN− (Pin 5): Differential Analog Inputs. The voltage on these pins can have any value between GND – 0.3V and VCC + 0.3V. Within these limits the converter bipolar input range (VIN = IN+ – IN−) extends from \(-0.5 \times V_{REF}\) to \(0.5 \times V_{REF}\). Outside this input range the converter produces unique overrange and underrange output codes.

CS (Pin 6): Active LOW Chip Select. A LOW on this pin enables the digital input/output and wakes up the ADC. Following each conversion the ADC automatically enters the sleep mode and remains in this low power state as long as CS is HIGH. A LOW-to-HIGH transition on CS during the Data Output transfer aborts the data transfer and starts a new conversion.

SDO (Pin 7): Three-State Digital Output. During the data output period, this pin is used as the serial data output. When the chip select, CS, is HIGH (CS = VCC), the SDO pin is in a high impedance state. During the conversion and sleep periods, this pin is used as the conversion status output. The conversion status can be observed by pulling CS LOW.

GND (Pin 8): Ground. Shared pin for analog ground, digital ground and reference ground. Should be connected directly to a ground plane through a minimum impedance.

For more information www.linear.com/LTC2484
PIN FUNCTIONS

SCK (Pin 9): Bidirectional Digital Clock Pin. In internal serial clock operation mode, SCK is used as the digital output for the internal serial interface clock during the data input/output period. In external serial clock operation mode, SCK is used as the digital input for the external serial interface clock during the data output period. A weak internal pull-up is automatically activated in Internal serial clock operation mode. The serial clock operation mode is determined by the logic level applied to the SCK pin at power up or during the most recent falling edge of CS.

f₀ (Pin 10): Frequency Control Pin. Digital input that controls the conversion clock. When f₀ is connected to GND the converter uses its internal oscillator running at 307.2kHz. The conversion clock may also be overridden by driving the f₀ pin with an external clock in order to change the output rate or the digital filter rejection null.

Exposed Pad (Pin 11): This pin is ground and should be soldered to the PCB, GND plane. For prototyping purposes this pin may remain floating.

FUNCTIONAL BLOCK DIAGRAM
### LTC2484

#### TEST CIRCUITS

**Timing Diagrams**

**Timing Diagram Using Internal SCK**

- **CS**
- **SDO**
- **SCK**
- **SDI**
- **SLEEP**
- **DATA IN/OUT**
- **CONVERSION**

**Timing Diagram Using External SCK**

- **CS**
- **SDO**
- **SCK**
- **SDI**
- **SLEEP**
- **DATA IN/OUT**
- **CONVERSION**

For more information [www.linear.com/LTC2484](http://www.linear.com/LTC2484)
APPLICATIONS INFORMATION

CONVERTER OPERATION

Converter Operation Cycle

The LTC2484 is a low power, delta-sigma analog-to-digital converter with an easy to use 4-wire serial interface and automatic differential input current cancellation. Its operation is made up of three states. The converter operating cycle begins with the conversion, followed by the low power sleep state and ends with the data output (see Figure 1). The 4-wire interface consists of serial data output (SDO), serial clock (SCK), chip select (CS) and serial data input (SDI).

Initially, the LTC2484 performs a conversion. Once the conversion is complete, the device enters the sleep state. While in this sleep state, power consumption is reduced by two orders of magnitude. The part remains in the sleep state as long as CS is HIGH. The conversion result is held indefinitely in a static shift register while the converter is in the sleep state.

Once CS is pulled LOW, the device exits the low power mode and enters the data output state. If CS is pulled HIGH before the first rising edge of SCK, the device returns to the low power sleep mode and the conversion result is still held in the internal static shift register. If CS remains LOW after the first rising edge of SCK, the device begins outputting the conversion result. Taking CS HIGH at this point will terminate the data input and output state and start a new conversion. The conversion result is shifted out of the device through the serial data output pin (SDO) on the falling edge of the serial clock (SCK) (see Figure 2). The LTC2484 includes a serial data input pin (SDI) in which data is latched by the device on the rising edge of SCK (Figure 2). The bit stream applied to this pin can be used to select various features of the LTC2484, including an on-chip temperature sensor, line frequency rejection and output data rate. Alternatively, this pin may be tied to ground and the part will perform conversions in a default state. In the default state (SDI grounded) the device simply performs conversions on the user applied input with simultaneous rejection of 50Hz and 60Hz line frequencies.

Figure 1. LTC2484 State Transition Diagram

Figure 2. Input/Output Data Timing
For more information www.linear.com/LTC2484
APPLICATIONS INFORMATION

sensors. Several applications leveraging this feature are presented in more detail in the applications section. While operating in this mode, the speed is set to normal independent of control bit SPD.

Rejection Mode (FA, FB)
The LTC2484 includes a high accuracy on-chip oscillator with no required external components. Coupled with a 4th order digital lowpass filter, the LTC2484 rejects line frequency noise. In the default mode, the LTC2484 simultaneously rejects 50Hz and 60Hz by at least 87dB. The LTC2484 can also be configured to selectively reject 50Hz or 60Hz to better than 110dB.

Speed Mode (SPD)
The LTC2484 continuously performs offset calibrations. Every conversion cycle, two conversions are automatically performed (default) and the results combined. This result is free from offset and drift. In applications where the offset is not critical, the auto-calibration feature can be disabled with the benefit of twice the output rate.

Linearity, full-scale accuracy, full-scale drift are identical for both 2x and 1x speed modes. In both the 1x and 2x speed there is no latency. This enables input steps or multiplexer channel changes to settle in a single conversion cycle easing system overhead and increasing the effective conversion rate.

Output Data Format
The LTC2484 serial output data stream is 32 bits long. The first 3 bits represent status information indicating the sign and conversion state. The next 24 bits are the conversion result, MSB first. The remaining 5 bits are sub LSBs below the 24-bit level. The third and fourth bit together are also used to indicate an underrange condition (the differential input voltage is below –FS) or an overrange condition (the differential input voltage is above +FS).

This bit is HIGH during the conversion and goes LOW when the conversion is complete.

Bit 30 (second output bit) is a dummy bit (DMY) and is always LOW.

Bit 29 (third output bit) is the conversion result sign indicator (SIG). If V_{IN} is >0, this bit is HIGH. If V_{IN} is <0, this bit is LOW.

Bit 28 (fourth output bit) is the most significant bit (MSB) of the result. This bit in conjunction with bit 29 also provides the underrange or overrange indication. If both bit 29 and bit 28 are HIGH, the differential input voltage is above +FS. If both bit 29 and bit 28 are LOW, the differential input voltage is below –FS.

The function of these bits is summarized in Table 2.

<table>
<thead>
<tr>
<th>INPUT RANGE</th>
<th>BIT 31 EOC</th>
<th>BIT 30 DMY</th>
<th>BIT 29 SIG</th>
<th>BIT 28 MSB</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{IN} ≥ 0.5 • V_{REF}</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>0V ≤ V_{IN} &lt; 0.5 • V_{REF}</td>
<td>0</td>
<td>0</td>
<td>1/0</td>
<td>0</td>
</tr>
<tr>
<td>–0.5 • V_{REF} ≤ V_{IN} &lt; 0V</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>V_{IN} &lt; –0.5 • V_{REF}</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Bits 28–5 are the 24-bit conversion result MSB first.

Bits 4–0 are sub LSBs below the 24-bit level. Bits 4–0 may be included in averaging or discarded without loss of resolution.

Data is shifted out of the SDO pin under control of the serial clock (SCK) (see Figure 2). Whenever CS is HIGH, SDO remains high impedance and any externally generated SCK clock pulses are ignored by the internal data out shift register.

In order to shift the conversion result out of the device, CS must first be driven LOW. EOC is seen at the SDO pin of the device once CS is pulled LOW. EOC changes in real time from HIGH to LOW at the completion of a conversion. This signal may be used as an interrupt for an external microcontroller. Bit 31 (EOC) can be captured on the first rising edge of SCK. Bit 30 is shifted out of the device on the first falling edge of SCK. The final data bit (bit 0) is shifted out on the falling edge of the 31st SCK and may be latched on the rising edge of the 32nd SCK pulse. On the falling edge of the 32nd SCK pulse, SDO goes HIGH.
indicating the initiation of a new conversion cycle. This bit serves as EOC (bit 31) for the next conversion cycle. Table 3 summarizes the output data format.

As long as the voltage on the IN+ and IN– pins is maintained within the −0.3V to (VCC + 0.3V) absolute maximum operating range, a conversion result is generated for any differential input voltage $V_{IN}$ from $-FS = -0.5 \cdot V_{REF}$ to $+FS = 0.5 \cdot V_{REF}$. For differential input voltages greater than $+FS$, the conversion result is clamped to the value corresponding to the $+FS + 1LSB$. For differential input voltages below $-FS$, the conversion result is clamped to the value corresponding to $-FS – 1LSB$.

**Conversion Clock**

A major advantage the delta-sigma converter offers over conventional type converters is an on-chip digital filter (commonly implemented as a SINC or Comb filter). For high resolution, low frequency applications, this filter is typically designed to reject line frequencies of 50Hz or 60Hz plus their harmonics. The filter rejection performance is directly related to the accuracy of the converter system clock. The LTC2484 incorporates a highly accurate on-chip oscillator. This eliminates the need for external frequency setting components such as crystals or oscillators.

**Frequency Rejection Selection ($f_0$)**

The LTC2484 internal oscillator provides better than 110dB normal mode rejection at the line frequency and all its harmonics (up to the 255th) for 50Hz ±2% or 60Hz ±2%, or better than 87dB normal mode rejection from 48Hz to 62.4Hz. The rejection mode is selected by writing to the on-chip configuration register and the default mode at POR is simultaneous 50Hz/60Hz rejection.

When a fundamental rejection frequency different from 50Hz or 60Hz is required or when the converter must be synchronized with an outside source, the LTC2484 can operate with an external conversion clock. The converter automatically detects the presence of an external clock signal at the $f_0$ pin and turns off the internal oscillator. The frequency $f_{EOSC}$ of the external signal must be at least 10kHz to be detected. The external clock signal duty cycle is not significant as long as the minimum and maximum specifications for the high and low periods $t_{HEO}$ and $t_{LEO}$ are observed.

While operating with an external conversion clock of a frequency $f_{EOSC}$, the LTC2484 provides better than 110dB normal mode rejection in a frequency range of $f_{EOSC}/5120 ±4\%$ and its harmonics. The normal mode rejection as a function of the input frequency deviation from $f_{EOSC}/5120$ is shown in Figure 3.

**Table 3. LTC2484 Output Data Format**

<table>
<thead>
<tr>
<th>DIFFERENTIAL INPUT VOLTAGE</th>
<th>BIT 31 EOC</th>
<th>BIT 30 DMY</th>
<th>BIT 29 SIG</th>
<th>BIT 28 MSB</th>
<th>BIT 27</th>
<th>BIT 26</th>
<th>BIT 25</th>
<th>…</th>
<th>BIT 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IN}^\ast \geq FS^\ast$</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>…</td>
<td>0</td>
</tr>
<tr>
<td>$FS^\ast – 1LSB$</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>…</td>
<td>1</td>
</tr>
<tr>
<td>$0.5 \cdot FS^\ast$</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>…</td>
<td>0</td>
</tr>
<tr>
<td>$0.5 \cdot FS^\ast – 1LSB$</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>…</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1/0***</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>…</td>
<td>0</td>
</tr>
<tr>
<td>$-1LSB$</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>…</td>
<td>1</td>
</tr>
<tr>
<td>$-0.5 \cdot FS^\ast$</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>…</td>
<td>0</td>
</tr>
<tr>
<td>$-0.5 \cdot FS^\ast – 1LSB$</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>…</td>
<td>1</td>
</tr>
<tr>
<td>$-FS^\ast$</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>…</td>
<td>0</td>
</tr>
<tr>
<td>$V_{IN}^\ast &lt; -FS^\ast$</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>…</td>
<td>1</td>
</tr>
</tbody>
</table>

* The differential input voltage $V_{IN} = IN^\ast – IN^\ast$.
** The full-scale voltage $FS = 0.5 \cdot V_{REF}$.
*** The sign bit changes state during the 0 output code when the device is operating in the 2x speed mode.
**** When operating in the 2x speed mode, the underrange output code is Ox00000000.
Whenever an external clock is not present at the $f_0$ pin, the converter automatically activates its internal oscillator and enters the internal conversion clock mode. The LTC2484 operation will not be disturbed if the change of conversion clock source occurs during the sleep state or during the data output state while the converter uses an external serial clock. If the change occurs during the conversion state, the result of the conversion in progress may be outside specifications but the following conversions will not be affected. If the change occurs during the data output state and the converter is in the Internal SCK mode, the serial clock duty cycle may be affected but the serial data stream will remain valid.

Table 4 summarizes the duration of each state and the achievable output data rate as a function of $f_0$.

### Ease of Use

The LTC2484 data output has no latency, filter settling delay or redundant data associated with the conversion cycle. There is a one-to-one correspondence between the conversion and the output data. Therefore, multiplexing multiple analog voltages is easy.

The LTC2484 performs offset and full-scale calibrations every conversion cycle. This calibration is transparent to the user and has no effect on the cyclic operation described above. The advantage of continuous calibration is extreme stability of offset and full-scale readings with respect to time, supply voltage change and temperature drift.

### Power-Up Sequence

The LTC2484 automatically enters an internal reset state when the power supply voltage $V_{CC}$ drops below approximately 2V. This feature guarantees the integrity of the conversion result and of the serial interface mode selection.

---

**Table 4. LTC2484 State Duration**

<table>
<thead>
<tr>
<th>STATE</th>
<th>OPERATING MODE</th>
<th>DURATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>CONVERT</td>
<td>Internal Oscillator</td>
<td>$60Hz$ Rejection</td>
</tr>
<tr>
<td></td>
<td></td>
<td>133ms, Output Data Rate $\leq 7.5$ Readings/s for 1x Speed Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td>67ms, Output Data Rate $\leq 15$ Readings/s for 2x Speed Mode</td>
</tr>
<tr>
<td></td>
<td>$50Hz$ Rejection</td>
<td>160ms, Output Data Rate $\leq 6.2$ Readings/s for 1x Speed Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td>80ms, Output Data Rate $\leq 12.5$ Readings/s for 2x Speed Mode</td>
</tr>
<tr>
<td></td>
<td>$50Hz/60Hz$ Rejection</td>
<td>147ms, Output Data Rate $\leq 6.8$ Readings/s for 1x Speed Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td>73.6ms, Output Data Rate $\leq 13.6$ Readings/s for 2x Speed Mode</td>
</tr>
<tr>
<td></td>
<td>External Oscillator</td>
<td>$f_0 = \text{External Oscillator with Frequency } f_{EOSC} \text{ kHz} (f_{EOSC}/5120 \text{ Rejection})$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$41036/f_{EOSC}$, Output Data Rate $\leq f_{EOSC}/41036$ Readings/s for 1x Speed Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$20556/f_{EOSC}$, Output Data Rate $\leq f_{EOSC}/20556$ Readings/s for 2x Speed Mode</td>
</tr>
<tr>
<td>SLEEP</td>
<td>As Long As $CS = \text{HIGH}$, After a Conversion is Complete</td>
<td></td>
</tr>
<tr>
<td>DATA OUTPUT</td>
<td>Internal Serial Clock</td>
<td>$f_0 = \text{LOW/HIGH}$ (Internal Oscillator)</td>
</tr>
<tr>
<td></td>
<td>As Long As $CS = \text{LOW But Not Longer Than } 0.83$ms (32 SCK Cycles)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$f_0 = \text{External Oscillator with Frequency } f_{EOSC} \text{ kHz}$</td>
<td></td>
</tr>
<tr>
<td></td>
<td>As Long As $CS = \text{LOW But Not Longer Than } 256/f_{EOSC}$ms (32 SCK Cycles)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>External Serial Clock</td>
<td>$f_{SC} \text{ kHz}$</td>
</tr>
<tr>
<td></td>
<td>As Long As $CS = \text{LOW But Not Longer Than } 32/f_{SC}$ms (32 SCK Cycles)</td>
<td></td>
</tr>
</tbody>
</table>
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When the $V_{CC}$ voltage rises above this critical threshold, the converter creates an internal power-on reset (POR) signal with a duration of approximately 4 ms. The POR signal clears all internal registers. Following the POR signal, the LTC2484 starts a normal conversion cycle and follows the succession of states described in Figure 1. The first conversion result following POR is accurate within the specifications of the device if the power supply voltage is restored within the operating range (2.7 V to 5.5 V) before the end of the POR time interval.

On-Chip Temperature Sensor

The LTC2484 contains an on-chip PTAT (proportional to absolute temperature) signal that can be used as a temperature sensor. The internal PTAT has a typical value of 420 mV at 27 °C and is proportional to the absolute temperature value with a temperature coefficient of $420/(27 + 273) = 1.40$ mV/°C (SLOPE), as shown in Figure 4. The internal PTAT signal is used in a single-ended mode referenced to device ground internally. The 1x speed mode with automatic offset calibration is automatically selected for the internal PTAT signal measurement as well.

When using the internal temperature sensor, if the output code is normalized to \( R_{SDO} = \frac{V_{PTAT}}{V_{REF}} \), the temperature is calculated using the following formula:

\[
T_K = \frac{R_{SDO} \times V_{REF}}{SLOPE} \text{ in Kelvin}
\]

and

\[
T_C = \frac{R_{SDO} \times V_{REF}}{SLOPE} - 273 \text{ in °C}
\]

where SLOPE is nominally 1.4 mV/°C

Since the PTAT signal can have an initial value variation which results in errors in SLOPE, to achieve better temperature measurements, a one-time calibration is needed to adjust the SLOPE value. The converter output of the PTAT signal, $R_{O SDO}$, is measured at a known temperature $T_0$ (in °C) and the SLOPE is calculated as:

\[
SLOPE = \frac{R_{O SDO} \times V_{REF}}{T_0 + 273}
\]

This calibrated SLOPE can be used to calculate the temperature.

If the same $V_{REF}$ source is used during calibration and temperature measurement, the actual value of the $V_{REF}$ is not needed to measure the temperature as shown in the calculation below:

\[
T_C = \frac{R_{SDO} \times V_{REF}}{SLOPE} - 273
\]

\[
= \frac{R_{SDO}}{R_{O SDO}} \times (T_0 + 273) - 273
\]

Reference Voltage Range

The LTC2484 external reference voltage range is 0.1 V to $V_{CC}$. The converter output noise is determined by the thermal noise of the front-end circuits, and as such, its value in nanovolts is nearly constant with reference voltage. A reduced reference voltage will improve the converter performance when operated with an external conversion clock (external $f_O$ signal) at substantially higher output data rates (see the Output Data Rate section). $V_{REF}$ must be ≥1.1 V to use the internal temperature sensor.

The negative reference input to the converter is internally tied to GND. GND (Pin 8) should be connected to a ground plane through as short a trace as possible to minimize voltage drop. The LTC2484 has an average operational current of 160 µA and for 0.1 Ω parasitic resistance, the voltage drop of 16 µV causes a gain error of 3.2 ppm for $V_{REF} = 5$ V.
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Input Voltage Range
The analog input is truly differential with an absolute/common mode range for the IN+ and IN– input pins extending from GND – 0.3V to VCC + 0.3V. Outside these limits, the ESD protection devices begin to turn on and the errors due to input leakage current increase rapidly. Within these limits, the LTC2484 converts the bipolar differential input signal, \( V_{IN} = IN^+ – IN^- \), from –FS to +FS where FS = 0.5 \( \cdot \) VREF. Outside this range, the converter indicates the over-range or the underrange condition using distinct output codes. Since the differential input current cancellation does not rely on an on-chip buffer, current cancellation as well as DC performance is maintained rail-to-rail.

Input signals applied to IN+ and IN– pins may extend by 300mV below ground and above VCC. In order to limit any fault current, resistors of up to 5k may be added in series with the IN+ and IN– pins without affecting the performance of the devices. The effect of the series resistance on the converter accuracy can be evaluated from the curves presented in the Input Current/Reference Current sections. In addition, series resistors will introduce a temperature dependent offset error due to the input leakage current. A 1nA input leakage current will develop a 1ppm offset error on a 5k resistor if VREF = 5V. This error has a very strong temperature dependency.

SERIAL INTERFACE TIMING MODES
The LTC2484’s 4-wire interface is SPI and MICROWIRE compatible. This interface offers several flexible modes of operation. These include internal/external serial clock, 3- or 4-wire I/O, single cycle or continuous conversion. The following sections describe each of these serial interface timing modes in detail. In all these cases, the converter can use the internal oscillator (\( f_0 = \text{LOW} \) or \( f_0 = \text{HIGH} \)) or an external oscillator connected to the \( f_0 \) pin. Refer to Table 5 for a summary.

External Serial Clock, Single Cycle Operation (SPI/MICROWIRE Compatible)
This timing mode uses an external serial clock to shift out the conversion result and a CS signal to monitor and control the state of the conversion cycle (see Figure 5).

The serial clock mode is selected on the falling edge of CS. To select the external serial clock mode, the serial clock pin (SCK) must be LOW during each CS falling edge.

The serial data output pin (SDO) is Hi-Z as long as CS is HIGH. At any time during the conversion cycle, CS may be pulled LOW in order to monitor the state of the converter. While CS is pulled LOW, EOC is output to the SDO pin. EOC = 1 while a conversion is in progress and EOC = 0 if the device is in the sleep state. Independent of CS, the device automatically enters the low power sleep state once the conversion is complete.

When the device is in the sleep state, its conversion result is held in an internal static shift register. The device remains in the sleep state until the first rising edge of SCK is seen while CS is LOW. The input data is then shifted in via the SDI pin on the rising edge of SCK (including the first rising edge) and the output data is shifted out of the SDO pin on each falling edge of SCK. This enables external circuitry to latch the output on the rising edge of SCK. EOC can be latched on the first rising edge of SCK and the last bit of the conversion result can be latched on the 32nd rising edge of SCK. On the 32nd falling edge of SCK, the device begins a new conversion. SD0 goes HIGH (EOC = 1) indicating a conversion is in progress.

Table 5. LTC2484 Interface Timing Modes

<table>
<thead>
<tr>
<th>CONFIGURATION</th>
<th>SCK SOURCE</th>
<th>CONVERSION CYCLE CONTROL</th>
<th>DATA OUTPUT CONTROL</th>
<th>CONNECTION and WAVEFORMS</th>
</tr>
</thead>
<tbody>
<tr>
<td>External SCK, Single Cycle Conversion</td>
<td>External</td>
<td>CS and SCK</td>
<td>CS and SCK</td>
<td>Figures 5, 6</td>
</tr>
<tr>
<td>External SCK, 3-Wire I/O</td>
<td>External</td>
<td>SCK</td>
<td>SCK</td>
<td>Figure 7</td>
</tr>
<tr>
<td>Internal SCK, Single Cycle Conversion</td>
<td>Internal</td>
<td>CS↓</td>
<td>CS↓</td>
<td>Figures 8, 9</td>
</tr>
<tr>
<td>Internal SCK, 3-Wire I/O, Continuous Conversion</td>
<td>Internal</td>
<td>Continuous</td>
<td>Internal</td>
<td>Figure 10</td>
</tr>
</tbody>
</table>
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Figure 5. External Serial Clock, Single Cycle Operation

Figure 6. External Serial Clock, Reduced Data Output Length

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At the conclusion of the data cycle, CS may remain LOW and EOC monitored as an end-of-conversion interrupt. Alternatively, CS may be driven HIGH setting SDO to Hi-Z. As described above, CS may be pulled LOW at any time in order to monitor the conversion status.

Typically, CS remains LOW during the data output state. However, the data output state may be aborted by pulling CS HIGH anytime between the first rising edge and the 32nd falling edge of SCK (see Figure 6). On the rising edge of CS, the device aborts the data output state and immediately initiates a new conversion. If the device has not finished loading the last input bit SPD of SDI by the time CS is pulled HIGH, the SDI information is discarded and the previous configuration is kept. This is useful for systems not requiring all 32 bits of output data, aborting an invalid conversion cycle or synchronizing the start of a conversion.

External Serial Clock, 3-Wire I/O

This timing mode utilizes a 3-wire serial I/O interface. The conversion result is shifted out of the device by an externally generated serial clock (SCK) signal (see Figure 7).

CS may be permanently tied to ground, simplifying the user interface or transmission over an isolation barrier.

The external serial clock mode is selected at the end of the power-on reset (POR) cycle. The POR cycle is concluded typically 4ms after VCC exceeds approximately 2V. The level applied to SCK at this time determines if SCK is internal or external. SCK must be driven LOW prior to the end of POR in order to enter the external serial clock timing mode.

Since CS is tied LOW, the end-of-conversion (EOC) can be continuously monitored at the SDO pin during the convert and sleep states. EOC may be used as an interrupt to an external controller indicating the conversion result is ready. EOC = 1 while the conversion is in progress and EOC = 0 once the conversion ends. On the falling edge of EOC, the conversion result is loaded into an internal static shift register. The input data is then shifted in via the SDI pin on the rising edge of SCK (including the first rising edge) and the output data is shifted out of the SDO pin on each falling edge of SCK. EOC can be latched on the first rising edge of SCK. On the 32nd falling edge of SCK, SDO goes HIGH (EOC = 1) indicating a new conversion has begun.

---

**Figure 7. External Serial Clock, CS = 0 Operation**
Internal Serial Clock, Single Cycle Operation

This timing mode uses an internal serial clock to shift out the conversion result and a CS signal to monitor and control the state of the conversion cycle (see Figure 8).

In order to select the internal serial clock timing mode, the serial clock pin (SCK) must be floating (Hi-Z) or pulled HIGH prior to the falling edge of CS. The device will not enter the internal serial clock mode if SCK is driven LOW on the falling edge of CS. An internal weak pull-up resistor is active on the SCK pin during the falling edge of CS; therefore, the internal serial clock timing mode is automatically selected if SCK is not externally driven.

The serial data output pin (SDO) is Hi-Z as long as CS is HIGH. At any time during the conversion cycle, CS may be pulled LOW in order to monitor the state of the converter. Once CS is pulled LOW, SCK goes LOW and EOC is output to the SDO pin. EOC = 1 while a conversion is in progress and EOC = 0 if the device is in the sleep state.

When testing EOC, if the conversion is complete (EOC = 0), the device will exit the low power mode during the EOC test. In order to allow the device to return to the low power sleep state, CS must be pulled HIGH before the first rising edge of SCK. In the internal SCK timing mode, SCK goes HIGH and the device begins outputting data at time t_{EOCtest} after the falling edge of CS (if EOC = 0) or t_{EOCtest} after EOC goes LOW (if CS is LOW during the falling edge of EOC). The value of t_{EOCtest} is 12μs if the device is using its internal oscillator. If fO is driven by an external oscillator of frequency f_{EOSC}, then t_{EOCtest} is 3.6/f_{EOSC} in seconds. If CS is pulled HIGH before time t_{EOCtest}, the device returns to the sleep state and the conversion result is held in the internal static shift register.

If CS remains LOW longer than t_{EOCtest}, the first rising edge of SCK will occur and the conversion result is serially shifted out of the SDO pin. The data I/O cycle concludes after the 32nd rising edge. The input data is shifted in via the SDI pin on the rising edge of SCK (including the first rising edge) and the output data is shifted out of the SDO pin on each falling edge of SCK. The internally generated serial clock is output to the SCK pin. This signal may be used to shift the conversion result into external circuitry. EOC can be latched on the first rising edge of SCK and the last bit of the conversion result on the 32nd rising edge of SCK. After the 32nd rising edge, SDO goes HIGH (EOC = 1), SCK stays HIGH and a new conversion starts. CS remains LOW during the data output state. However, the data output state may be aborted by pulling CS HIGH anytime between the first and 32nd rising edge of SCK (see Figure 9). On the rising edge of CS, the device aborts the data output state and immediately initiates a new conversion. If the device has not finished loading the last input bit (SPD) of SDI by the time CS is pulled HIGH, the SDI information is discarded and the previous configuration is still kept. This is useful for systems not requiring all 32 bits of output data, aborting an invalid conversion cycle, or synchronizing the start of a conversion. If CS is pulled HIGH while the converter is driving SCK LOW, the internal pull-up is not available to restore SCK to a logic HIGH state. This will cause the device to exit the internal serial clock mode on the next falling edge of CS. This can be avoided by adding an external 10k pull-up resistor to the SCK pin or by never pulling CS HIGH when SCK is LOW.

Whenever SCK is LOW, the LTC2484’s internal pull-up at pin SCK is disabled. Normally, SCK is not externally driven if the device is in the internal SCK timing mode. However, certain applications may require an external driver on SCK. If this driver goes Hi-Z after outputting a LOW signal, the LTC2484’s internal pull-up remains disabled. Hence, SCK remains LOW. On the next falling edge of CS, the device is switched to the external SCK timing mode. By adding an external 10k pull-up resistor to SCK, this pin goes HIGH once the external driver goes Hi-Z. On the next CS falling edge, the device will remain in the internal SCK timing mode.

A similar situation may occur during the sleep state when CS is pulsed HIGH-LOW-HIGH in order to test the conversion status. If the device is in the sleep state (EOC = 0), SCK will go LOW. Once CS goes HIGH (within the time period defined above as t_{EOCtest}), the internal pull-up is activated. For a heavy capacitive load on the SCK pin, the internal pull-up may not be adequate to return SCK to a HIGH level before CS goes low again. This is not a concern under normal conditions where CS remains LOW after detecting EOC = 0. This situation is easily overcome by adding an external 10k pull-up resistor to the SCK pin.
Figure 8. Internal Serial Clock, Single Cycle Operation

Figure 9. Internal Serial Clock, Reduce Data Output Length
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Internal Serial Clock, 3-Wire I/O, Continuous Conversion

This timing mode uses a 3-wire interface. The conversion result is shifted out of the device by an internally generated serial clock (SCK) signal, see Figure 10. CS may be permanently tied to ground, simplifying the user interface or transmission over an isolation barrier.

The internal serial clock mode is selected at the end of the power-on reset (POR) cycle. The POR cycle is concluded approximately 1ms after VCC exceeds 2V. An internal weak pull-up is active during the POR cycle; therefore, the internal serial clock timing mode is automatically selected if SCK is not externally driven LOW (if SCK is loaded such that the internal pull-up cannot pull the pin HIGH, the external SCK mode will be selected).

During the conversion, the SCK and the serial data output pin (SDO) are HIGH (EOC = 1). Once the conversion is complete, SCK and SDO go LOW (EOC = 0) indicating the conversion has finished and the device has entered the low power sleep state. The part remains in the sleep state a minimum amount of time (1/2 the internal SCK period) then immediately begins outputting data. The data input/output cycle begins on the first rising edge of SCK and ends after the 32nd rising edge. The input data is then shifted in via the SDI pin on the rising edge of SCK (including the first rising edge) and the output data is shifted out of the SDO pin on each falling edge of SCK. The internally generated serial clock is output to the SCK pin. This signal may be used to shift the conversion result into external circuitry. EOC can be latched on the first rising edge of SCK and the last bit of the conversion result can be latched on the 32nd rising edge of SCK. After the 32nd rising edge, SDO goes HIGH (EOC = 1) indicating a new conversion is in progress. SCK remains HIGH during the conversion.

![Figure 10. Internal Serial Clock, CS = 0 Continuous Operation](image-url)
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Preserving the Converter Accuracy

The LTC2484 is designed to reduce as much as possible the conversion result sensitivity to device decoupling, PCB layout, anti-aliasing circuits, line frequency perturbations and so on. Nevertheless, in order to preserve the 24-bit accuracy capability of this part, some simple precautions are required.

Digital Signal Levels

The LTC2484’s digital interface is easy to use. Its digital inputs (SDI, fO, CS and SCK in External SCK mode of operation) accept standard CMOS logic levels and the internal hysteresis receivers can tolerate edge transition times as slow as 100µs. However, some considerations are required to take advantage of the exceptional accuracy and low supply current of this converter.

The digital output signals (SDO and SCK in Internal SCK mode of operation) are less of a concern because they are not generally active during the conversion state.

While a digital input signal is in the range 0.5V to (VCC – 0.5V), the CMOS input receiver draws additional current from the power supply. It should be noted that, when any one of the digital input signals (SDI, fO, CS and SCK in External SCK mode of operation) is within this range, the power supply current may increase even if the signal in question is at a valid logic level. For micropower operation, it is recommended to drive all digital input signals to full CMOS levels [VIL < 0.4V and VOH > (VCC – 0.4V)].

During the conversion period, the undershoot and/or overshoot of a fast digital signal connected to the pins can severely disturb the analog to digital conversion process. Undershoot and overshoot occur because of the impedance mismatch at the converter pin when the transition time of an external control signal is less than twice the propagation delay from the driver to the LTC2484. For reference, on a regular FR-4 board, signal propagation velocity is approximately 183ps/inch for internal traces and 170ps/inch for surface traces. Thus, a driver generating a control signal with a minimum transition time of 1ns must be connected to the converter pin through a trace shorter than 2.5 inches. This problem becomes particularly difficult when shared control lines are used and multiple reflections may occur. The solution is to carefully terminate all transmission lines close to their characteristic impedance.

Parallel termination near the LTC2484 pin will eliminate this problem but will increase the driver power dissipation. A series resistor between 27Ω and 56Ω placed near the driver output pin will also eliminate this problem without additional power dissipation. The actual resistor value depends upon the trace impedance and connection topology.

An alternate solution is to reduce the edge rate of the control signals. It should be noted that using very slow edges will increase the converter power supply current during the transition time. The differential input architecture reduces the converter’s sensitivity to ground currents.

Particular attention must be given to the connection of the fO signal when the LTC2484 is used with an external conversion clock. This clock is active during the conversion time and the normal mode rejection provided by the internal digital filter is not very high at this frequency. A normal mode signal of this frequency at the converter reference terminals can result in DC gain and INL errors. A normal mode signal of this frequency at the converter input terminals can result in a DC offset error. Such perturbations can occur due to asymmetric capacitive coupling between the fO signal trace and the converter input and/or reference connection traces. An immediate solution is to maintain maximum possible separation between the fO signal trace and the input/reference signals. When the fO signal is parallel terminated near the converter, substantial AC current is flowing in the loop formed by the fO connection trace, the termination and the ground return path. Thus, perturbation signals may be inductively coupled into the converter input and/or reference. In this situation, the user must reduce to a minimum the loop area for the fO signal as well as the loop area for the differential input and reference connections. Even when fO is not driven, other nearby signals pose similar EMI threats which will be minimized by following good layout practices.
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**Driving the Input and Reference**

The input and reference pins of the LTC2484 converter are directly connected to a network of sampling capacitors. Depending upon the relation between the differential input voltage and the differential reference voltage, these capacitors are switching between these four pins transferring small amounts of charge in the process. A simplified equivalent circuit is shown in Figure 11.

For a simple approximation, the source impedance \( R_S \) driving an analog input pin (IN+, IN–, VREF+ or GND) can be considered to form, together with \( R_{SW} \) and \( C_{EQ} \) (see Figure 11), a first order passive network with a time constant \( \tau = (R_S + R_{SW}) \cdot C_{EQ} \). The converter is able to sample the input signal with better than 1ppm accuracy if the sampling period is at least 14 times greater than the input circuit time constant, \( \tau \). The sampling process on the four input analog pins is quasi-independent so each time constant should be considered by itself and, under worst-case circumstances, the errors may add.

When using the internal oscillator, the LTC2484’s front-end switched-capacitor network is clocked at 123kHz corresponding to an 8.1µs sampling period. Thus, for settling errors of less than 1ppm, the driving source impedance should be chosen such that \( \tau \leq 8.1\mu s/14 = 580\mathrm{ns} \). When an external oscillator of frequency \( f_{EOSC} \) is used, the sampling period is \( 2.5/f_{EOSC} \) and, for a settling error of less than 1ppm, \( \tau \leq 0.178/f_{EOSC} \).

**Automatic Differential Input Current Cancellation**

In applications where the sensor output impedance is low (up to 10kΩ with no external bypass capacitor or up to 500Ω with 0.001µF bypass), complete settling of the input occurs. In this case, no errors are introduced and direct digitization of the sensor is possible.

For many applications, the sensor output impedance combined with external bypass capacitors produces RC time constants much greater than the 580ns required for 1ppm accuracy. For example, a 10kΩ bridge driving a 0.1µF bypass capacitor has a time constant an order of magnitude greater than the required maximum. Historically, settling issues were solved using buffers. These buffers led to increased noise, reduced DC performance (Offset/Drift), limited input/output swing (cannot digitize signals near ground or VCC), added system cost and increased power. The LTC2484 uses a proprietary switching

**Figure 11. LTC2484 Equivalent Analog Input Circuit**

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For more information www.linear.com/LTC2484
algorithm that forces the average differential input current to zero independent of external settling errors. This allows accurate direct digitization of high impedance sensors without the need for buffers. Additional errors resulting from mismatched leakage currents must also be taken into account.

The switching algorithm forces the average input current on the positive input (IIN+) to be equal to the average input current on the negative input (IIN-). Over the complete conversion cycle, the average differential input current (IIN+ - IIN-) is zero. While the differential input current is zero, the common mode input current (IIN+ + IIN-)/2 is proportional to the difference between the common mode input voltage (VINCM) and the common mode reference voltage (VREFCM).

In applications where the input common mode voltage is equal to the reference common mode voltage, as in the case of a balance bridge type application, both the differential and common mode input current are zero. The accuracy of the converter is unaffected by settling errors. Mismatches in source impedances between IN+ and IN- also do not affect the accuracy.

In applications where the input common mode voltage is constant but different from the reference common mode voltage, the differential input current remains zero while the common mode input current is proportional to the difference between VINCM and VREFCM. For a reference common mode of 2.5V and an input common mode of 1.5V, the common mode input current is approximately 0.74µA (in simultaneous 50Hz/60Hz rejection mode). This common mode input current has no effect on the accuracy if the external source impedances tied to IN+ and IN- are matched. Mismatches in these source impedances lead to a fixed offset error but do not affect the linearity or full-scale reading. A 1% mismatch in 1k source resistances leads to a 15ppm shift (74µV) in offset voltage.

In applications where the common mode input voltage varies as a function of input signal level (single-ended input, RTDs, half bridges, current sensors, etc.), the common mode input current varies proportionally with input voltage. For the case of balanced input impedances, the common mode input current effects are rejected by the large CMRR of the LTC2484 leading to little degradation in accuracy. Mismatches in source impedances lead to gain errors proportional to the difference between the common mode input voltage and the common mode reference voltage. 1% mismatches in 1k source resistances lead to gain worst-case gain errors on the order of 15ppm (for 1V differences in reference and input common mode voltage). Table 6 summarizes the effects of mismatched source impedance and differences in reference/input common mode voltages.

<table>
<thead>
<tr>
<th>Table 6. Suggested Input Configuration for LTC2484</th>
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<tr>
<td><strong>BALANCED INPUT RESISTANCES</strong></td>
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<tr>
<td>Constant V_IN(CM) – V_REF(CM)</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>Varying V_IN(CM) – V_REF(CM)</td>
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</tbody>
</table>

The magnitude of the dynamic input current depends upon the size of the very stable internal sampling capacitors and upon the accuracy of the converter sampling clock. The accuracy of the internal clock over the entire temperature and power supply range is typically better than 0.5%. Such a specification can also be easily achieved by an external clock. When relatively stable resistors (50ppm/°C) are used for the external source impedance seen by IN+ and IN-, the expected drift of the dynamic current and offset will be insignificant (about 1% of their respective values over the entire temperature and voltage range). Even for the most stringent applications, a one-time calibration operation may be sufficient.

In addition to the input sampling charge, the input ESD protection diodes have a temperature dependent leakage current. This current, nominally 1nA (≤10nA max), results in a small offset shift. A 1k source resistance will create a 1µV typical and 10µV maximum offset voltage.
Reference Current

In a similar fashion, the LTC2484 samples the differential reference pins $V_{REF}^+$ and GND transferring small amount of charge to and from the external driving circuits thus producing a dynamic reference current. This current does not change the converter offset, but it may degrade the gain and INL performance. The effect of this current can be analyzed in two distinct situations.

For relatively small values of the external reference capacitors ($C_{REF} < 1\text{nF}$), the voltage on the sampling capacitor settles almost completely and relatively large values for the source impedance result in only small errors. Such values for $C_{REF}$ will deteriorate the converter offset and gain performance without significant benefits of reference filtering and the user is advised to avoid them.

Larger values of reference capacitors ($C_{REF} > 1\text{nF}$) may be required as reference filters in certain configurations. Such capacitors will average the reference sampling charge and the external source resistance will see a quasi constant reference differential impedance.

In the following discussion, it is assumed the input and reference common mode are the same. Using internal oscillator for 60Hz mode, the typical differential reference resistance is $1\text{M} \Omega$ which generates a full-scale ($V_{REF}/2$) gain error of 0.51ppm for each ohm of source resistance driving the $V_{REF}$ pin. For 50Hz/60Hz mode, the related difference resistance is $1.1\text{M} \Omega$ and the resulting full-scale error is 0.46ppm for each ohm of source resistance driving the $V_{REF}$ pin. For 50Hz mode, the related difference resistance is $1.2\text{M} \Omega$ and the resulting full-scale error is 0.42ppm for each ohm of source resistance driving the $V_{REF}$ pin. When $f_O$ is driven by an external oscillator with a frequency $f_{EOSC}$ (external conversion clock operation), the typical differential reference resistance is $0.30 \cdot 10^{12}/f_{EOSC}$ \Omega and each ohm of source resistance driving the
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V<sub>REF</sub> pin will result in 1.67 • 10<sup>-6</sup> • f<sub>EOSC</sub>ppm gain error. The typical +FS and –FS errors for various combinations of source resistance seen by the V<sub>REF</sub> pin and external capacitance connected to that pin are shown in Figures 15-18.

In addition to this gain error, the converter INL performance is degraded by the reference source impedance. The INL is caused by the input dependent terms –<sup>2</sup>/(V<sub>REF</sub> • R<sub>EQ</sub>) – (0.5 • V<sub>REF</sub> • D<sub>T</sub>) / R<sub>EQ</sub> in the reference pin current as expressed in Figure 11. When using internal oscillator and 60Hz mode, every 100Ω of reference source resistance translates into about 0.67ppm additional INL error. When using internal oscillator and 50Hz/60Hz mode, every 100Ω of reference source resistance translates into about 0.61ppm additional INL error. When using internal oscillator and 50Hz mode, every 100Ω of reference source resistance translates into about 0.56ppm additional INL error. When f<sub>O</sub> is driven by an external oscillator with a
frequency $f_{EOSC}$, every 100Ω of source resistance driving $V_{REF}$ translates into about $2.18 \times 10^{-6} \times f_{EOSC}$ppm additional INL error. Figure 19 shows the typical INL error due to the source resistance driving the $V_{REF}$ pin when large $C_{REF}$ values are used. The user is advised to minimize the source impedance driving the $V_{REF}$ pin.

![Figure 19. INL vs Differential Input Voltage and Reference Source Resistance for $C_{REF} > 1\mu F$](image)

In applications where the reference and input common mode voltages are different, extra errors are introduced. For every 1V of the reference and input common mode voltage difference ($V_{REFCM} - V_{INCM}$) and a 5V reference, each Ohm of reference source resistance introduces an extra $(V_{REFCM} - V_{INCM})/(V_{REF} \cdot R_{EQ})$ full-scale gain error, which is 0.074ppm when using internal oscillator and 60Hz mode. When using internal oscillator and 50Hz/60Hz mode, the extra full-scale gain error is 0.067ppm. When using internal oscillator and 50Hz mode, the extra gain error is 0.061ppm. If an external clock is used, the corresponding extra gain error is $0.24 \times 10^{-6} \times f_{EOSC}$ppm.

The magnitude of the dynamic reference current depends upon the size of the very stable internal sampling capacitors and upon the accuracy of the converter sampling clock. The accuracy of the internal clock over the entire temperature and power supply range is typically better than 0.5%. Such a specification can also be easily achieved by an external clock. When relatively stable resistors (50ppm/°C) are used for the external source impedance seen by $V_{REF}^+$ and GND, the expected drift of the dynamic current gain error will be insignificant (about 1% of its value over the entire temperature and voltage range). Even for the most stringent applications a one-time calibration operation may be sufficient.

In addition to the reference sampling charge, the reference pins ESD protection diodes have a temperature dependent leakage current. This leakage current, nominally 1nA ($\pm 10nA$ max), results in a small gain error. A 100Ω source resistance will create a 0.05µV typical and 0.5µV maximum full-scale error.

### Output Data Rate

When using its internal oscillator, the LTC2484 produces up to 7.5 samples per second (sps) with a notch frequency of 60Hz, 6.25sps with a notch frequency of 50Hz and 6.8sps with the 50Hz/60Hz rejection mode. The actual output data rate will depend upon the length of the sleep and data output phases which are controlled by the user and which can be made insignificantly short. When operated with an external conversion clock ($f_0$ connected to an external oscillator), the LTC2484 output data rate can be increased as desired. The duration of the conversion phase is $41036/f_{EOSC}$. If $f_{EOSC} = 307.2kHz$, the converter behaves as if the internal oscillator is used and the notch is set at 60Hz.

An increase in $f_{EOSC}$ over the nominal 307.2kHz will translate into a proportional increase in the maximum output data rate. The increase in output rate is nevertheless accompanied by two potential effects, which must be carefully considered.

First, a change in $f_{EOSC}$ will result in a proportional change in the internal notch position and in a reduction of the converter differential mode rejection at the power line frequency. In many applications, the subsequent performance degradation can be substantially reduced by relying upon the LTC2484’s exceptional common mode rejection and by carefully eliminating common mode to differential mode conversion sources in the input circuit. The user should avoid single-ended input filters and should maintain a very high degree of matching and symmetry in the circuits driving the $IN^+$ and $IN^-$ pins.

Second, the increase in clock frequency will increase proportionally the amount of sampling charge transferred.
through the input and the reference pins. If large external input and/or reference capacitors \((C_{IN}, C_{REF})\) are used, the previous section provides formulae for evaluating the effect of the source resistance upon the converter performance for any value of \(f_{EOSC}\). If small external input and/or reference capacitors \((C_{IN}, C_{REF})\) are used, the effect of the external source resistance upon the LTC2484 typical performance can be inferred from Figures 13, 14, 15 and 16 in which the horizontal axis is scaled by \(307200/f_{EOSC}\).

Typical measured performance curves for output data rates up to 25 readings per second are shown in Figures 20 to 27. In order to obtain the highest possible level of accuracy from this converter at output data rates above 20 readings per second, the user is advised to maximize the power supply voltage used and to limit the maximum ambient operating temperature. In certain circumstances, a reduction of the differential reference voltage may be beneficial.

![Figure 20. Offset Error vs Output Data Rate and Temperature](image1)

![Figure 21. +FS Error vs Output Data Rate and Temperature](image2)

![Figure 22. –FS Error vs Output Data Rate and Temperature](image3)

![Figure 23. Resolution \((\text{Noise}_{\text{RMS}} \leq 1\text{LSB})\) vs Output Data Rate and Temperature](image4)
Due to the complex filtering and calibration algorithms utilized, the converter input bandwidth is not modeled very accurately by a first order filter with the pole located at the 3dB frequency. When the internal oscillator is used, the shape of the LTC2484 input bandwidth is shown in Figure 28. When an external oscillator of frequency $f_{EOSC}$ is used, the shape of the LTC2484 input bandwidth can be derived from Figure 28, 60Hz mode curve in which the horizontal axis is scaled by $f_{EOSC}/307200$. 

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**APPLICATIONS INFORMATION**

**Input Bandwidth**

The combined effect of the internal SINC$^4$ digital filter and of the analog and digital auto-calibration circuits determines the LTC2484 input bandwidth. When the internal oscillator is used with the notch set at 60Hz, the 3dB input bandwidth is 3.63Hz. When the internal oscillator is used with the notch set at 50Hz, the 3dB input bandwidth is 3.02Hz. If an external conversion clock generator of frequency $f_{EOSC}$ is connected to the $f_O$ pin, the 3dB input bandwidth is $11.8 \times 10^{-6} \times f_{EOSC}$.

---

![Figure 24](image24.png)  
**Figure 24. Resolution (INL$_{MAX} \leq 1$LSB) vs Output Data Rate and Temperature**

![Figure 25](image25.png)  
**Figure 25. Offset Error vs Output Data Rate and Reference Voltage**

![Figure 26](image26.png)  
**Figure 26. Resolution (Noise$_{RMS} \leq 1$LSB) vs Output Data Rate and Reference Voltage**

![Figure 27](image27.png)  
**Figure 27. Resolution (INL$_{MAX} \leq 1$LSB) vs Output Data Rate and Reference Voltage**

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For more information [www.linear.com/LTC2484](http://www.linear.com/LTC2484)
The conversion noise (600nV_{RMS} typical for V_{REF} = 5V) can be modeled by a white noise source connected to a noise free converter. The noise spectral density is 47nV/\sqrt{Hz} for an infinite bandwidth source and 64nV/\sqrt{Hz} for a single 0.5MHz pole source. From these numbers, it is clear that particular attention must be given to the design of external amplification circuits. Such circuits face the simultaneous requirements of very low bandwidth (just a few Hz) in order to reduce the output referred noise and relatively high bandwidth (at least 500kHz) necessary to drive the input switched-capacitor network. A possible solution is a high gain, low bandwidth amplifier stage followed by a high bandwidth unity-gain buffer.

When external amplifiers are driving the LTC2484, the ADC input referred system noise calculation can be simplified by Figure 29. The noise of an amplifier driving the LTC2484 input pin can be modeled as a band limited white noise source. Its bandwidth can be approximated by the bandwidth of a single pole lowpass filter with a corner frequency f_i. The amplifier noise spectral density is n_i. From Figure 29, using f_i as the x-axis selector, we can find on the y-axis the noise equivalent bandwidth f_{eq} of the input driving amplifier. This bandwidth includes the band limiting effects of the ADC internal calibration and filtering. The noise of the driving amplifier referred to the converter input and including all these effects can be calculated as N = n_i \cdot \sqrt{f_{eq}}. The total system noise (referred to the LTC2484 input) can now be obtained by summing as square root of sum of squares the three ADC input referred noise sources: the LTC2484 internal noise, the noise of the IN+ driving amplifier and the noise of the IN- driving amplifier.

If the f_o pin is driven by an external oscillator of frequency f_{EOsc}, Figure 29 can still be used for noise calculation if the x-axis is scaled by f_{EOsc}/307200. For large values of the ratio f_{EOsc}/307200, the Figure 29 plot accuracy begins to decrease, but at the same time the LTC2484 noise floor rises and the noise contribution of the driving amplifiers lose significance.

**Normal Mode Rejection and Anti-Aliasing**

One of the advantages delta-sigma ADCs offer over conventional ADCs is on-chip digital filtering. Combined with a large oversampling ratio, the LTC2484 significantly simplifies anti-aliasing filter requirements. Additionally,
the input current cancellation feature of the LTC2484 allows external lowpass filtering without degrading the DC performance of the device.

The SINC⁴ digital filter provides greater than 120dB normal mode rejection at all frequencies except DC and integer multiples of the modulator sampling frequency (fₛ). The LTC2484’s auto-calibration circuits further simplify the anti-aliasing requirements by additional normal mode signal filtering both in the analog and digital domain. Independent of the operating mode, fₛ = 256 • f₅ = 2048 • fₒᵤ₅(锳) where f₅ is the notch frequency and fₒᵤ₅(_MethodInfo) is the maximum output data rate. In the internal oscillator mode with a 50Hz notch setting, fₛ = 12800Hz, with 50Hz/60Hz rejection, fₛ = 13960Hz and with a 60Hz notch setting fₛ = 15360Hz. In the external oscillator mode, fₛ = fₑₒₛₕ / 20. The performance of the normal mode rejection is shown in Figures 30 and 31.

In 1x speed mode, the regions of low rejection occurring at integer multiples of fₛ have a very narrow bandwidth. Magnified details of the normal mode rejection curves are shown in Figure 32 (rejection near DC) and Figure 33 (rejection at fₛ = 256f₅) where f₅ represents the notch frequency. These curves have been derived for the external oscillator mode but they can be used in all operating modes by appropriately selecting the f₅ value.

The user can expect to achieve this level of performance using the internal oscillator as it is demonstrated by Figures 34, 35 and 36. Typical measured values of the normal mode rejection of the LTC2484 operating with an internal oscillator and a 60Hz notch setting are shown in Figure 34 superimposed over the theoretical calculated curve. Similarly, the measured normal mode rejection of the LTC2484 for the 50Hz rejection mode and 50Hz/60Hz rejection mode are shown in Figures 35 and 36.

As a result of these remarkable normal mode specifications, minimal (if any) anti-alias filtering is required in front of the LTC2484. If passive RC components are placed in front of the LTC2484, the input dynamic current should be considered (see Input Current section). In this case, the differential input current cancellation feature of the LTC2484 allows external RC networks without significant degradation in DC performance.

![Figure 30. Input Normal Mode Rejection, Internal Oscillator and 50Hz Notch Mode](image1)

![Figure 31. Input Normal Mode Rejection, Internal Oscillator and 60Hz Notch Mode of External Oscillator](image2)
Figure 32. Input Normal Mode Rejection at DC

Figure 33. Input Normal Mode Rejection at \( f_s = 256f_N \)

Figure 34. Input Normal Mode Rejection vs Input Frequency with Input Perturbation of 100% Full-Scale (60Hz Notch)

Figure 35. Input Normal Mode Rejection vs Input Frequency with Input Perturbation of 100% Full-Scale (50Hz Notch)

Figure 36. Input Normal Mode Rejection vs Input Frequency with Input Perturbation of 100% Full-Scale (50Hz/60Hz Mode)
Traditional high order delta-sigma modulators, while providing very good linearity and resolution, suffer from potential instabilities at large input signal levels. The proprietary architecture used for the LTC2484 third order modulator resolves this problem and guarantees a predictable stable behavior at input signal levels of up to 150% of full-scale. In many industrial applications, it is not uncommon to have to measure microvolt level signals superimposed over volt level perturbations and the LTC2484 is eminently suited for such tasks. When the perturbation is differential, the specification of interest is the normal mode rejection for large input signal levels. With a reference voltage $V_{REF} = 5V$, the LTC2484 has a full-scale differential input range of 5V peak-to-peak. Figures 37 and 38 show measurement results for the LTC2484 normal mode rejection ratio with a 7.5V peak-to-peak (150% of full-scale) input signal superimposed over the more traditional normal mode rejection ratio results obtained with a 5V peak-to-peak (full-scale) input signal. In Figure 37, the LTC2484 uses the internal oscillator with the notch set at 60Hz ($f_O = LOW$) and in Figure 38 it uses the internal oscillator with the notch set at 50Hz. It is clear that the LTC2484 rejection performance is maintained with no compromises in this extreme situation. When operating with large input signal levels, the user must observe that such signals do not violate the device absolute maximum ratings.

Using the 2x speed mode of the LTC2484, the device bypasses the digital offset calibration operation to double the output data rate. The superior normal mode rejection is maintained as shown in Figures 30 and 31. However, the magnified details near DC and $f_S = 256f_N$ are different.

![Figure 37. Measured Input Normal Mode Rejection vs Input Frequency with Input Perturbation of 150% Full-Scale (60Hz Notch)](image1)

![Figure 38. Measured Input Normal Mode Rejection vs Input Frequency with Input Perturbation of 150% Full-Scale (50Hz Notch)](image2)
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see Figures 39 and 40. In 2x speed mode, the bandwidth is 11.4Hz for the 50Hz rejection mode, 13.6Hz for the 60Hz rejection mode and 12.4Hz for the 50Hz/60Hz rejection mode. Typical measured values of the normal mode rejection of the LTC2484 operating with the internal oscillator and 2x speed mode is shown in Figure 41.

When the LTC2484 is configured in 2x speed mode, by performing a running average, a SINC\(^1\) notch is combined with the SINC\(^4\) digital filter, yielding the normal mode rejection identical as that for the 1x speed mode. The averaging operation still keeps the output rate with the following algorithm:

Result 1 = average (sample 0, sample 1)
Result 2 = average (sample 1, sample 2)

\[ \ldots \]

\[ \text{Result } n = \text{average (sample } n - 1, \text{ sample } n) \]

The main advantage of the running average is that it achieves simultaneous 50Hz/60Hz rejection at twice the effective output rate, as shown in Figure 42. The raw output data provides a better than 70dB rejection over 48Hz to 62.4Hz, which covers both 50Hz ±2% and 60Hz ±2%. With running average on, the rejection is better than 87dB for both 50Hz ±2% and 60Hz ±2%.

Complete Thermocouple Measurement System with Cold Junction Compensation

The LTC2484 is ideal for direct digitization of thermocouples and other low voltage output sensors. The input...
has a typical offset error of 500nV (2.5µV max) offset drift of 10nV/°C and a noise level of 600nV_RMS.

Figure 44 (last page of this data sheet) is a complete type K thermocouple meter. The only signal conditioning is a simple surge protection network. In any thermocouple meter, the cold junction temperature sensor must be at the same temperature as the junction between the thermocouple materials and the copper printed circuit board traces. The tiny LTC2484 can be tucked neatly underneath an Omega MPJ-K-F thermocouple socket ensuring close thermal coupling.

The LTC2484’s 1.4mV/°C PTAT circuit measures the cold junction temperature. Once the thermocouple voltage and cold junction temperature are known, there are many ways of calculating the thermocouple temperature including a straight-line approximation, lookup tables or a polynomial curve fit. Calibration is performed by applying an accurate 500mV to the ADC input derived from an LT®1236 reference and measuring the local temperature with an accurate thermometer as shown in Figure 43. In calibration mode, the up and down buttons are used to adjust the local temperature reading until it matches an accurate thermometer. Both the voltage and temperature calibration are easily automated.

The complete microcontroller code for this application is available on the LTC2484 product Web page at:

http://www.linear.com

It can be used as a template for many different instruments and it illustrates how to generate calibration coefficients for the onboard temperature sensor. Extensive comments detail the operation of the program. The read_LT2484() function controls the operation of the LTC2484 and is listed below for reference.

Figure 43. Calibration Setup
/** read_LTC2484() *********************************************************************/

This is the function that actually does all the work of talking to the LTC2484.
The spi_read() function performs an 8 bit bidirectional transfer on the SPI bus.
Data changes state on falling clock edges and is valid on rising edges, as
determined by the setup_spi() line in the initialize() function.

A good starting point when porting to other processors is to write your own
spi_write function. Note that each processor has its own way of configuring
the SPI port, and different compilers may or may not have built-in functions
for the SPI port. Also, since the state of the LTC2484’s SDO line indicates
when a conversion is complete you need to be able to read the state of this line
through the processor’s serial data input. Most processors will let you read
this pin as if it were a general purpose I/O line, but there may be some that
don’t.

When in doubt, you can always write a “bit bang” function for troubleshooting
purposes.

The “fourbytes” structure allows byte access to the 32 bit return value:

```
struct fourbytes  // Define structure of four consecutive bytes
{               // To allow byte access to a 32 bit int or float.
    int8 te0;      // The make32() function in this compiler will
    int8 te1;      // also work, but a union of 4 bytes and a 32 bit int
    int8 te2;      // is probably more portable.
    int8 te3;      //
};
```

Also note that the lower 4 bits are the configuration word from the previous
conversion. The 4 LSBs are cleared so that
they don’t affect any subsequent mathematical operations. While you can do a
right shift by 4, there is no point if you are going to convert to floating point
numbers - just adjust your scaling constants appropriately.

```
signed int32 read_LTC2484(char config)
{
    union                         // adc_code.bits32    all 32 bits
        {                          // adc_code.by.te0    byte 0
            signed int32 bits32; // adc_code.by.te1    byte 1
            struct fourbytes by; // adc_code.by.te2    byte 2
        } adc_code;                // adc_code.by.te3    byte 3
    output_low(CS);               // Enable LTC2484 SPI interface
    while(input(PIN_C4)) {}       // Wait for end of conversion. The longest
                                  // you will ever wait is one whole conversion period
    // Now is the time to switch any multiplexers because the conversion is finished
    // and you have the whole data output time for things to settle.
    adc_code.by.te3 = 0;          // Set upper byte to zero.
    adc_code.by.te2 = spi_read(config); // Read first byte, send config byte
    adc_code.by.te1 = spi_read(0);  // Read 2nd byte, send speed bit
    adc_code.by.te0 = spi_read(0);  // Read 3rd byte. ‘0’ argument is necessary
                                  // to act as SPI master!! (compiler
                                  // and processor specific.)
    output_high(CS);              // Disable LTC2484 SPI interface

    // Clear configuration bits and subtract offset. This results in
    // a 2’s complement 32 bit integer with the LTC2484’s MSB in the 2^20 position
    adc_code.by.te0 = adc_code.by.te0 & 0xF0;
    adc_code.bits32 = adc_code.bits32 - 0x000200000;

    return adc_code.bits32;
} // End of read_LTC2484()
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1699 Rev C)

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE MO-229 VARIATION OF (WEED-2).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

For more information www.linear.com/LTC2484
# Revision History

(Revision history begins at Rev B)

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<td>Revised Tables 2 and 3.</td>
<td>15, 16</td>
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<td>6/10</td>
<td>Revised Typical Application</td>
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<td>Added Note 16 to V_{IH} Conditions in Digital Inputs and Digital Outputs section</td>
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<td>Corrected Label on G39 in Typical Performance Characteristics</td>
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<td>Corrected typos in Figure 4, Output Data Rate section, and Figures 35, 36, 37, and 38 in Applications Information section</td>
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<td>E</td>
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<td>Clarify temperature sensor performance</td>
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<td>F</td>
<td>10/14</td>
<td>Updated PTAT minimum and maximum values.</td>
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Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.
TYPICAL APPLICATION

Figure 44. Complete Type K Thermocouple Meter

RELATED PARTS

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
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<td>No External Components 5µV Offset, 1.6µVP-P Noise</td>
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<td>LT1236A-5</td>
<td>Precision Bandgap Reference, 5V</td>
<td>0.05% Max Initial Accuracy, 5ppm/°C Drift</td>
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<td>LT1460</td>
<td>Micropower Series Reference</td>
<td>0.075% Max Initial Accuracy, 5ppm/°C Max Drift</td>
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<td>0.3ppm Noise, 4ppm INL, 10ppm Total Unadjusted Error, 200µA</td>
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<td>LTC2401/LTC2402</td>
<td>1-/2-Channel, 24-Bit, No Latency ∆Σ ADCs in MSOP</td>
<td>0.6ppm Noise, 4ppm INL, 10ppm Total Unadjusted Error, 200µA</td>
</tr>
<tr>
<td>LTC2404/LTC2408</td>
<td>4-/8-Channel, 24-Bit, No Latency ∆Σ ADCs with Differential Inputs</td>
<td>0.3ppm Noise, 4ppm INL, 10ppm Total Unadjusted Error, 200µA</td>
</tr>
<tr>
<td>LTC2410</td>
<td>24-Bit, No Latency ∆Σ ADC with Differential Inputs</td>
<td>0.8µVRMS Noise, 2ppm INL</td>
</tr>
<tr>
<td>LTC2411/LTC2411-1</td>
<td>24-Bit, No Latency ∆Σ ADCs with Differential Inputs in MSOP</td>
<td>1.45µVRMS Noise, 4ppm INL, Simultaneous 50Hz/60Hz Rejection (LTC2411-1)</td>
</tr>
<tr>
<td>LTC2413</td>
<td>24-Bit, No Latency ∆Σ ADC with Differential Inputs</td>
<td>Simultaneous 50Hz/60Hz Rejection, 800nVRMS Noise</td>
</tr>
<tr>
<td>LTC2415/LTC2415-1</td>
<td>24-Bit, No Latency ∆Σ ADCs with 15Hz Output Rate</td>
<td>Pin-Compatible with the LTC2410</td>
</tr>
<tr>
<td>LTC2414/LTC2418</td>
<td>8-/16-Channel 24-Bit, No Latency ∆Σ ADCs</td>
<td>0.2ppm Noise, 2ppm INL, 3ppm Total Unadjusted Errors 200µA</td>
</tr>
<tr>
<td>LTC2420</td>
<td>20-Bit, No Latency ∆Σ ADC in SO-8</td>
<td>1.2ppm Noise, 8ppm INL, Pin-Compatible with LTC2400</td>
</tr>
<tr>
<td>LTC2430/LTC2431</td>
<td>20-Bit, No Latency ∆Σ ADCs with Differential Inputs</td>
<td>2.8µV Noise, SSOP-16/MSOP Package</td>
</tr>
<tr>
<td>LTC2435/LTC2435-1</td>
<td>20-Bit, No Latency ∆Σ ADCs with 15Hz Output Rate</td>
<td>3ppm INL, Simultaneous 50Hz/60Hz Rejection</td>
</tr>
<tr>
<td>LTC2440</td>
<td>High Speed, Low Noise 24-Bit ∆Σ ADC</td>
<td>3.5kHz Output Rate, 200mV Noise, 24.6 ENOBs</td>
</tr>
<tr>
<td>LTC2480</td>
<td>16-Bit, No Latency ∆Σ ADC with PGA/Temperature Sensor</td>
<td>Pin-Compatible with LTC2484</td>
</tr>
<tr>
<td>LTC2482</td>
<td>16-Bit, No Latency ∆Σ ADC</td>
<td>Pin-Compatible with LTC2484</td>
</tr>
</tbody>
</table>