FEATURES

- Differential Input and Differential Reference with GND to VCC Common Mode Range
- 2ppm INL, No Missing Codes
- 2.5ppm Full-Scale Error
- 0.1ppm Offset
- 0.16ppm Noise
- Single Conversion Settling Time for Multiplexed Applications
- Internal Oscillator—No External Components Required
- 110dB Min, 50Hz or 60Hz Notch Filter
- 24-Bit ADC in Narrow SSOP-16 Package (SO-8 Footprint)
- Single Supply 2.7V to 5.5V Operation
- Low Supply Current (200µA) and Auto Shutdown
- Fully Differential Version of LTC2400

APPLICATIONS

- Direct Sensor Digitizer
- Weight Scales
- Direct Temperature Measurement
- Gas Analyzers
- Strain-Gauge Transducers
- Instrumentation
- Data Acquisition
- Industrial Process Control
- 6-Digit DVMs

DESCRIPTION

The LTC®2410 is a 2.7V to 5.5V micropower 24-bit differential ΔΣ™ analog to digital converter with an integrated oscillator, 2ppm INL and 0.16ppm RMS noise. It uses delta-sigma technology and provides single cycle settling time for multiplexed applications. Through a single pin, the LTC2410 can be configured for better than 110dB input differential mode rejection at 50Hz or 60Hz ±2%, or it can be driven by an external oscillator for a user defined rejection frequency. The internal oscillator requires no external frequency setting components.

The converter accepts any external differential reference voltage from 0.1V to VCC for flexible ratiometric and remote sensing measurement configurations. The full-scale differential input range is from −0.5VREF to 0.5VREF. The reference common mode voltage, VREFCM, and the input common mode voltage, VINCM, may be independently set anywhere within the GND to VCC range of the LTC2410. The DC common mode input rejection is better than 140dB.

The LTC2410 communicates through a flexible 3-wire digital interface which is compatible with SPI and MICROWIRE protocols.

© LT, LT, LTC, LT M, Linear Technology and the Linear logo are registered trademarks and No Latency ΔΣ is a trademark of Linear Technology Corporation. All other trademarks are the property of their respective owners.

TYPICAL APPLICATION

For more information www.linear.com/LTC2410
**LTC2410**

**ABSOLUTE MAXIMUM RATINGS**
(Notes 1, 2)

Supply Voltage ($V_{CC}$) to GND ................. –0.3V to 7V
Analog Input Pins Voltage
  to GND ........................................ –0.3V to ($V_{CC} + 0.3V$)
Reference Input Pins Voltage
  to GND ........................................ –0.3V to ($V_{CC} + 0.3V$)
Digital Input Voltage to GND .................–0.3V to ($V_{CC} + 0.3V$)
Digital Output Voltage to GND .............–0.3V to ($V_{CC} + 0.3V$)
Operating Temperature Range
  LTC2410C ........................................... 0°C to 70°C
  LTC2410I ...........................................–40°C to 85°C
Storage Temperature Range .................–65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..........300°C

**PIN CONFIGURATION**

**ORDER INFORMATION**

<table>
<thead>
<tr>
<th>LEAD FREE FINISH</th>
<th>TAPE AND REEL</th>
<th>PART MARKING</th>
<th>PACKAGE DESCRIPTION</th>
<th>TEMPERATURE RANGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>LTC2410CGN#PBF</td>
<td>LTC2410CGN#TRPBF</td>
<td>2410</td>
<td>16-Lead Plastic SSOP</td>
<td>0°C to 70°C</td>
</tr>
<tr>
<td>LTC2410IGN#PBF</td>
<td>LTC2410IGN#TRPBF</td>
<td>2410I</td>
<td>16-Lead Plastic SSOP</td>
<td>–40°C to 85°C</td>
</tr>
</tbody>
</table>

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: [http://www.linear.com/leadfree/](http://www.linear.com/leadfree/)
For more information on tape and reel specifications, go to: [http://www.linear.com/tapeandreel/](http://www.linear.com/tapeandreel/)

**ELECTRICAL CHARACTERISTICS**
The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ C$. (Notes 3, 4)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution (No Missing Codes)</td>
<td>$0.1V \leq V_{REF} \leq V_{CC}$, $-0.5 \cdot V_{REF} \leq V_{IN} \leq 0.5 \cdot V_{REF}$ (Note 5)</td>
<td>●</td>
<td>24</td>
<td></td>
<td>Bits</td>
</tr>
<tr>
<td>Integral Nonlinearity</td>
<td>$5V \leq V_{CC} \leq 5.5V$, $REF^+ = 2.5V$, $REF^- = GND$, $V_{INCM} = 1.25V$ (Note 6)</td>
<td>●</td>
<td>1</td>
<td>14</td>
<td>ppm of $V_{REF}$</td>
</tr>
<tr>
<td></td>
<td>$5V \leq V_{CC} \leq 5.5V$, $REF^+ = 5V$, $REF^- = GND$, $V_{INCM} = 2.5V$ (Note 6)</td>
<td>●</td>
<td>2</td>
<td>14</td>
<td>ppm of $V_{REF}$</td>
</tr>
<tr>
<td></td>
<td>$REF^+ = 2.5V$, $REF^- = GND$, $V_{INCM} = 1.25V$ (Note 6)</td>
<td></td>
<td>5</td>
<td></td>
<td>ppm of $V_{REF}$</td>
</tr>
<tr>
<td>Offset Error</td>
<td>$2.5V \leq REF^+ \leq V_{CC}$, $REF^- = GND$, $GND \leq IN^+ = IN^- \leq V_{CC}$ (Note 14)</td>
<td>●</td>
<td>0.5</td>
<td>0.25</td>
<td>µV</td>
</tr>
<tr>
<td>Offset Error Drift</td>
<td>$2.5V \leq REF^+ \leq V_{CC}$, $REF^- = GND$, $GND \leq IN^+ = IN^- \leq V_{CC}$</td>
<td></td>
<td>10</td>
<td></td>
<td>nV/°C</td>
</tr>
<tr>
<td>Positive Full-Scale Error</td>
<td>$2.5V \leq REF^+ \leq V_{CC}$, $REF^- = GND$, $IN^+ = 0.75REF^+$, $IN^- = 0.25 \cdot REF^+$</td>
<td>●</td>
<td>2.5</td>
<td>12</td>
<td>ppm of $V_{REF}$</td>
</tr>
<tr>
<td>Positive Full-Scale Error Drift</td>
<td>$2.5V \leq REF^+ \leq V_{CC}$, $REF^- = GND$, $IN^+ = 0.75REF^+$, $IN^- = 0.25 \cdot REF^+$</td>
<td></td>
<td>0.03</td>
<td></td>
<td>ppm of $V_{REF}$/°C</td>
</tr>
<tr>
<td>Negative Full-Scale Error</td>
<td>$2.5V \leq REF^+ \leq V_{CC}$, $REF^- = GND$, $IN^+ = 0.25 \cdot REF^+$, $IN^- = 0.75 \cdot REF^+$</td>
<td>●</td>
<td>2.5</td>
<td>12</td>
<td>ppm of $V_{REF}$</td>
</tr>
<tr>
<td>Negative Full-Scale Error Drift</td>
<td>$2.5V \leq REF^+ \leq V_{CC}$, $REF^- = GND$, $IN^+ = 0.25 \cdot REF^+$, $IN^- = 0.75 \cdot REF^+$</td>
<td></td>
<td>0.03</td>
<td></td>
<td>ppm of $V_{REF}$/°C</td>
</tr>
</tbody>
</table>

For more information www.linear.com/LTC2410
## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ C$. (Notes 3, 4)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total Unadjusted Error</td>
<td>$5V \leq V_{CC} \leq 5.5V$, $REF^+ = 2.5V$, $REF^- = GND$, $V_{INCM} = 1.25V$</td>
<td>3</td>
<td>3</td>
<td>4</td>
<td>ppm of $V_{REF}$</td>
</tr>
<tr>
<td></td>
<td>$5V \leq V_{CC} \leq 5.5V$, $REF^+ = 5V$, $REF^- = GND$, $V_{INCM} = 2.5V$</td>
<td></td>
<td></td>
<td></td>
<td>ppm of $V_{REF}$</td>
</tr>
<tr>
<td></td>
<td>$REF^+ = 2.5V$, $REF^- = GND$, $V_{INCM} = 1.25V$, (Note 6)</td>
<td></td>
<td></td>
<td></td>
<td>ppm of $V_{REF}$</td>
</tr>
<tr>
<td>Output Noise</td>
<td>$5V \leq V_{CC} \leq 5.5V$, $REF^+ = 5V$, $REF^- = GND$, $GND \leq IN^- \leq IN^+ \leq V_{CC}$, (Note 13)</td>
<td>0.8</td>
<td></td>
<td></td>
<td>$\mu V_{RMS}$</td>
</tr>
</tbody>
</table>

## CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ C$. (Notes 3, 4)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Common Mode Rejection DC</td>
<td>$2.5V \leq REF^+ \leq V_{CC}$, $REF^- = GND$, $GND \leq IN^- \leq IN^+ \leq V_{CC}$</td>
<td>130</td>
<td>140</td>
<td>140</td>
<td>dB</td>
</tr>
<tr>
<td>Input Common Mode Rejection 60Hz ±2%</td>
<td>$2.5V \leq REF^+ \leq V_{CC}$, $REF^- = GND$, $GND \leq IN^- \leq IN^+ \leq V_{CC}$, (Note 7)</td>
<td>140</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Input Common Mode Rejection 50Hz ±2%</td>
<td>$2.5V \leq REF^+ \leq V_{CC}$, $REF^- = GND$, $GND \leq IN^- \leq IN^+ \leq V_{CC}$, (Note 8)</td>
<td>140</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Input Normal Mode Rejection 60Hz ±2%</td>
<td>(Note 7)</td>
<td>110</td>
<td>140</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Input Normal Mode Rejection 50Hz ±2%</td>
<td>(Note 8)</td>
<td>110</td>
<td>140</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Reference Common Mode Rejection DC</td>
<td>$2.5V \leq REF^+ \leq V_{CC}$, $GND \leq REF^- \leq 2.5V$, $V_{REF} = 2.5V$, $IN^- \leq IN^+ = GND$</td>
<td>130</td>
<td>140</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Power Supply Rejection, DC</td>
<td>$REF^+ = 2.5V$, $REF^- = GND$, $IN^- \leq IN^+ = GND$</td>
<td>120</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Power Supply Rejection, 60Hz ±2%</td>
<td>$REF^+ = 2.5V$, $REF^- = GND$, $IN^- \leq IN^+ = GND$, (Note 7)</td>
<td>120</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Power Supply Rejection, 50Hz ±2%</td>
<td>$REF^+ = 2.5V$, $REF^- = GND$, $IN^- \leq IN^+ = GND$, (Note 8)</td>
<td>120</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
</tbody>
</table>

## ANALOG INPUT AND REFERENCE

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ C$. (Note 3)

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>IN£</td>
<td>Absolute/Common Mode IN£ Voltage</td>
<td>$GND - 0.3V$</td>
<td>$V_{CC} + 0.3V$</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IN£</td>
<td>Absolute/Common Mode IN£ Voltage</td>
<td>$GND - 0.3V$</td>
<td>$V_{CC} + 0.3V$</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VIN</td>
<td>Input Differential Voltage Range (IN£ – IN£)</td>
<td>$-V_{REF}/2$</td>
<td>$V_{REF}/2$</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>REF£</td>
<td>Absolute/Common Mode REF£ Voltage</td>
<td>$0.1$</td>
<td>$V_{CC}$</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>REF£</td>
<td>Absolute/Common Mode REF£ Voltage</td>
<td>$GND$</td>
<td>$V_{CC} - 0.1V$</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VREF</td>
<td>Reference Differential Voltage Range (REF£ – REF£)</td>
<td>$0.1$</td>
<td>$V_{CC}$</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CS (IN£)</td>
<td>IN£ Sampling Capacitance</td>
<td>18</td>
<td>pF</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CS (IN£)</td>
<td>IN£ Sampling Capacitance</td>
<td>18</td>
<td>pF</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CS (REF£)</td>
<td>REF£ Sampling Capacitance</td>
<td>18</td>
<td>pF</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CS (REF£)</td>
<td>REF£ Sampling Capacitance</td>
<td>18</td>
<td>pF</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IDC_LEAK (IN£)</td>
<td>IN£ DC Leakage Current</td>
<td>$CS = V_{CC}, IN£ = GND$</td>
<td>$-10$</td>
<td>1</td>
<td>10</td>
<td>nA</td>
</tr>
<tr>
<td>IDC_LEAK (IN£)</td>
<td>IN£ DC Leakage Current</td>
<td>$CS = V_{CC}, IN£ = GND$</td>
<td>$-10$</td>
<td>1</td>
<td>10</td>
<td>nA</td>
</tr>
<tr>
<td>IDC_LEAK (REF£)</td>
<td>REF£ DC Leakage Current</td>
<td>$CS = V_{CC}, REF£ = 5V$</td>
<td>$-10$</td>
<td>1</td>
<td>10</td>
<td>nA</td>
</tr>
<tr>
<td>IDC_LEAK (REF£)</td>
<td>REF£ DC Leakage Current</td>
<td>$CS = V_{CC}, REF£ = GND$</td>
<td>$-10$</td>
<td>1</td>
<td>10</td>
<td>nA</td>
</tr>
</tbody>
</table>
### DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25\degree C$. (Note 3)

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IH}$</td>
<td>High Level Input Voltage</td>
<td>$2.7V \leq V_{CC} \leq 5.5V$</td>
<td>●</td>
<td>2.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$\text{CS, FO}$</td>
<td>$2.7V \leq V_{CC} \leq 3.3V$</td>
<td>●</td>
<td>2.0</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Low Level Input Voltage</td>
<td>$4.5V \leq V_{CC} \leq 5.5V$</td>
<td>●</td>
<td>0.8</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$\text{CS, FO}$</td>
<td>$2.7V \leq V_{CC} \leq 5.5V$</td>
<td>●</td>
<td>0.6</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>High Level Input Voltage</td>
<td>$2.7V \leq V_{CC} \leq 5.5V$</td>
<td>●</td>
<td>2.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>SCK</td>
<td>$2.7V \leq V_{CC} \leq 3.3V$</td>
<td>●</td>
<td>2.0</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Low Level Input Voltage</td>
<td>$4.5V \leq V_{CC} \leq 5.5V$</td>
<td>●</td>
<td>0.8</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>SCK</td>
<td>$2.7V \leq V_{CC} \leq 5.5V$</td>
<td>●</td>
<td>0.6</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{IN}$</td>
<td>Digital Input Current</td>
<td>$0V \leq V_{IN} \leq V_{CC}$</td>
<td>●</td>
<td>–10</td>
<td>10</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td>$\text{CS, FO}$</td>
<td>($Note 9$)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{IN}$</td>
<td>Digital Input Current</td>
<td>$0V \leq V_{IN} \leq V_{CC}$</td>
<td>●</td>
<td>–10</td>
<td>10</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td>SCK</td>
<td>($Note 9$)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$C_{IN}$</td>
<td>Digital Input Capacitance</td>
<td>$\text{CS, FO}$</td>
<td>●</td>
<td>10</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td></td>
<td>SCK</td>
<td>($Note 9$)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>High Level Output Voltage</td>
<td>$I_D = –800\mu A$</td>
<td>●</td>
<td>$V_{CC} – 0.5V$</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>SDO</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Low Level Output Voltage</td>
<td>$I_D = 1.6mA$</td>
<td>●</td>
<td>0.4</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>SDO</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>High Level Output Voltage</td>
<td>$I_D = –800\mu A$</td>
<td>●</td>
<td>$V_{CC} – 0.5V$</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>SCK</td>
<td>($Note 10$)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Low Level Output Voltage</td>
<td>$I_D = 1.6mA$</td>
<td>●</td>
<td>0.4</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>SCK</td>
<td>($Note 10$)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{OZ}$</td>
<td>Hi-Z Output Leakage</td>
<td></td>
<td>●</td>
<td>–10</td>
<td>10</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td>SDO</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25\degree C$. (Note 3)

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$</td>
<td>Supply Voltage</td>
<td></td>
<td>2.7</td>
<td>5.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{CC}$</td>
<td>Supply Current</td>
<td>Conversion Mode</td>
<td>●</td>
<td>200</td>
<td>300</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$CS = 0V$ ($Note 12$)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sleep Mode</td>
<td>●</td>
<td>20</td>
<td>30</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$CS = V_{CC}$ ($Note 12$)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
**TIMING CHARACTERISTICS**  
The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. (Note 3)

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{EOSC}$</td>
<td>External Oscillator Frequency Range</td>
<td>●</td>
<td>2.56</td>
<td>500</td>
<td>kHz</td>
<td></td>
</tr>
<tr>
<td>$t_{HEO}$</td>
<td>External Oscillator High Period</td>
<td>●</td>
<td>0.25</td>
<td>390</td>
<td>μs</td>
<td></td>
</tr>
<tr>
<td>$t_{LEO}$</td>
<td>External Oscillator Low Period</td>
<td>●</td>
<td>0.25</td>
<td>390</td>
<td>μs</td>
<td></td>
</tr>
<tr>
<td>$t_{CONV}$</td>
<td>Conversion Time</td>
<td>●</td>
<td>130.86</td>
<td>133.53</td>
<td>136.20</td>
<td>ms</td>
</tr>
<tr>
<td>$t_{ISCK}$</td>
<td>Internal SCK Frequency</td>
<td>●</td>
<td>160.23</td>
<td>163.44</td>
<td>20510/$f_{EOSC}$ (in kHz)</td>
<td></td>
</tr>
<tr>
<td>$f_{ESCK}$</td>
<td>External SCK Frequency Range</td>
<td>●</td>
<td>19.2</td>
<td>$f_{EOSC}$/8</td>
<td>kHz</td>
<td></td>
</tr>
<tr>
<td>$t_{DSC}$</td>
<td>Internal SCK Duty Cycle</td>
<td>(Note 10)</td>
<td>45</td>
<td>55</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>$t_{ESCK}$</td>
<td>External SCK Low Period</td>
<td>(Note 9)</td>
<td>2000</td>
<td>kHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{ESCK}$</td>
<td>External SCK High Period</td>
<td>(Note 9)</td>
<td>250</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{OUT_ISCK}$</td>
<td>Internal SCK 32-Bit Data Output Time</td>
<td>(Note 10), (Note 11)</td>
<td>1.64</td>
<td>1.67</td>
<td>1.70</td>
<td>ms</td>
</tr>
<tr>
<td>$t_{OUT_ESCK}$</td>
<td>External SCK 32-Bit Data Output Time</td>
<td>(Note 9)</td>
<td>256/$f_{EOSC}$ (in kHz)</td>
<td>ms</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_1$</td>
<td>CS ↓ to SDO Low Z</td>
<td>●</td>
<td>0</td>
<td>200</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_2$</td>
<td>CS ↑ to SDO High Z</td>
<td>●</td>
<td>0</td>
<td>200</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_3$</td>
<td>CS ↓ to SCK ↓</td>
<td>(Note 10)</td>
<td>0</td>
<td>200</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_4$</td>
<td>CS ↓ to SCK ↑</td>
<td>(Note 9)</td>
<td>50</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{NDMA}$</td>
<td>SCK ↓ to SDO Valid</td>
<td>●</td>
<td>220</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{KMIN}$</td>
<td>SDO Hold After SCK ↓</td>
<td>(Note 5)</td>
<td>15</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_5$</td>
<td>SCK Set-Up Before CS ↓</td>
<td>●</td>
<td>50</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_6$</td>
<td>SCK Hold After CS ↓</td>
<td>●</td>
<td>50</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** All voltage values are with respect to GND.

**Note 3:** $V_{CC} = 2.7$ to 5.5V unless otherwise specified.  
$V_{REF} = REF^+ - REF^–$, $V_{REFCM} = (REF^+ + REF^–)/2$;  
$V_{IN} = IN^+ - IN^–$, $V_{INCM} = (IN^+ + IN^–)/2$.

**Note 4:** $F_0$ pin tied to GND or to $V_{CC}$ or to external conversion clock source with $f_{EOSC} = 153600Hz$ unless otherwise specified.

**Note 5:** Guaranteed by design, not subject to test.

**Note 6:** Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

**Note 7:** $F_0 = 0V$ (internal oscillator) or $f_{EOSC} = 153600Hz ±2\%$ (external oscillator).

**Note 8:** $F_0 = V_{CC}$ (internal oscillator) or $f_{EOSC} = 128000Hz ±2\%$ (external oscillator).

**Note 9:** The converter is in external SCK mode of operation such that the SCK pin is used as digital input. The frequency of the clock signal driving SCK during the data output is $f_{ESCK}$ and is expressed in kHz.

**Note 10:** The converter is in internal SCK mode of operation such that the SCK pin is used as digital output. In this mode of operation the SCK pin has a total equivalent load capacitance $C_{LOAD} = 20pF$.

**Note 11:** The external oscillator is connected to the FO pin. The external oscillator frequency, $f_{EOSC}$, is expressed in kHz.

**Note 12:** The converter uses the internal oscillator.  
$F_0 = 0V$ or $F_0 = V_{CC}$.

**Note 13:** The output noise includes the contribution of the internal calibration operations.

**Note 14:** Guaranteed by design and test correlation.
TYPICAL PERFORMANCE CHARACTERISTICS

- **Total Unadjusted Error vs Temperature**:
  - (VCC = 5V, VREF = 5V)
  - (VCC = 5V, VREF = 2.5V)
  - (VCC = 2.7V, VREF = 2.5V)

- **Integral Nonlinearity vs Temperature**:
  - (VCC = 5V, VREF = 5V)
  - (VCC = 5V, VREF = 2.5V)
  - (VCC = 2.7V, VREF = 2.5V)

- **Noise Histogram**:
  - (Output Rate = 7.5Hz, VCC = 5V, VREF = 5V)
  - (Output Rate = 22.5Hz, VCC = 5V, VREF = 5V)
  - (Output Rate = 7.5Hz, VCC = 5V, VREF = 2.5V)

For more information: www.linear.com/LTC2410
TYPICAL PERFORMANCE CHARACTERISTICS

Noise Histogram (Output Rate = 22.5Hz, VCC = 5V, VREF = 2.5V)

Consecutive ADC Readings vs Time

RMS Noise vs VINCM

RMS Noise vs Temperature (TA)

RMS Noise vs VCC

For more information www.linear.com/LTC2410
**LTC2410**

**TYPICAL PERFORMANCE CHARACTERISTICS**

- **RMS Noise vs VREF**
- **Offset Error vs VINCM**
- **Offset Error vs Temperature (T_A)**
- **Offset Error vs VCC**
- **Offset Error vs VREF**
- **+Full-Scale Error vs VCC**
- **–Full-Scale Error vs VREF**
- **–Full-Scale Error vs Temperature (T_A)**

For more information [www.linear.com/LTC2410](http://www.linear.com/LTC2410)
TYPICAL PERFORMANCE CHARACTERISTICS

- Full-Scale Error vs $V_{CC}$
- Full-Scale Error vs $V_{REF}$
- PSRR vs Frequency at $V_{CC}$
- PSRR vs Frequency at $V_{CC}$
- PSRR vs Frequency at $V_{CC}$

Conversion Current vs Temperature ($T_A$)

Conversion Current vs Output Data Rate

Sleep Current vs Temperature ($T_A$)
**PIN FUNCTIONS**

**GND (Pins 1, 7, 8, 9, 10, 15, 16):** Ground. Multiple ground pins internally connected for optimum ground current flow and VCC decoupling. Connect each one of these pins to a ground plane through a low impedance connection. All seven pins must be connected to ground for proper operation.

**VCC (Pin 2):** Positive Supply Voltage. Bypass to GND (Pin 1) with a 10µF tantalum capacitor in parallel with 0.1µF ceramic capacitor as close to the part as possible.

**REF+ (Pin 3), REF− (Pin 4):** Differential Reference Input. The voltage on these pins can have any value between GND and VCC as long as the reference positive input, REF+, is maintained more positive than the reference negative input, REF−, by at least 0.1V.

**IN+ (Pin 5), IN− (Pin 6):** Differential Analog Input. The voltage on these pins can have any value between GND − 0.3V and VCC + 0.3V. Within these limits the converter bipolar input range (VIN = IN+ − IN−) extends from −0.5 • (VREF) to 0.5 • (VREF). Outside this input range the converter produces unique overrange and underrange output codes.

**CS (Pin 11):** Active LOW Digital Input. A LOW on this pin enables the SDO digital output and wakes up the ADC. Following each conversion the ADC automatically enters the Sleep mode and remains in this low power state as long as CS is HIGH. A LOW-to-HIGH transition on CS during the Data Output transfer aborts the data transfer and starts a new conversion.

**SDO (Pin 12):** Three-State Digital Output. During the Data Output period, this pin is used as serial data output. When the chip select CS is HIGH (CS = VCC) the SDO pin is in a high impedance state. During the Conversion and Sleep periods, this pin is used as the conversion status output. The conversion status can be observed by pulling CS LOW.

**SCK (Pin 13):** Bidirectional Digital Clock Pin. In Internal Serial Clock Operation mode, SCK is used as digital output for the internal serial interface clock during the Data Output period. In External Serial Clock Operation mode, SCK is used as digital input for the external serial interface clock during the Data Output period. A weak internal pull-up is automatically activated in Internal Serial Clock Operation mode. The Serial Clock Operation mode is determined by the logic level applied to the SCK pin at power up or during the most recent falling edge of CS.

**F0 (Pin 14):** Frequency Control Pin. Digital input that controls the ADC’s notch frequencies and conversion time. When the F0 pin is connected to VCC (F0 = VCC), the converter uses its internal oscillator and the digital filter first null is located at 50Hz. When the F0 pin is connected to GND (F0 = OV), the converter uses its internal oscillator and the digital filter first null is located at 60Hz. When F0 is driven by an external clock signal with a frequency fEOSC, the converter uses this signal as its system clock and the digital filter first null is located at a frequency fEOSC/2560.
Figure 1. Functional Block Diagram

TEST CIRCUIT

SDO

1.69k

CLOAD = 20pF

Hi-Z TO VDD
VOL TO VDD
VDD TO Hi-Z

SDO

1.69k

CLOAD = 20pF

Hi-Z TO VOL
VOL TO VOL
VOL TO Hi-Z
CONVERTER OPERATION

Converter Operation Cycle

The LTC2410 is a low power, delta-sigma analog-to-digital converter with an easy to use 3-wire serial interface (see Figure 1). Its operation is made up of three states. The converter operating cycle begins with the conversion, followed by the low power sleep state and ends with the data output (see Figure 2). The 3-wire interface consists of serial data output (SDO), serial clock (SCK) and chip select (CS).

Initially, the LTC2410 performs a conversion. Once the conversion is complete, the device enters the sleep state. While in this sleep state, power consumption is reduced by an order of magnitude. The part remains in the sleep state as long as CS is HIGH. The conversion result is held indefinitely in a static shift register while the converter is in the sleep state.

Once CS is pulled LOW, the device begins outputting the conversion result. There is no latency in the conversion result. The data output corresponds to the conversion just performed. This result is shifted out on the serial data out pin (SDO) under the control of the serial clock (SCK). Data is updated on the falling edge of SCK allowing the user to reliably latch data on the rising edge of SCK (see Figure 3). The data output state is concluded once 32 bits are read out of the ADC or when CS is brought HIGH. The device automatically initiates a new conversion and the cycle repeats.

Through timing control of the CS and SCK pins, the LTC2410 offers several flexible modes of operation (internal or external SCK and free-running conversion modes). These various modes do not require programming configuration registers; moreover, they do not disturb the cyclic operation described above. These modes of operation are described in detail in the Serial Interface Timing Modes section.

Conversion Clock

A major advantage the delta-sigma converter offers over conventional type converters is an on-chip digital filter (commonly implemented as a Sinc or Comb filter). For high resolution, low frequency applications, this filter is typically designed to reject line frequencies of 50 or 60Hz plus their harmonics. The filter rejection performance is directly related to the accuracy of the converter system clock. The LTC2410 incorporates a highly accurate on-chip oscillator. This eliminates the need for external frequency setting components such as crystals or oscillators. Clocked by the on-chip oscillator, the LTC2410 achieves a minimum of 110dB rejection at the line frequency (50Hz or 60Hz ±2%).

Ease of Use

The LTC2410 data output has no latency, filter settling delay or redundant data associated with the conversion cycle. There is a one-to-one correspondence between the conversion and the output data. Therefore, multiplexing multiple analog voltages is easy.

The LTC2410 performs offset and full-scale calibrations every conversion cycle. This calibration is transparent to the user and has no effect on the cyclic operation described above. The advantage of continuous calibration is extreme stability of offset and full-scale readings with respect to time, supply voltage change and temperature drift.

Power-Up Sequence

The LTC2410 automatically enters an internal reset state when the power supply voltage $V_{CC}$ drops below approximately 2.2V. This feature guarantees the integrity of the conversion result and of the serial interface mode selection. (See the 2-wire I/O sections in the Serial Interface Timing Modes section.)
APPLICATIONS INFORMATION

When the $V_{CC}$ voltage rises above this critical threshold, the converter creates an internal power-on-reset (POR) signal with a duration of approximately 0.5ms. The POR signal clears all internal registers. Following the POR signal, the LTC2410 starts a normal conversion cycle and follows the succession of states described above. The first conversion result following POR is accurate within the specifications of the device if the power supply voltage is restored within the operating range (2.7V to 5.5V) before the end of the POR time interval.

Reference Voltage Range

This converter accepts a truly differential external reference voltage. The absolute/common mode voltage specification for the REF$^+$ and REF$^-$ pins covers the entire range from GND to $V_{CC}$. For correct converter operation, the REF$^+$ pin must always be more positive than the REF$^-$ pin.

The LTC2410 can accept a differential reference voltage from 0.1V to $V_{CC}$. The converter output noise is determined by the thermal noise of the front-end circuits, and as such, its value in nanovolts is nearly constant with reference voltage. A decrease in reference voltage will not significantly improve the converter’s effective resolution. On the other hand, a reduced reference voltage will improve the converter’s overall INL performance. A reduced reference voltage will also improve the converter performance when operated with an external conversion clock (external $F_0$ signal) at substantially higher output data rates (see the Output Data Rate section).

Input Voltage Range

The analog input is truly differential with an absolute/common mode range for the IN$^+$ and IN$^-$ input pins extending from GND $-$ 0.3V to $V_{CC}$ + 0.3V. Outside these limits, the ESD protection devices begin to turn on and the errors due to input leakage current increase rapidly. Within these limits, the LTC2410 converts the bipolar differential input signal, $V_{IN} = IN^+ - IN^-$, from $-FS = -0.5 \times V_{REF}$ to $+FS = 0.5 \times V_{REF}$ where $V_{REF} = REF^+ - REF^-$. Outside this range, the converter indicates the overrange or the underrange condition using distinct output codes.

Input signals applied to IN$^+$ and IN$^-$ pins may extend by 300mV below ground and above $V_{CC}$. In order to limit any fault current, resistors of up to 5k may be added in series with the IN$^+$ and IN$^-$ pins without affecting the performance of the device. In the physical layout, it is important to maintain the parasitic capacitance of the connection between these series resistors and the corresponding pins as low as possible; therefore, the resistors should be located as close as practical to the pins. The effect of the series resistance on the converter accuracy can be evaluated from the curves presented in the Input Current/Reference Current sections. In addition, series resistors will introduce a temperature dependent offset error due to the input leakage current. A 1nA input leakage current will develop a 1ppm offset error on a 5k resistor if $V_{REF} = 5V$. This error has a very strong temperature dependency.

Output Data Format

The LTC2410 serial output data stream is 32 bits long. The first 3 bits represent status information indicating the sign and conversion state. The next 24 bits are the conversion result, MSB first. The remaining 5 bits are sub LSBs beyond the 24-bit level that may be included in averaging or discarded without loss of resolution. The third and fourth bit together are also used to indicate an underrange condition (the differential input voltage is below $-FS$) or an overrange condition (the differential input voltage is above $+FS$).

Bit 31 (first output bit) is the end of conversion (EOC) indicator. This bit is available at the SDO pin during the conversion and sleep states whenever the CS pin is LOW. This bit is HIGH during the conversion and goes LOW when the conversion is complete.

Bit 30 (second output bit) is a dummy bit (DMY) and is always LOW.

Bit 29 (third output bit) is the conversion result sign indicator (SIG). If $V_{IN}$ is $>0$, this bit is HIGH. If $V_{IN}$ is $<0$, this bit is LOW.

Bit 28 (fourth output bit) is the most significant bit (MSB) of the result. This bit in conjunction with Bit 29 also provides the underrange or overrange indication. If both Bit 29 and Bit 28 are HIGH, the differential input voltage is above $+FS$. For more information www.linear.com/LTC2410
If both Bit 29 and Bit 28 are LOW, the differential input voltage is below –FS.

The function of these bits is summarized in Table 1.

Table 1. LTC2410 Status Bits

<table>
<thead>
<tr>
<th>Input Range</th>
<th>Bit 31</th>
<th>Bit 30</th>
<th>Bit 29</th>
<th>Bit 28</th>
</tr>
</thead>
<tbody>
<tr>
<td>( VIN \geq 0.5 \cdot V_{REF} )</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>( 0 \leq VIN &lt; 0.5 \cdot V_{REF} )</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>(-0.5 \cdot V_{REF} \leq VIN &lt; 0V )</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>( VIN &lt; -0.5 \cdot V_{REF} )</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Bits 28-5 are the 24-bit conversion result MSB first.

Bit 5 is the least significant bit (LSB).

Bits 4-0 are sub LSBs below the 24-bit level. Bits 4-0 may be included in averaging or discarded without loss of resolution.

Data is shifted out of the SDO pin under control of the serial clock (SCK), see Figure 3. Whenever CS is HIGH, SDO remains high impedance and any externally generated SCK clock pulses are ignored by the internal data out shift register.

In order to shift the conversion result out of the device, CS must first be driven LOW. EOC is seen at the SDO pin of the device once CS is pulled LOW. EOC changes real time from HIGH to LOW at the completion of a conversion. This signal may be used as an interrupt for an external microcontroller. Bit 31 (EOC) can be captured on the first rising edge of SCK. Bit 30 is shifted out of the device on the first falling edge of SCK. The final data bit (Bit 0) is shifted out on the falling edge of the 31st SCK and may be latched on the rising edge of the 32nd SCK pulse. On the falling edge of the 32nd SCK pulse, SDO goes HIGH indicating the initiation of a new conversion cycle. This bit serves as EOC (Bit 31) for the next conversion cycle. Table 2 summarizes the output data format.

Table 2. LTC2410 Output Data Format

<table>
<thead>
<tr>
<th>Differential Input Voltage ( VIN^* )</th>
<th>Bit 31 EOC</th>
<th>Bit 30 DMY</th>
<th>Bit 29 SIG</th>
<th>Bit 28 MSB</th>
<th>Bit 27</th>
<th>Bit 26</th>
<th>Bit 25</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>( VIN^* \geq 0.5 \cdot V_{REF}^* )</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>...</td>
</tr>
<tr>
<td>( 0.5 \cdot V_{REF}^* \leq 1\text{LSB} )</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>...</td>
</tr>
<tr>
<td>( 0.25 \cdot V_{REF}^* )</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>...</td>
</tr>
<tr>
<td>( 0.25 \cdot V_{REF}^* \leq 1\text{LSB} )</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>...</td>
</tr>
<tr>
<td>( 0 )</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>...</td>
</tr>
<tr>
<td>(-1\text{LSB} )</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>...</td>
</tr>
<tr>
<td>(-0.25 \cdot V_{REF}^* )</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>...</td>
</tr>
<tr>
<td>(-0.25 \cdot V_{REF}^* \leq 1\text{LSB} )</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>...</td>
</tr>
<tr>
<td>(-0.5 \cdot V_{REF}^* )</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>...</td>
</tr>
<tr>
<td>( VIN^* &lt; -0.5 \cdot V_{REF}^* )</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>...</td>
</tr>
</tbody>
</table>

*The differential Input voltage \( VIN = IN^* - IN^* \).

**The differential reference voltage \( V_{REF} = REF^* - REF^* \).
APPLICATIONS INFORMATION

As long as the voltage on the IN+ and IN– pins is maintained within the –0.3V to (VCC + 0.3V) absolute maximum operating range, a conversion result is generated for any differential input voltage V_IN from –FS = –0.5 • V_REF to +FS = 0.5 • V_REF. For differential input voltages greater than +FS, the conversion result is clamped to the value corresponding to the +FS + 1LSB. For differential input voltages below –FS, the conversion result is clamped to the value corresponding to –FS – 1LSB.

Frequency Rejection Selection (F0)

The LTC2410 internal oscillator provides better than 110dB normal mode rejection at the line frequency and all its harmonics for 50Hz ±2% or 60Hz ±2%. For 60Hz rejection, F0 should be connected to GND while for 50Hz rejection the F0 pin should be connected to VCC.

The selection of 50Hz or 60Hz rejection can also be made by driving F0 to an appropriate logic level. A selection change during the sleep or data output states will not disturb the converter operation. If the selection is made during the conversion state, the result of the conversion in progress may be outside specifications but the following conversions will not be affected.

When a fundamental rejection frequency different from 50Hz or 60Hz is required or when the converter must be synchronized with an outside source, the LTC2410 can operate with an external conversion clock. The converter automatically detects the presence of an external clock signal at the F0 pin and turns off the internal oscillator. The frequency fEOSC of the external signal must be at least 2560Hz (1Hz notch frequency) to be detected. The external clock signal duty cycle is not significant as long as the minimum and maximum specifications for the high and low periods tHEO and tLEO are observed.

While operating with an external conversion clock of a frequency fEOSC, the LTC2410 provides better than 110dB normal mode rejection in a frequency range fEOSC/2560 ±4% and its harmonics. The normal mode rejection as a function of the input frequency deviation from fEOSC/2560 is shown in Figure 4.

Whenever an external clock is not present at the F0 pin, the converter automatically activates its internal oscillator and enters the Internal Conversion Clock mode. The LTC2410 operation will not be disturbed if the change of conversion clock source occurs during the sleep state or during the data output state while the converter uses an external serial clock. If the change occurs during the conversion state, the result of the conversion in progress may be outside specifications but the following conversions will not be affected. If the change occurs during the data output state and the converter is in the Internal SCK mode, the serial clock duty cycle may be affected but the serial data stream will remain valid.

Table 3 summarizes the duration of each state and the achievable output data rate as a function of F0.

SERIAL INTERFACE PINS

The LTC2410 transmits the conversion results and receives the start of conversion command through a synchronous 3-wire interface. During the conversion and sleep states, this interface can be used to assess the converter status and during the data output state it is used to read the conversion result.

Serial Clock Input/Output (SCK)

The serial clock signal present on SCK (Pin 13) is used to synchronize the data transfer. Each bit of data is shifted out the SDO pin on the falling edge of the serial clock.
APPLICATIONS INFORMATION

Table 3. LTC2410 State Duration

<table>
<thead>
<tr>
<th>State</th>
<th>Operating Mode</th>
<th>Duration</th>
</tr>
</thead>
<tbody>
<tr>
<td>CONVERT</td>
<td>Internal Oscillator</td>
<td></td>
</tr>
<tr>
<td></td>
<td>( F_0 = \text{LOW} ) (60Hz Rejection)</td>
<td>133ms, Output Data Rate ( \leq 7.5 ) Readings/s</td>
</tr>
<tr>
<td></td>
<td>( F_0 = \text{HIGH} ) (50Hz Rejection)</td>
<td>160ms, Output Data Rate ( \leq 6.2 ) Readings/s</td>
</tr>
<tr>
<td></td>
<td>External Oscillator</td>
<td></td>
</tr>
<tr>
<td></td>
<td>( F_0 = \text{External Oscillator} ) with Frequency ( f_{EOSC} ) kHz ( (f_{EOSC}/2560 ) Rejection)</td>
<td>20510/( f_{EOSC} ), Output Data Rate ( \leq f_{EOSC}/20510 ) Readings/s</td>
</tr>
<tr>
<td>SLEEP</td>
<td>As Long As ( CS = \text{HIGH} ) Until ( CS = \text{LOW} ) and ( SCK ), ( \downarrow )</td>
<td></td>
</tr>
<tr>
<td>DATA OUTPUT</td>
<td>Internal Serial Clock</td>
<td></td>
</tr>
<tr>
<td></td>
<td>( F_0 = \text{LOW/HIGH} ) (Internal Oscillator)</td>
<td>As Long As ( CS = \text{LOW} ) But Not Longer Than 1.67ms (32 SCK cycles)</td>
</tr>
<tr>
<td></td>
<td>( F_0 = \text{External Oscillator} ) with Frequency ( f_{EOSC} ) kHz</td>
<td>As Long As ( CS = \text{LOW} ) But Not Longer Than 256/( f_{EOSC} )ms (32 SCK cycles)</td>
</tr>
<tr>
<td></td>
<td>External Serial Clock with Frequency ( f_{SDK} ) kHz</td>
<td>As Long As ( CS = \text{LOW} ) But Not Longer Than 32/( f_{SDK} )ms (32 SCK cycles)</td>
</tr>
</tbody>
</table>

In the Internal SCK mode of operation, the SCK pin is an output and the LTC2410 creates its own serial clock by dividing the internal conversion clock by 8. In the External SCK mode of operation, the SCK pin is used as input. The internal or external SCK mode is selected on power-up and then reselected every time a HIGH-to-LOW transition is detected at the \( CS \) pin. If SCK is HIGH or floating at power-up or during this transition, the converter enters the internal SCK mode. If SCK is LOW at power-up or during this transition, the converter enters the external SCK mode.

**Serial Data Output (SDO)**

The serial data output pin, SDO (Pin 12), provides the result of the last conversion as a serial bit stream (MSB first) during the data output state. In addition, the SDO pin is used as an end of conversion indicator during the conversion and sleep states.

When \( CS \) (Pin 11) is HIGH, the SDO driver is switched to a high impedance state. This allows sharing the serial interface with other devices. If \( CS \) is LOW during the convert or sleep state, SDO will output \( EOC \). If \( CS \) is LOW during the conversion phase, the \( EOC \) bit appears HIGH on the SDO pin. Once the conversion is complete, \( EOC \) goes LOW. The device remains in the sleep state until the first rising edge of SCK occurs while \( CS = \text{LOW} \).

**Chip Select Input (\( CS \))**

The active LOW chip select, \( CS \) (Pin 11), is used to test the conversion status and to enable the data output transfer as described in the previous sections.

In addition, the \( CS \) signal can be used to trigger a new conversion cycle before the entire serial data transfer has been completed. The LTC2410 will abort any serial data transfer in progress and start a new conversion cycle anytime a LOW-to-HIGH transition is detected at the \( CS \) pin after the converter has entered the data output state (i.e., after the first rising edge of SCK occurs with \( CS = \text{LOW} \)).

Finally, \( CS \) can be used to control the free-running modes of operation, see Serial Interface Timing Modes section. Grounding \( CS \) will force the ADC to continuously convert at the maximum output rate selected by \( F_0 \). Tying a capacitor to \( CS \) will reduce the output rate and power dissipation by a factor proportional to the capacitor’s value, see Figures 12 to 14.

**SERIAL INTERFACE TIMING MODES**

The LTC2410’s 3-wire interface is SPI and MICROWIRE compatible. This interface offers several flexible modes of operation. These include internal/external serial clock, 2- or 3-wire I/O, single cycle conversion and autostart. The
following sections describe each of these serial interface timing modes in detail. In all these cases, the converter can use the internal oscillator (F₀ = LOW or F₀ = HIGH) or an external oscillator connected to the F₀ pin. Refer to Table 4 for a summary.

**External Serial Clock, Single Cycle Operation (SPI/MICROWIRE Compatible)**

This timing mode uses an external serial clock to shift out the conversion result and a CS signal to monitor and control the state of the conversion cycle, see Figure 5.

The serial clock mode is selected on the falling edge of CS. To select the external serial clock mode, the serial clock pin (SCK) must be LOW during each CS falling edge. The serial data output pin (SDO) is Hi-Z as long as CS is HIGH. At any time during the conversion cycle, CS may be pulled LOW in order to monitor the state of the converter. While CS is pulled LOW, EOC is output to the SDO pin. EOC = 1 while a conversion is in progress and EOC = 0 if the device is in the sleep state. Independent of CS, the device automatically enters the low power sleep state once the conversion is complete.

When the device is in the sleep state (EOC = 0), its conversion result is held in an internal static shift register. The device remains in the sleep state until the first rising edge of SCK is seen while CS is LOW. Data is shifted out the SDO pin on each falling edge of SCK. This enables external circuitry to latch the output on the rising edge of

**Table 4. LTC2410 Interface Timing Modes**

<table>
<thead>
<tr>
<th>Configuration</th>
<th>SCK Source</th>
<th>Conversion Cycle Control</th>
<th>Data Output Control</th>
<th>Connection and Waveforms</th>
</tr>
</thead>
<tbody>
<tr>
<td>External SCK, Single Cycle Conversion</td>
<td>External</td>
<td>CS and SCK</td>
<td>CS and SCK</td>
<td>Figures 5, 6</td>
</tr>
<tr>
<td>External SCK, 2-Wire I/O</td>
<td>External</td>
<td>SCK</td>
<td>SCK</td>
<td>Figure 7</td>
</tr>
<tr>
<td>Internal SCK, Single Cycle Conversion</td>
<td>Internal</td>
<td>CS ↓</td>
<td>CS ↓</td>
<td>Figures 8, 9</td>
</tr>
<tr>
<td>Internal SCK, 2-Wire I/O, Continuous Conversion</td>
<td>Internal</td>
<td>Continuous</td>
<td>Internal</td>
<td>Figure 10</td>
</tr>
<tr>
<td>Internal SCK, Autostart Conversion</td>
<td>Internal</td>
<td>C_EXT</td>
<td>Internal</td>
<td>Figure 11</td>
</tr>
</tbody>
</table>

The serial data output pin (SDO) is Hi-Z as long as CS is HIGH. At any time during the conversion cycle, CS may be pulled LOW in order to monitor the state of the converter. While CS is pulled LOW, EOC is output to the SDO pin. EOC = 1 while a conversion is in progress and EOC = 0 if the device is in the sleep state. Independent of CS, the device automatically enters the low power sleep state once the conversion is complete.

When the device is in the sleep state (EOC = 0), its conversion result is held in an internal static shift register. The device remains in the sleep state until the first rising edge of SCK is seen while CS is LOW. Data is shifted out the SDO pin on each falling edge of SCK. This enables external circuitry to latch the output on the rising edge of

**Figure 5. External Serial Clock, Single Cycle Operation**
SCK. EOC can be latched on the first rising edge of SCK and the last bit of the conversion result can be latched on the 32nd rising edge of SCK. On the 32nd falling edge of SCK, the device begins a new conversion. SDO goes HIGH (EOC = 1) indicating a conversion is in progress.

At the conclusion of the data cycle, CS may remain LOW and EOC monitored as an end-of-conversion interrupt. Alternatively, CS may be driven HIGH setting SDO to Hi-Z. As described above, CS may be pulled LOW at any time in order to monitor the conversion status. Typically, CS remains LOW during the data output state. However, the data output state may be aborted by pulling CS HIGH anytime between the first rising edge and the 32nd falling edge of SCK, see Figure 6. On the rising edge of CS, the device aborts the data output state and immediately initiates a new conversion. This is useful for systems not requiring all 32 bits of output data, aborting an invalid conversion cycle or synchronizing the start of a conversion.

External Serial Clock, 2-Wire I/O

This timing mode utilizes a 2-wire serial I/O interface. The conversion result is shifted out of the device by an externally generated serial clock (SCK) signal, see Figure 7. CS may be permanently tied to ground, simplifying the user interface or isolation barrier.

The external serial clock mode is selected at the end of the power-on reset (POR) cycle. The POR cycle is concluded approximately 0.5ms after Vcc exceeds 2.2V. The level applied to SCK at this time determines if SCK is internal or external. SCK must be driven LOW prior to the end of POR in order to enter the external serial clock timing mode. Since CS is tied LOW, the end-of-conversion (EOC) can be continuously monitored at the SDO pin during the convert and sleep states. EOC may be used as an interrupt to an external controller indicating the conversion result is ready. EOC = 1 while the conversion is in progress and EOC = 0 once the conversion enters the low power sleep state. On the falling edge of EOC, the conversion result is loaded into an internal static shift register. The device remains in the sleep state until the first rising edge of SCK. Data is shifted out the SDO pin on each falling edge of SCK enabling external circuitry to latch data on the rising edge of SCK. EOC can be latched on the first rising edge of SCK. On the 32nd falling edge of SCK, SDO goes HIGH (EOC = 1) indicating a new conversion has begun.

Figure 6. External Serial Clock, Reduced Data Output Length
**APPLICATIONS INFORMATION**

**Internal Serial Clock, Single Cycle Operation**

This timing mode uses an internal serial clock to shift out the conversion result and a CS signal to monitor and control the state of the conversion cycle, see Figure 8.

In order to select the internal serial clock timing mode, the serial clock pin (SCK) must be floating (Hi-Z) or pulled HIGH prior to the falling edge of CS. The device will not enter the internal serial clock mode if SCK is driven LOW on the falling edge of CS. An internal weak pull-up resis-
APPLICATIONS INFORMATION

The serial data output pin (SDO) is Hi-Z as long as \( \overline{CS} \) is HIGH. At any time during the conversion cycle, \( \overline{CS} \) may be pulled LOW in order to monitor the state of the converter. Once \( \overline{CS} \) is pulled LOW, SCK goes LOW and EOC is output to the SDO pin. EOC = 1 while a conversion is in progress and EOC = 0 if the device is in the sleep state.

When testing EOC, if the conversion is complete (EOC = 0), the device will exit the sleep state and enter the data output state if \( \overline{CS} \) remains LOW. In order to prevent the device from exiting the low power sleep state, \( \overline{CS} \) must be pulled HIGH before the first rising edge of SCK. In the internal SCK timing mode, SCK goes HIGH and the device begins outputting data at time \( t_{EOC\text{test}} \) after the falling edge of CS (if EOC = 0) or \( t_{EOC\text{test}} \) after EOC goes LOW (if \( \overline{CS} \) is LOW during the falling edge of EOC). The value of \( t_{EOC\text{test}} \) is 23µs if the device is using its internal oscillator (\( F_0 = \text{logic LOW or HIGH} \)). If \( F_0 \) is driven by an external oscillator of frequency \( f_{EOSC} \), then \( t_{EOC\text{test}} \) is \( 3.6/f_{EOSC} \). If \( \overline{CS} \) is pulled HIGH before time \( t_{EOC\text{test}} \), the device remains in the sleep state. The conversion result is held in the internal static shift register.

If \( \overline{CS} \) remains LOW longer than \( t_{EOC\text{test}} \), the first rising edge of SCK will occur and the conversion result is serially shifted out of the SDO pin. The data output cycle begins on this first rising edge of SCK and concludes after the 32nd rising edge. Data is shifted out the SDO pin on each falling edge of SCK. The internally generated serial clock is output to the SCK pin. This signal may be used to shift the conversion result into external circuitry. EOC can be latched on the first rising edge of SCK and the last bit of the conversion result on the 32nd rising edge of SCK. After the 32nd rising edge, SDO goes HIGH (EOC = 1), SCK stays HIGH and a new conversion starts.

Typically, \( \overline{CS} \) remains LOW during the data output state. However, the data output state may be aborted by pulling \( \overline{CS} \) HIGH anytime between the first and 32nd rising edge of SCK, see Figure 9. On the rising edge of \( \overline{CS} \), the device aborts the data output state and immediately initiates a new conversion. This is useful for systems not requiring all 32 bits of output data, aborting an invalid conversion cycle, or synchronizing the start of a conversion. If \( \overline{CS} \) is
pulled HIGH while the converter is driving SCK LOW, the internal pull-up is not available to restore SCK to a logic HIGH state. This will cause the device to exit the internal serial clock mode on the next falling edge of CS. This can be avoided by adding an external 10k pull-up resistor to the SCK pin or by never pulling CS HIGH when SCK is LOW.

Whenever SCK is LOW, the LTC2410’s internal pull-up at pin SCK is disabled. Normally, SCK is not externally driven if the device is in the internal SCK timing mode. However, certain applications may require an external driver on SCK. If this driver goes Hi-Z after outputting a LOW signal, the LTC2410’s internal pull-up remains disabled. Hence, SCK remains LOW. On the next falling edge of CS, the device is switched to the external SCK timing mode. By adding an external 10k pull-up resistor to SCK, this pin goes HIGH once the external driver goes Hi-Z. On the next CS falling edge, the device will remain in the internal SCK timing mode.

A similar situation may occur during the sleep state when CS is pulsed HIGH-LOW-HIGH in order to test the conversion status. If the device is in the sleep state (EOC = 0), SCK will go LOW. Once CS goes HIGH (within the time period defined above as tEOCtest), the internal pull-up is activated. For a heavy capacitive load on the SCK pin, the internal pull-up may not be adequate to return SCK to a HIGH level before CS goes low again. This is not a concern under normal conditions where CS remains LOW after detecting EOC = 0. This situation is easily overcome by adding an external 10k pull-up resistor to the SCK pin.

**Internal Serial Clock, 2-Wire I/O, Continuous Conversion**

This timing mode uses a 2-wire, all output (SCK and SDO) interface. The conversion result is shifted out of the device by an internally generated serial clock (SCK) signal, see Figure 10. CS may be permanently tied to ground, simplifying the user interface or isolation barrier.

The internal serial clock mode is selected at the end of the power-on reset (POR) cycle. The POR cycle is concluded approximately 0.5ms after VCC exceeds 2.2V. An internal weak pull-up is active during the POR cycle; therefore, the internal serial clock timing mode is automatically selected if SCK is not externally driven LOW (if SCK is loaded such that the internal pull-up cannot pull the pin HIGH, the external SCK mode will be selected).

During the conversion, the SCK and the serial data output pin (SDO) are HIGH (EOC = 1). Once the conversion is complete, SCK and SDO go LOW (EOC = 0) indicating the...
APPLICATIONS INFORMATION

Conversion has finished and the device has entered the low power sleep state. The part remains in the sleep state a minimum amount of time (1/2 the internal SCK period) then immediately begins outputting data. The data output cycle begins on the first rising edge of SCK and ends after the 32nd rising edge. Data is shifted out the SDO pin on each falling edge of SCK. The internally generated serial clock is output to the SCK pin. This signal may be used to shift the conversion result into external circuitry. EOC can be latched on the first rising edge of SCK and the last bit of the conversion result can be latched on the 32nd rising edge of SCK. After the 32nd rising edge, SDO goes HIGH (EOC = 1) indicating a new conversion is in progress. SCK remains HIGH during the conversion.

Internal Serial Clock, Autostart Conversion

This timing mode is identical to the internal serial clock, 2-wire I/O described above with one additional feature. Instead of grounding CS, an external timing capacitor is tied to CS.

While the conversion is in progress, the CS pin is held HIGH by an internal weak pull-up. Once the conversion is complete, the device enters the low power sleep state and an internal 25nA current source begins discharging the capacitor tied to CS, see Figure 11. The time the converter spends in the sleep state is determined by the value of the external timing capacitor, see Figures 12 and 13. Once the voltage at CS falls below an internal threshold (≈1.4V), the device automatically begins outputting data. The data output cycle begins on the first rising edge of SCK and ends on the 32nd rising edge. Data is shifted out the SDO pin on each falling edge of SCK. The internally generated serial clock is output to the SCK pin. This signal may be used to shift the conversion result into external circuitry. After the 32nd rising edge, CS is pulled HIGH and a new conversion is immediately started. This is useful in applications requiring periodic monitoring and ultralow power. Figure 14 shows the average supply current as a function of capacitance on CS.
APPLICATIONS INFORMATION

It should be noticed that the external capacitor discharge current is kept very small in order to decrease the converter power dissipation in the sleep state. In the autostart mode, the analog voltage on the CS pin cannot be observed without disturbing the converter operation using a regular oscilloscope probe. When using this configuration, it is important to minimize the external leakage current at the CS pin by using a low leakage external capacitor and properly cleaning the PCB surface.

The internal serial clock mode is selected every time the voltage on the CS pin crosses an internal threshold voltage. An internal weak pull-up at the SCK pin is active while CS is discharging; therefore, the internal serial clock timing mode is automatically selected if SCK is floating. It is important to ensure there are no external drivers pulling SCK LOW while CS is discharging.

PRESERVING THE CONVERTER ACCURACY

The LTC2410 is designed to reduce as much as possible the conversion result sensitivity to device decoupling, PCB layout, anti-aliasing circuits, line frequency perturbations and so on. Nevertheless, in order to preserve the extreme accuracy capability of this part, some simple precautions are desirable.

Digital Signal Levels

The LTC2410’s digital interface is easy to use. Its digital inputs (FO, CS and SCK in External SCK mode of operation) accept standard TTL/CMOS logic levels and the internal hysteresis receivers can tolerate edge rates as slow as 100µs. However, some considerations are required to take advantage of the exceptional accuracy and low supply current of this converter.

The digital output signals (SDO and SCK in Internal SCK mode of operation) are less of a concern because they are not generally active during the conversion state.

While a digital input signal is in the range 0.5V to (VCC – 0.5V), the CMOS input receiver draws additional current from the power supply. It should be noted that, when any one of the digital input signals (FO, CS and SCK in External SCK mode of operation) is within this range, the LTC2410 power supply current may increase even if
APPLICATIONS INFORMATION

the signal in question is at a valid logic level. For micro-
power operation, it is recommended to drive all digital
input signals to full CMOS levels \(V_{IL} < 0.4V\) and \(V_{OH} > (V_{CC} – 0.4V)\).

During the conversion period, the undershoot and/or
overshoot of a fast digital signal connected to the LTC2410
pins may severely disturb the analog to digital conversion
process. Undershoot and overshoot can occur because of
the impedance mismatch at the converter pin when the
transition time of an external control signal is less than
twice the propagation delay from the driver to LTC2410.
For reference, on a regular FR-4 board, signal propagation
velocity is approximately 183ps/inch for internal traces and
170ps/inch for surface traces. Thus, a driver generating a
control signal with a minimum transition time of 1ns must
be connected to the converter pin through a trace shorter
than 2.5 inches. This problem becomes particularly difficult
when shared control lines are used and multiple reflections
may occur. The solution is to carefully terminate all
transmission lines close to their characteristic impedance.

Parallel termination near the LTC2410 pin will eliminate
this problem but will increase the driver power dissipation.
A series resistor between 27Ω and 56Ω placed near
the driver or near the LTC2410 pin will also eliminate this
problem without additional power dissipation. The actual
resistor value depends upon the trace impedance and
connection topology.

An alternate solution is to reduce the edge rate of the
control signals. It should be noted that using very slow
edges will increase the converter power supply current
during the transition time. The multiple ground pins used
in this package configuration, as well as the differential
input and reference architecture, reduce substantially the
converter’s sensitivity to ground currents.

Particular attention must be given to the connection of
the \(F_O\) signal when the LTC2410 is used with an external
conversion clock. This clock is active during the conver-
sion time and the normal mode rejection provided by the
internal digital filter is not very high at this frequency. A
normal mode signal of this frequency at the converter
reference terminals may result into DC gain and INL errors.
A normal mode signal of this frequency at the converter
input terminals may result into a DC offset error. Such
perturbations may occur due to asymmetric capacitive
coupling between the \(F_O\) signal trace and the converter
input and/or reference connection traces. An immediate
solution is to maintain maximum possible separation be-
tween the \(F_O\) signal trace and the input/reference signals.
When the \(F_O\) signal is parallel terminated near the converter,
substantial AC current is flowing in the loop formed by
the \(F_O\) connection trace, the termination and the ground
return path. Thus, perturbation signals may be inductively
coupled into the converter input and/or reference. In this
situation, the user must reduce to a minimum the loop
area for the \(F_O\) signal as well as the loop area for the dif-
ferential input and reference connections.

Driving the Input and Reference

The input and reference pins of the LTC2410 converter
are directly connected to a network of sampling capaci-
tors. Depending upon the relation between the differential
input voltage and the differential reference voltage, these
capacitors are switching between these four pins transferr-
ing small amounts of charge in the process. A simplified
equivalent circuit is shown in Figure 15.

For a simple approximation, the source impedance \(R_S\)
driving an analog input pin \((IN^+, IN^-, REF^+ or REF^-)\) can
be considered to form, together with \(R_{SW}\) and \(C_{EQ}\) (see
Figure 15), a first order passive network with a time
constant \(\tau = (R_S + R_{SW}) \cdot C_{EQ}\). The converter is able to
sample the input signal with better than 1ppm accuracy if
the sampling period is at least 14 times greater than the
input circuit time constant \(\tau\). The sampling process on
the four input analog pins is quasi-independent so each
time constant should be considered by itself and, under
worst-case circumstances, the errors may add.

When using the internal oscillator \((F_O = LOW or HIGH)\),
the LTC2410’s front-end switched-capacitor network is
clocked at 76800Hz corresponding to a 13µs sampling
period. Thus, for settling errors of less than 1ppm, the
driving source impedance should be chosen such that \(\tau \leq
13\mu s/14 = 920\)ns. When an external oscillator of frequency
\(f_{EOSC}\) is used, the sampling period is \(2/f_{EOSC}\) and, for a
settling error of less than 1ppm, \(\tau \leq 0.14/f_{EOSC}\).
APPLICATIONS INFORMATION

Input Current

If complete settling occurs on the input, conversion results will be unaffected by the dynamic input current. An incomplete settling of the input signal sampling process may result in gain and offset errors, but it will not degrade the INL performance of the converter. Figure 15 shows the mathematical expressions for the average bias currents flowing through the IN+ and IN− pins as a result of the sampling charge transfers when integrated over a substantial time period (longer than 64 internal clock cycles).

The effect of this input dynamic current can be analyzed using the test circuit of Figure 16. The CPAR capacitor includes the LTC2410 pin capacitance (5pF typical) plus the capacitance of the test fixture used to obtain the results shown in Figures 17 and 18. A careful implementation can bring the total input capacitance (CIN + CPAR) closer to 5pF thus achieving better performance than the one predicted by Figures 17 and 18. For simplicity, two distinct situations can be considered.

For relatively small values of input capacitance (CIN < 0.01µF), the voltage on the sampling capacitor settles almost completely and relatively large values for the source impedance result in only small errors. Such values for CIN

\[
\begin{align*}
I_{IN+}(AVG) &= \frac{V_{IN+} + V_{INCM} - V_{REFCM}}{0.5 \times R_{EO}} \\
I_{IN-}(AVG) &= -\frac{V_{IN-} + V_{INCM} - V_{REFCM}}{0.5 \times R_{EO}} \\
I_{REF+}(AVG) &= \frac{1.5 \times (V_{REF} - V_{REFCM}) - V_{IN+}}{0.5 \times R_{EO}} \\
I_{REF-}(AVG) &= -\frac{1.5 \times (V_{REF} - V_{REFCM}) + V_{IN-}}{0.5 \times R_{EO}} \\
\end{align*}
\]

where:

\[
V_{REF} = REF^+ - REF^- \\
V_{REFCM} = \frac{REF^+ + REF^-}{2} \\
V_{IN} = IN^+ - IN^- \\
V_{INCM} = \frac{IN^+ - IN^-}{2} \\
R_{EO} = 3.6\,\text{MO} \quad \text{INTERNAL OSCILLATOR 60Hz Notch (FD = LOW)} \\
R_{EO} = 4.32\,\text{MO} \quad \text{INTERNAL OSCILLATOR 50Hz Notch (FD = HIGH)} \\
R_{EO} = (0.555 \times 10^{12}) / f_{EOSC} \quad \text{EXTERNAL OSCILLATOR}
\]

For more information visit www.linear.com/LTC2410
will deteriorate the converter offset and gain performance without significant benefits of signal filtering and the user is advised to avoid them. Nevertheless, when small values of $C_{IN}$ are unavoidably present as parasitics of input multiplexers, wires, connectors or sensors, the LTC2410 can maintain its exceptional accuracy while operating with relative large values of source resistance as shown in Figures 17 and 18. These measured results may be slightly different from the first order approximation suggested earlier because they include the effect of the actual second order input network together with the nonlinear settling process of the input amplifiers. For small $C_{IN}$ values, the settling on $IN^+$ and $IN^-$ occurs almost independently and there is little benefit in trying to match the source impedance for the two pins.

Larger values of input capacitors ($C_{IN} > 0.01\mu F$) may be required in certain configurations for anti-aliasing or general input signal filtering. Such capacitors will average the input sampling charge and the external source resistance will see a quasi constant input differential impedance. When $F_O$ = LOW (internal oscillator and 60Hz notch), the typical differential input resistance is $1.8M\Omega$ which will generate a gain error of approximately 0.28ppm for each ohm of source resistance driving $IN^+$ or $IN^-$. When $F_O$ = HIGH (internal oscillator and 50Hz notch), the typical differential input resistance is $2.16M\Omega$ which will generate a gain error of approximately 0.23ppm for each ohm of source resistance driving $IN^+$ or $IN^-$. When $F_O$ is driven by an external oscillator with a frequency $f_{EOSC}$, every $1\Omega$ mismatch in source impedance transforms a full-scale common mode input signal into a differential mode input signal of $0.28ppm$. When $F_O$ = HIGH (internal oscillator and 50Hz notch), every $1\Omega$ mismatch in source impedance transforms a full-scale common mode input signal into a differential mode input signal of $0.23ppm$. When $F_O$ is driven by an external oscillator with a frequency $f_{EOSC}$, every $1\Omega$ mismatch in source impedance transforms a full-scale common mode input signal into a differential mode input signal of $1.78 \times 10^{-6} \cdot f_{EOSC} ppm$. Figure 21 shows the typical offset error due to input common mode voltage for various values of source resistance imbalance between the $IN^+$ and $IN^-$ pins when large $C_{IN}$ values are used.

If possible, it is desirable to operate with the input signal common mode voltage very close to the reference signal common mode voltage as is the case in the ratiometric measurement of a symmetric bridge. This configuration eliminates the offset error caused by mismatched source impedances.

The magnitude of the dynamic input current depends upon the size of the very stable internal sampling capacitors and upon the accuracy of the converter sampling clock. The accuracy of the internal clock over the entire temperature range is $0.28 \times 10^{12} / f_{EOSC} \Omega$ and each ohm of source resistance driving $IN^+$ or $IN^-$ will result in $1.78 \times 10^{-6} \cdot f_{EOSC} ppm$ gain error. The effect of the source resistance on the two input pins is additive with respect to this gain error. The typical +FS and –FS errors as a function of the source resistance seen by $IN^+$ and $IN^-$ for large values of $C_{IN}$ are shown in Figures 19 and 20.

In addition to this gain error, an offset error term may also appear. The offset error is proportional with the mismatch between the source impedance driving the two input pins $IN^+$ and $IN^-$ and with the difference between the input and reference common mode voltages. While the input drive circuit nonzero source impedance combined with the converter average input current will not degrade the INL performance, indirect distortion may result from the modulation of the offset error by the common mode component of the input signal. Thus, when using large $C_{IN}$ capacitor values, it is advisable to carefully match the source impedance seen by the $IN^+$ and $IN^-$ pins. When $F_O$ = LOW (internal oscillator and 60Hz notch), every $1\Omega$ mismatch in source impedance transforms a full-scale common mode input signal into a differential mode input signal of $0.28ppm$. When $F_O$ = HIGH (internal oscillator and 50Hz notch), every $1\Omega$ mismatch in source impedance transforms a full-scale common mode input signal into a differential mode input signal of $0.23ppm$. When $F_O$ is driven by an external oscillator with a frequency $f_{EOSC}$, every $1\Omega$ mismatch in source impedance transforms a full-scale common mode input signal into a differential mode input signal of $1.78 \times 10^{-6} \cdot f_{EOSC} ppm$. Figure 21 shows the typical offset error due to input common mode voltage for various values of source resistance imbalance between the $IN^+$ and $IN^-$ pins when large $C_{IN}$ values are used.
APPLICATIONS INFORMATION

Figure 21. Offset Error vs Common Mode Voltage (VINCM = IN+ = IN–) and Input Source Resistance Imbalance (∆RIN = RSOURCEIN+ – RSOURCEIN–) for Large CIN Values (CIN ≥ 1µF)

For more information www.linear.com/LTC2410

and power supply range is typical better than 0.5%. Such a specification can also be easily achieved by an external clock. When relatively stable resistors (50ppm/°C) are used for the external source impedance seen by IN+ and IN–, the expected drift of the dynamic current, offset and gain errors will be insignificant (about 1% of their respective values over the entire temperature and voltage range). Even for the most stringent applications, a one-time calibration operation may be sufficient.

In addition to the input sampling charge, the input ESD protection diodes have a temperature dependent leakage current. This current, nominally 1nA (±10nA max), results in a small offset shift. A 100Ω source resistance will create a 0.1µV typical and 1µV maximum offset voltage.

Reference Current

In a similar fashion, the LTC2410 samples the differential reference pins REF+ and REF– transferring small amount of charge to and from the external driving circuits thus producing a dynamic reference current. This current does not change the converter offset, but it may degrade the gain and INL performance. The effect of this current can be analyzed in the same two distinct situations.

For relatively small values of the external reference capacitors (CREF < 0.01µF), the voltage on the sampling capacitor settles almost completely and relatively large values for the source impedance result in only small errors. Such values for CREF will deteriorate the converter offset and gain performance without significant benefits of reference filtering and the user is advised to avoid them.

Larger values of reference capacitors (CREF > 0.01µF) may be required as reference filters in certain configurations. Such capacitors will average the reference sampling charge and the external source resistance will see a quasi constant reference differential impedance. When FO = LOW (internal oscillator and 60Hz notch), the typical differential reference resistance is 1.3MΩ which will generate a gain error of approximately 0.38ppm for each ohm of source resistance driving REF+ or REF–. When FO = HIGH (internal oscillator and 50Hz notch), the typical differential reference resistance is 1.56MΩ which will generate a gain error of approximately 0.32ppm for each ohm of source resistance driving REF+ or REF–. When FO is driven by
an external oscillator with a frequency \( f_{EOSC} \) (external conversion clock operation), the typical differential reference resistance is \( 0.20 \times 10^{12}/f_{EOSC} \Omega \) and each ohm of source resistance driving \( \text{REF}^+ \) or \( \text{REF}^- \) will result in \( 2.47 \times 10^{-6} \times f_{EOSC} \) ppm gain error. The effect of the source resistance on the two reference pins is additive with respect to this gain error. The typical \( +\text{FS} \) and \( -\text{FS} \) errors for various combinations of source resistance seen by the \( \text{REF}^+ \) and \( \text{REF}^- \) pins and external capacitance \( C_{\text{REF}} \) connected to these pins are shown in Figures 22, 23, 24 and 25.

In addition to this gain error, the converter INL performance is degraded by the reference source impedance. When \( F_O = \text{LOW} \) (internal oscillator and 60Hz notch), every 100\( \Omega \) of source resistance driving \( \text{REF}^+ \) or \( \text{REF}^- \) translates into about 1.34ppm additional INL error. When \( F_O \) = HIGH (internal oscillator and 50Hz notch), every 100\( \Omega \) of source resistance driving \( \text{REF}^+ \) or \( \text{REF}^- \) translates into about 1.1ppm additional INL error. When \( F_O \) is driven by an external oscillator with a frequency \( f_{EOSC} \), every 100\( \Omega \) of source resistance driving \( \text{REF}^+ \) or \( \text{REF}^- \) translates into about 8.73 \( \times 10^{-6} \times f_{EOSC} \) ppm additional INL error. Figure 26 shows the typical INL error due to the source resistance driving the \( \text{REF}^+ \) or \( \text{REF}^- \) pins when large \( C_{\text{REF}} \) values are used. The effect of the source resistance on the two reference pins is additive with respect to this INL error. In general, matching of source impedance for the \( \text{REF}^+ \) and \( \text{REF}^- \) pins does not help the gain or the INL error. The user is thus advised to minimize the combined source impedance driving the \( \text{REF}^+ \) and \( \text{REF}^- \) pins rather than to try to match it.

![Figure 22. +FS Error vs R\text{SOURCE} at \text{REF}^+ or \text{REF}^- (Small C\text{IN})](image1)

![Figure 23. –FS Error vs R\text{SOURCE} at \text{REF}^+ or \text{REF}^- (Small C\text{IN})](image2)

![Figure 24. +FS Error vs R\text{SOURCE} at \text{REF}^+ or \text{REF}^- (Large C\text{REF})](image3)

![Figure 25. –FS Error vs R\text{SOURCE} at \text{REF}^+ or \text{REF}^- (Large C\text{REF})](image4)
APPLICATIONS INFORMATION

Figure 26. INL vs Differential Input Voltage (VIN = IN+ = IN–) and Reference Source Resistance (RSOURCE at REF+ and REF–) for Large CREF Values (CREF ≥ 1µF)

The magnitude of the dynamic reference current depends upon the size of the very stable internal sampling capacitors and upon the accuracy of the converter sampling clock. The accuracy of the internal clock over the entire temperature and power supply range is typical better than 0.5%. Such a specification can also be easily achieved by an external clock. When relatively stable resistors (50ppm/°C) are used for the external source impedance seen by REF+ and REF–, the expected drift of the dynamic current gain error will be insignificant (about 1% of its value over the entire temperature and voltage range). Even for the most stringent applications a one-time calibration operation may be sufficient.

In addition to the reference sampling charge, the reference pins ESD protection diodes have a temperature dependent leakage current. This leakage current, nominally 1nA (±10nA max), results in a small gain error. A 100Ω source resistance will create a 0.05µV typical and 0.5µV maximum full-scale error.

Output Data Rate

When using its internal oscillator, the LTC2410 can produce up to 7.5 readings per second with a notch frequency of 60Hz (FO = LOW) and 6.25 readings per second with a notch frequency of 50Hz (FO = HIGH). The actual output data rate will depend upon the length of the sleep and data output phases which are controlled by the user and which can be made insignificantly short. When operated with an external conversion clock (FO connected to an external oscillator), the LTC2410 output data rate can be increased as desired. The duration of the conversion phase is 20510/fEOSC. If fEOSC = 153600Hz, the converter behaves as if the internal oscillator is used and the notch is set at 60Hz. There is no significant difference in the LTC2410 performance between these two operation modes.

An increase in fEOSC over the nominal 153600Hz will translate into a proportional increase in the maximum output data rate. This substantial advantage is nevertheless accompanied by three potential effects, which must be carefully considered.

First, a change in fEOSC will result in a proportional change in the internal notch position and in a reduction of the converter differential mode rejection at the power line frequency. In many applications, the subsequent performance degradation can be substantially reduced by relying upon the LTC2410’s exceptional common mode rejection and by carefully eliminating common mode to differential mode conversion sources in the input circuit. The user should avoid single-ended input filters and should maintain a very high degree of matching and symmetry in the circuits driving the IN+ and IN– pins.

Second, the increase in clock frequency will increase proportionally the amount of sampling charge transferred through the input and the reference pins. If large external input and/or reference capacitors (CIN, CREF) are used, the previous section provides formulae for evaluating the effect of the source resistance upon the converter performance for any value of fEOSC. If small external input and/or reference capacitors (CIN, CREF) are used, the effect of the external source resistance upon the LTC2410 typical performance can be inferred from Figures 17, 18, 22 and 23 in which the horizontal axis is scaled by 153600/fEOSC.

Third, an increase in the frequency of the external oscillator above 460800Hz (a more than 3× increase in the output data rate) will start to decrease the effectiveness of the internal auto-calibration circuits. This will result in a progressive degradation in the converter accuracy and linearity. Typical measured performance curves for output data rates up to 25 readings per second are shown in Figures 27, 28, 29,
APPLICATIONS INFORMATION

30, 31, 32, 33 and 34. In order to obtain the highest possible level of accuracy from this converter at output data rates above 7.5 readings per second, the user is advised to maximize the power supply voltage used and to limit the maximum ambient operating temperature. In certain circumstances, a reduction of the differential reference voltage may be beneficial.

Input Bandwidth

The combined effect of the internal Sinc⁴ digital filter and of the analog and digital autocalibration circuits determines the LTC2410 input bandwidth. When the internal oscillator is used with the notch set at 60Hz (F₀ = LOW), the 3dB input bandwidth is 3.63Hz. When the internal oscillator is used with the notch set at 50Hz (F₀ = HIGH), the 3dB input bandwidth is 3.02Hz. If an external conversion clock generator of frequency fEOSC is connected to the F₀ pin, the 3dB input bandwidth is 0.236 • 10⁻⁶ • fEOSC.

Due to the complex filtering and calibration algorithms utilized, the converter input bandwidth is not modeled very accurately by a first order filter with the pole located at the 3dB frequency. When the internal oscillator is used, the shape of the LTC2410 input bandwidth is shown in Figure 35 for F₀ = LOW and F₀ = HIGH. When an external oscillator of frequency fEOSC is used, the shape of the LTC2410 input bandwidth can be derived from Figure 35, F₀ = LOW curve in which the horizontal axis is scaled by fEOSC/153600.

The conversion noise (800nVRMS typical for VREF = 5V) can be modeled by a white noise source connected to a noise free converter. The noise spectral density is 62.75nV√Hz for an infinite bandwidth source and 86.1nV√Hz for a single 0.5MHz pole source. From these numbers, it is clear that particular attention must be given to the design of external amplification circuits. Such circuits face the simultaneous requirements of very low bandwidth (just a few Hz) in order to reduce the output referred noise and relatively high bandwidth (at least 500kHz) necessary to drive the input switched-capacitor network. A possible solution is a high gain, low bandwidth amplifier stage followed by a high bandwidth unity-gain buffer.

When external amplifiers are driving the LTC2410, the ADC input referred system noise calculation can be
APPLICATIONS INFORMATION

Figure 30. Resolution (NoiseRMS ≤ 1LSB) vs Output Data Rate and Temperature

Figure 31. Resolution (INLRMS ≤ 1LSB) vs Output Data Rate and Temperature

Figure 32. Offset Error vs Output Data Rate and Reference Voltage

Figure 33. Resolution (INLMAX ≤ 1LSB) vs Output Data Rate and Reference Voltage

Figure 34. Resolution (INLMAX ≤ 1LSB) vs Output Data Rate and Reference Voltage

Figure 35. Input Signal Bandwidth Using the Internal Oscillator
APPLICATIONS INFORMATION

simplified by Figure 36. The noise of an amplifier driving the LTC2410 input pin can be modeled as a band limited white noise source. Its bandwidth can be approximated by the bandwidth of a single pole lowpass filter with a corner frequency $f_i$. The amplifier noise spectral density is $n_i$. From Figure 36, using $f_i$ as the x-axis selector, we can find on the y-axis the noise equivalent bandwidth $\text{freq}_i$ of the input driving amplifier. This bandwidth includes the band limiting effects of the ADC internal calibration and filtering. The noise of the driving amplifier referred to the converter input and including all these effects can be calculated as $N = n_i \cdot \sqrt{\text{freq}_i}$. The total system noise (referred to the LTC2410 input) can now be obtained by summing as square root of sum of squares the three ADC input referred noise sources: the LTC2410 internal noise (800nV), the noise of the IN+ driving amplifier and the noise of the IN– driving amplifier.

If the $F_O$ pin is driven by an external oscillator of frequency $f_{EOSC}$, Figure 36 can still be used for noise calculation if the x-axis is scaled by $f_{EOSC}/153600$. For large values of the ratio $f_{EOSC}/153600$, the Figure 36 plot accuracy begins to decrease, but in the same time the LTC2410 noise floor rises and the noise contribution of the driving amplifiers lose significance.

Normal Mode Rejection and Anti-aliasing

One of the advantages delta-sigma ADCs offer over conventional ADCs is on-chip digital filtering. Combined with a large oversampling ratio, the LTC2410 significantly simplifies anti-aliasing filter requirements.

The Sinc⁴ digital filter provides greater than 120dB normal mode rejection at all frequencies except DC and integer multiples of the modulator sampling frequency ($f_S$). The LTC2410’s auto-calibration circuits further simplify the anti-aliasing requirements by additional normal mode signal filtering both in the analog and digital domain. Independent of the operating mode, $f_S = 256 \times f_N = 2048 \times f_{\text{OUTMAX}}$ where $f_N$ in the notch frequency and $f_{\text{OUTMAX}}$ is the maximum output data rate. In the internal oscillator mode with a 50Hz notch setting, $f_S = 12800Hz$ and with a 60Hz notch setting $f_S = 15360Hz$. In the external oscillator mode, $f_S = f_{EOSC}/10$. 
APPLICATIONS INFORMATION

The combined normal mode rejection performance is shown in Figure 37 for the internal oscillator with 50Hz notch setting (F₀ = HIGH) and in Figure 38 for the internal oscillator with 60Hz notch setting (F₀ = LOW) and for the external oscillator mode. The regions of low rejection occurring at integer multiples of fₛ have a very narrow bandwidth. Magnified details of the normal mode rejection curves are shown in Figure 39 (rejection near DC) and Figure 40 (rejection at fₛ = 256fₜ) where fₜ represents the notch frequency. These curves have been derived for the external oscillator mode but they can be used in all operating modes by appropriately selecting the fₜ value.

The user can expect to achieve in practice this level of performance using the internal oscillator as it is demonstrated by Figures 41 and 42. Typical measured values of the normal mode rejection of the LTC2410 operating with an internal oscillator and a 60Hz notch setting are shown in Figure 41 superimposed over the theoretical calculated curve. Similarly, typical measured values of the normal mode rejection of the LTC2410 operating with an internal oscillator and a 50Hz notch setting are shown in Figure 42 superimposed over the theoretical calculated curve.

As a result of these remarkable normal mode specifications, minimal (if any) anti-alias filtering is required in front of the LTC2410. If passive RC components are placed in front of the LTC2410, the input dynamic current should be considered (see Input Current section). In cases where large effective RC time constants are used, an external buffer amplifier may be required to minimize the effects of dynamic input current.

For more information www.linear.com/LTC2410
APPLICATIONS INFORMATION

Traditional high order delta-sigma modulators, while providing very good linearity and resolution, suffer from potential instabilities at large input signal levels. The proprietary architecture used for the LTC2410 third order modulator resolves this problem and guarantees a predictable stable behavior at input signal levels of up to 150% of full scale. In many industrial applications, it is not uncommon to have to measure microvolt level signals superimposed over volt level perturbations and LTC2410 is eminently suited for such tasks. When the perturbation is differential, the specification of interest is the normal mode rejection for large input signal levels. With a reference voltage $V_{REF} = 5V$, the LTC2410 has a full-scale differential input range of 5V peak-to-peak. Figures 43 and 44 show measurement results for the LTC2410 normal mode rejection ratio with a 7.5V peak-to-peak (150% of full scale) input signal superimposed over the more traditional normal mode rejection ratio results obtained with a 5V peak-to-peak (full scale) input signal. In Figure 43, the LTC2410 uses the internal oscillator with the notch set at 60Hz ($F_O = LOW$) and in Figure 44 it uses the internal oscillator with the notch set at 50Hz ($F_O = HIGH$). It is clear that the LTC2410 rejection performance is maintained with no compromises in this extreme situation. When operating with large input signal levels, the user must observe that such signals do not violate the device absolute maximum ratings.

SYNCHRONIZATION OF MULTIPLE LTC2410S

Since the LTC2410’s absolute accuracy (total unadjusted error) is 5ppm, applications utilizing multiple synchronized ADCs are possible.
Simultaneous Sampling with Two LTC2410s

One such application is synchronizing multiple LTC2410s, see Figure 45. The start of conversion is synchronized to the rising edge of CS. In order to synchronize multiple LTC2410s, CS is a common input to all the ADCs. To prevent the converters from autostarting a new conversion at the end of data output read, 31 or fewer SCK clock signals are applied to the LTC2410 instead of 32 (the 32nd falling edge would start a conversion). The exact timing and frequency for the SCK signal is not critical since it is only shifting out the data. In this case, two LTC2410’s simultaneously start and end their conversion cycles under the external control of CS.

Increasing the Output Rate Using Multiple LTC2410s

A second application uses multiple LTC2410s to increase the effective output rate by 4×, see Figure 46. In this case, four LTC2410s are interleaved under the control of separate CS signals. This increases the effective output rate from 7.5Hz to 30Hz (up to a maximum of 60Hz). Additionally, the one-shot output spectrum is unfolded allowing further digital signal processing of the conversion results. SCK and SDO may be common to all four LTC2410s. The four CS rising edges equally divide one LTC2410 conversion cycle (7.5Hz for 60Hz notch frequency). In order to synchronize the start of conversion to CS, 31 or less SCK clock pulses must be applied to each ADC.

Both the synchronous and 4× output rate applications use the external serial clock and single cycle operation with reduced data output length (see Serial Interface Timing Modes section and Figure 6). An external oscillator clock is applied commonly to the FO pin of each LTC2410 in order to synchronize the sampling times. Both circuits may be extended to include more LTC2410s.

![Figure 45. Synchronous Conversion—Extendable](image-url)
BRIDGE APPLICATIONS

Typical strain gauge based bridges deliver only 2mV/Volt of excitation. As the maximum reference voltage of the LTC2410 is 5V, remote sensing of applied excitation without additional circuitry requires that excitation be limited to 5V. This gives only 10mV full scale input signal, which can be resolved to 1 part in 10000 without averaging. For many solid state sensors, this is still better than the sensor. Averaging 64 samples however reduces the noise level by a factor of eight, bringing the resolving power to 1 part in 80000, comparable to better weighing systems. Hysteresis and creep effects in the load cells are typically much greater than this. Most applications that require strain measurements to this level of accuracy are measuring slowly changing phenomena, hence the time required to average a large number of readings is usually not an issue. For those systems that require accurate measurement of a small incremental change on a significant tare weight, the lack of history effects in the LTC2400 family is of great benefit.

For those applications that cannot be fulfilled by the LTC2410 alone, compensating for error in external amplification can be done effectively due to the “no latency” feature of the LTC2410. No latency operation allows samples of the amplifier offset and gain to be interleaved with weighing measurements. The use of correlated double sampling allows suppression of 1/f noise, offset and thermocouple effects within the bridge. Correlated double sampling involves alternating the polarity of excitation and dealing with the reversal of input polarity mathematically. Alternatively, bridge excitation can be increased to as much as ±10V,
APPLICATIONS INFORMATION

if one of several precision attenuation techniques is used to produce a precision divide operation on the reference signal. Another option is the use of a reference within the 5V input range of the LTC2410 and developing excitation via fixed gain, or LTC1043 based voltage multiplication, along with remote feedback in the excitation amplifiers, as shown in Figures 52 and 53.

Figure 47 shows an example of a simple bridge connection. Note that it is suitable for any bridge application where measurement speed is not of the utmost importance. For many applications where large vessels are weighed, the average weight over an extended period of time is of concern and short term weight is not readily determined due to movement of contents, or mechanical resonance. Often, large weighing applications involve load cells located at each load bearing point, the output of which can be summed passively prior to the signal processing circuitry, actively with amplification prior to the ADC, or can be digitized via multiple ADC channels and summed mathematically. The mathematical summation of the output of multiple LTC2410’s provides the benefit of a root square reduction in noise. The low power consumption of the LTC2410 makes it attractive for multidrop communication schemes where the ADC is located within the load-cell housing.

A direct connection to a load cell is perhaps best incorporated into the load-cell body, as minimizing the distance to the sensor largely eliminates the need for protection devices, RFI suppression and wiring. The LTC2410 exhibits extremely low temperature dependent drift. As a result, exposure to external ambient temperature ranges does not compromise performance. The incorporation of any amplification considerably complicates thermal stability, as input offset voltages and currents, temperature coefficient of gain settling resistors all become factors.

The circuit in Figure 48 shows an example of a simple amplification scheme. This example produces a differential output with a common mode voltage of 2.5V, as determined by the bridge. The use of a true three amplifier instrumentation amplifier is not necessary, as the LTC2410 has common mode rejection far beyond that of most amplifiers. The LTC1051 is a dual autozero amplifier that can be used to produce a gain of 15 before its input referred noise dominates the LTC2410 noise. This example shows a gain of 34, that is determined by a feedback network built using a resistor array containing 8 individual resistors. The resistors are organized to optimize temperature tracking in the presence of thermal gradients. The second LTC1051 buffers the low noise input stage from the transient load steps produced during conversion.

The gain stability and accuracy of this approach is very good, due to a statistical improvement in resistor matching. A gain of 34 may seem low, when compared to common practice in earlier generations of load-cell interfaces, however the accuracy of the LTC2410 changes the rationale. Achieving high gain accuracy and linearity at higher gains may prove difficult, while providing little benefit in terms of noise reduction.

At a gain of 100, the gain error that could result from typical open-loop gain of 160dB is –1ppm, however, worst-case is at the minimum gain of 116dB, giving a gain error of –158ppm. Worst-case gain error at a gain of 34, is –54ppm. The use of the LTC1051A reduces the worst-case gain error to –33ppm. The advantage of gain higher than 34, then becomes dubious, as the input referred noise sees little improvement1 and gain accuracy is potentially compromised.

Note that this 4-amplifier topology has advantages over the typical integrated 3-amplifier instrumentation amplifier in that it does not have the high noise level common in the output stage that usually dominates when an instru-
APPLICATIONS INFORMATION

An instrumentation amplifier is used at low gain. If this amplifier is used at a gain of 10, the gain error is only 10 ppm and input referred noise is reduced to 0.1 µV RMS. The buffer stages can also be configured to provide gain of up to 50 with high gain stability and linearity.

Figure 49 shows an example of a single amplifier used to produce single-ended gain. This topology is best used in applications where the gain setting resistor can be made to match the temperature coefficient of the strain gauges. If the bridge is composed of precision resistors, with only one or two variable elements, the reference arm of the bridge can be made to act in conjunction with the feedback resistor to determine the gain. If the feedback resistor is incorporated into the design of the load cell, using resistors which match the temperature coefficient of the load-cell elements, good results can be achieved without the need for resistors with a high degree of absolute accuracy. The common mode voltage in this case, is again a function of the bridge output. Differential gain as used with a 350 Ω bridge is 

\[ A_V = \frac{R1 + R2}{R1 + 175 \Omega} \]

Figure 48. Using Autozero Amplifiers to Reduce Input Referred Noise

Remote Half Bridge Interface

As opposed to full bridge applications, typical half bridge applications must contend with nonlinearity in the bridge output, as signal swing is often much greater. Applications include RTD’s, thermistors and other resistive elements that undergo significant changes over their span. For single variable element bridges, the nonlinearity of the half bridge output can be eliminated completely; if the reference arm of the bridge is used as the reference to the ADC, as shown in Figure 50. The LTC2410 can accept inputs up to 1/2 V REF. Hence, the reference resistor R1 must be at least 2x the highest value of the variable resistor.

In the case of 100 Ω platinum RTD’s, this would suggest a value of 800 Ω for R1. Such a low value for R1 is not advisable due to self-heating effects. A value of 25.5 k is shown for R1, reducing self-heating effects to acceptable levels for most sensors.

The basic circuit shown in Figure 50 shows connections for a full 4-wire connection to the sensor, which may be located remotely. The differential input connections will reject induced or coupled 60 Hz interference, however, input referred noise for AV = 34 is approximately 0.05 µV RMS, whereas at a gain of 50, it would be 0.048 µV RMS.
the reference inputs do not have the same rejection. If 60Hz or other noise is present on the reference input, a low pass filter is recommended as shown in Figure 51. Note that you cannot place a large capacitor directly at the junction of R1 and R2, as it will store charge from the sampling process. A better approach is to produce a low pass filter decoupled from the input lines with a high value resistor (R3).

The use of a third resistor in the half bridge, between the variable and fixed elements gives essentially the same result as the two resistor version, but has a few benefits. If, for example, a 25k reference resistor is used to set the excitation current with a 100Ω RTD, the negative reference input is sampling the same external node as the positive input and may result in errors if used with a long cable. For short cable applications, the errors may be acceptable low. If instead the single 25k resistor is replaced with a 10k 5% and a 10k 0.1% reference resistor, the noise level introduced at the reference, at least at higher frequencies, will be reduced. A filter can be introduced into the network, in the form of one or more capacitors, or ferrite beads, as long as the sampling pulses are not translated into an error. The reference voltage is also reduced, but this is not undesirable, as it will decrease the value of the LSB, although, not the input referred noise level.

The circuit shown in Figure 51 shows a more rigorous example of Figure 50, with increased noise suppression and more protection for remote applications.

Figure 52 shows an example of gain in the excitation circuit and remote feedback from the bridge. The LTC1043’s provide voltage multiplication, providing ±10V from a 5V reference with only 1ppm error. The amplifiers are used at unity gain and introduce very little error due to gain error or due to offset voltages. A 1µV/°C offset voltage drift translates into 0.05ppm/°C gain error. Simpler alternatives, with the amplifiers providing gain using resistor arrays for feedback, can produce results that are similar to bridge sensing schemes via attenuators. Note that the amplifiers must have high open-loop gain or gain error will be a source of error. The fact that input offset voltage has relatively little effect on overall error may lead one to use low performance amplifiers for this application. Note that the gain of a device such as an LF156, (25V/mV over temperature) will produce a worst-case error of –180ppm at a noise gain of 3, such as would be encountered in an inverting gain of 2, to produce –10V from a 5V reference.

![Figure 49. Bridge Amplification Using a Single Amplifier](image_url)
The error associated with the 10V excitation would be –80ppm. Hence, overall reference error could be as high as 130ppm, the average of the two.

Figure 53 shows a similar scheme to provide excitation using resistor arrays to produce precise gain. The circuit is configured to provide 10V and –5V excitation to the bridge, producing a common mode voltage at the input to the LTC2410 of 2.5V, maximizing the AC input range for applications where induced 60Hz could reach amplitudes up to 2V_RMS.

The last two example circuits could be used where multiple bridge circuits are involved and bridge output can be multiplexed onto a single LTC2410, via an inexpensive multiplexer such as the 74HC4052.

Figure 54 shows the use of an LTC2410 with a differential multiplexer. This is an inexpensive multiplexer that will contribute some error due to leakage if used directly with the output from the bridge, or if resistors are inserted as a protection mechanism from overvoltage. Although the bridge output may be within the input range of the A/D and multiplexer in normal operation, some thought should be given to fault conditions that could result in full excitation voltage at the inputs to the multiplexer or ADC. The use of amplification prior to the multiplexer will largely eliminate errors associated with channel leakage developing error voltages in the source impedance.
Figure 52. LTC1043 Provides Precise 4x Reference for Excitation Voltages

*FLYING CAPACITORS ARE 1µF FILM (MKP OR EQUIVALENT)

SEE LTC1043 DATA SHEET FOR DETAILS ON UNUSED HALF OF U1
Figure 53. Use Resistor Arrays to Provide Precise Matching in Excitation Amplifier

Figure 54. Use a Differential Multiplexer to Expand Channel Capability
TYPICAL APPLICATIONS

Sample Driver for LTC2410 SPI Interface

The LTC2410 has a very simple serial interface that makes interfacing to microprocessors and microcontrollers very easy.

The listing in Figure 56 is a simple assembler routine for the 68HC11 microcontroller. It uses PORT D, configuring it for SPI data transfer between the controller and the LTC2410. Figure 55 shows the simple 3-wire SPI connection.

The code begins by declaring variables and allocating four memory locations to store the 32-bit conversion result. This is followed by initializing PORT D's SPI configuration. The program then enters the main sequence. It activates the LTC2410’s serial interface by setting the SS output low, sending a logic low to CS. It next waits in a loop for a logic low on the data line, signifying end-of-conversion. After the loop is satisfied, four SPI transfers are completed, retrieving the conversion. The main sequence ends by setting SS high. This places the LTC2410’s serial interface in a high impedance state and initiates another conversion.

The performance of the LTC2410 can be verified using the demonstration board DC291A, see Figure 57 for the schematic. This circuit uses the computer’s serial port to generate power and the SPI digital signals necessary for starting a conversion and reading the result. It includes a Labview application software program (see Figure 58) which graphically captures the conversion results. It can be used to determine noise performance, stability and with an external source, linearity. As exemplified in the schematic, the LTC2410 is extremely easy to use. This demonstration board and associated software is available by contacting Linear Technology.

Figure 55. Connecting the LTC2410 to a 68HC11 MCU Using the SPI Serial Interface
TYPICAL APPLICATIONS

* This example program transfers the LTC2410’s 32-bit output conversion result into four consecutive 8-bit memory locations.*

*68HC11 register definition

PORTD EQU $1008 Port D data register
* “–, –, SS*, CSK, MOSI, MISO, TxD, RxD”

DDRD EQU $1009 Port D data direction register

SPSR EQU $1028 SPI control register
* “SPIE, SPE, DWOM, MSTR; SPOL, CPHA, SPR1, SPR0”

SPSR EQU $1029 SPI status register
* “SPIF, WCOL, –, MODF; –, –, –, –”

SPDR EQU $102A SPI data register; Read-Buffer; Write-Shifter
* 

* RAM variables to hold the LTC2410’s 32 conversion result

DIN1 EQU $00 This memory location holds the LTC2410’s bits 31 - 24
DIN2 EQU $01 This memory location holds the LTC2410’s bits 23 - 16
DIN3 EQU $02 This memory location holds the LTC2410’s bits 15 - 08
DIN4 EQU $03 This memory location holds the LTC2410’s bits 07 - 00
*

***************************
* Start GETDATA Routine *
***************************

* ORG $C000 Program start location

INIT1 LDS #$CFFF Top of C page RAM, beginning location of stack
LDAA #$2F “–,–, Hi, SCK, Lo, MOSI, Hi, MISO, Hi, X, X
STAA PORTD Keeps SS* a logic high when DDRD, bit 5 is set
LDAA #$38 “–,–,1,1;1,0,0,0
STAA DDRD SS*, SCK, MOSI are configured as Outputs
* MISO, TxD, RxD are configured as Inputs

*DDRD’s bit 5 is a 1 so that port D’s SS* pin is a general output

LDAA #$50
STAA SPCR The SPI is configured as Master, CPHA = 0, CPOL = 0
* and the clock rate is E/2
* (This assumes an E-Clock frequency of 4MHz. For higher E-
* Clock frequencies, change the above value of $50 to a value
* that ensures the SCK frequency is 2MHz or less.)

GETDATA PSHX
PSHY
LDX #$0 The X register is used as a pointer to the memory locations
* that hold the conversion data
* 

LDY #$1000
BCLR PORTD, Y %0010000000 This sets the SS* output bit to a logic
* low, selecting the LTC2410
**TYPICAL APPLICATIONS**

* The next short loop waits for the  
* LTC2410's conversion to finish before  
* starting the SPI data transfer  

```
* CONVEND  
  LDAA PORTD  
  ANDA #%00000100  
  Retrieve the contents of port D  
  Look at bit 2  
  *  
  Bit 2 = Hi; the LTC2410's conversion is not  
  complete  
  *  
  Bit 2 = Lo; the LTC2410's conversion is complete  
  BNE CONVEND  
  Branch to the loop's beginning while bit 2 remains high  
```

* The SPI data transfer *

```
* TRFLP1  
  LDAA #$0  
  Load accumulator A with a null byte for SPI transfer  
  *  
  STAA SPDR  
  This writes the byte in the SPI data register and starts  
  the transfer  
  *  
  WAIT1  
  LDAA SPSR  
  This loop waits for the SPI to complete a serial  
  transfer/exchange by reading the SPI Status Register  
  *  
  BPL WAIT1  
  The SPIF (SPI transfer complete flag) bit is the SPSR's MSB  
  and is set to one at the end of an SPI transfer. The branch  
  will occur while SPIF is a zero.  
  *  
  LDAA SPDR  
  Load accumulator A with the current byte of LTC2410 data  
  that was just received  
  *  
  STAA 0,X  
  Transfer the LTC2410's data to memory  
  *  
  INX  
  Increment the pointer  
  *  
  CPX #DIN4+1  
  Has the last byte been transferred/exchanged?  
  *  
  BNE TRFLP1  
  If the last byte has not been reached, then proceed to the  
  next byte for transfer/exchange  
  BSET PORTD,Y %00100000  
  This sets the SS* output bit to a logic high,  
  de-selecting the LTC2410  
  PULA  
  Restore the A register  
  PULY  
  Restore the Y register  
  PULX  
  Restore the X register  
  RTS  
```

Figure 56. This is an Example of 68HC11 Code That Captures the LTC2410's Conversion Results Over the SPI Serial Interface Shown in Figure 55
TYPICAL APPLICATIONS

![Schematic Diagram]

Figure 57. 24-Bit A/D Demo Board Schematic

![Display Graphic]

Figure 58. Display Graphic

For more information www.linear.com/LTC2410
**PACKAGE DESCRIPTION**


---

**GN Package**

16-Lead Plastic SSOP (Narrow .150 Inch)

(Reference LTC DWG # 05-08-1641 Rev B)

---

**NOTE:**

1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING NOT TO SCALE
4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE
LTC2410

PCB LAYOUT AND FILM

LTC2410CGN
Differential Input 24 Bit ADC
Demo Circuit DC291A

www.linear-tech.com
LTC Confidential For Customer Use Only

Linear Technology
(408) 432-1900

Silkscreen Top

Top Layer

For more information www.linear.com/LTC2410
## REVISION HISTORY

<table>
<thead>
<tr>
<th>REV</th>
<th>DATE</th>
<th>DESCRIPTION</th>
<th>PAGE NUMBER</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>08/15</td>
<td>Updated $f_{EOSC}$ maximum to 500kHz and all associated information. Removed 52.5Hz noise histograms.</td>
<td>5, 9, 30, 31, 6, 7</td>
</tr>
</tbody>
</table>
## RELATED PARTS

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>LT1019</td>
<td>Precision Bandgap Reference, 2.5V, 5V</td>
<td>3ppm/°C Drift, 0.05% Max</td>
</tr>
<tr>
<td>LT1025</td>
<td>Micropower Thermocouple Cold Junction Compensator</td>
<td>80µA Supply Current, 0.5°C Initial Accuracy</td>
</tr>
<tr>
<td>LTC1043</td>
<td>Dual Precision Instrumentation Switched Capacitor Building Block</td>
<td>Precise Charge, Balanced Switching, Low Power</td>
</tr>
<tr>
<td>LTC1050</td>
<td>Precision Chopper Stabilized Op Amp</td>
<td>No External Components 5µV Offset, 1.6µVp-p Noise</td>
</tr>
<tr>
<td>LT1236A-5</td>
<td>Precision Bandgap Reference, 5V</td>
<td>0.05% Max, 5ppm/°C Drift</td>
</tr>
<tr>
<td>LT1460</td>
<td>Micropower Series Reference</td>
<td>0.075% Max, 10ppm/°C Max Drift, 2.5V, 5V and 10V Versions</td>
</tr>
<tr>
<td>LTC2400</td>
<td>24-Bit, No Latency ΔΣ ADC in SO-8</td>
<td>0.3ppm Noise, 4ppm INL, 10ppm Total Unadjusted Error, 200µA</td>
</tr>
<tr>
<td>LTC2401/LTC2402</td>
<td>1-/2-Channel, 24-Bit, No Latency ΔΣ ADC in MSOP</td>
<td>0.6ppm Noise, 4ppm INL, 10ppm Total Unadjusted Error, 200µA</td>
</tr>
<tr>
<td>LTC2404/LTC2408</td>
<td>4-/8-Channel, 24-Bit, No Latency ΔΣ ADC</td>
<td>0.3ppm Noise, 4ppm INL, 10ppm Total Unadjusted Error, 200µA</td>
</tr>
<tr>
<td>LTC2411</td>
<td>24-Bit, No Latency ΔΣ ADC in MSOP</td>
<td>1.45µVRMS Noise, 4ppm INL</td>
</tr>
<tr>
<td>LTC2413</td>
<td>24-Bit, No Latency ΔΣ ADC</td>
<td>Simultaneous 50Hz/60Hz Rejection, 800nVRMS Noise</td>
</tr>
<tr>
<td>LTC2420</td>
<td>20-Bit, No Latency ΔΣ ADC in SO-8</td>
<td>1.2ppm Noise, 8ppm INL, Pin Compatible with LTC2400</td>
</tr>
<tr>
<td>LTC2424/LTC2428</td>
<td>4-/8-Channel, 20-Bit, No Latency ΔΣ ADCs</td>
<td>1.2ppm Noise, 8ppm INL Pin Compatible with LTC2404/LTC2408</td>
</tr>
</tbody>
</table>