



DS2155

T1/E1/J1 Single-Chip Transceiver

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REVISION A3 ERRATA

The errata listed below describe situations where DS2155 revision A3 components perform differently than expected or differently than described in the data sheet. Dallas Semiconductor intends to fix these errata in subsequent die revisions.

This errata sheet only applies to DS2155 revision A3 components. Revision A3 components are branded on the top side of the package with a six-digit code of the form yywwA3, where yy and ww are two-digit numbers representing the year and work-week of manufacture, respectively. The die revision can also be determined through the lower four bits of the IDR register at location 0Fh. Revision A3 devices contain a B0h at location 0Fh. To obtain an errata sheet on another DS2155 die revision, visit the website at www.maxim-ic.com/errata.

1. RECEIVE PACKET BYTES AVAILABLE REGISTER

Description:

The HDLC receive bytes available in the H1RPBA and H2RPBA registers may not report the correct value.

Work Around:

Do not use the HxRPBA registers. Poll the EMPTY (in the INFO5 and INFO6 registers) bit after each byte is read from the receive FIFO until the bit indicates that there are no more bytes to be retrieved.

2. RECEIVE DIGITAL MILLIWATT (T1 MODE)

Description:

The receive digital-milliwatt enable channel-selection bits are scrambled in the T1RDMR1, T1RDMR2, and T1RDMR3 registers.

The data sheet shows the channel assignment as follows:

T1RDMR1	8	7	6	5	4	3	2	1
T1RDMR2	16	15	14	13	12	11	10	9
T1RDMR3	24	23	22	21	20	19	18	17

Work Around:

Use the channel assignment as implemented in the DS2155 revision A3:

T1RDMR1	14	6	23	15	7	24	16	8
T1RDMR2	3	20	12	4	21	13	5	22
T1RDMR3	17	9	1	18	10	2	19	11

3. TRANSMIT SA BIT SELECT (E1 MODE)

Description:

The 5 bits that control the Sa bits to be sourced from the TLINK pin are reversed from the order described in the data sheet for the E1TCR2 register.

E1TCR2 (Data Sheet)	Sa8S	Sa7S	Sa6S	Sa5S	Sa4S	AEBE	AAIS	ARA
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Work Around:

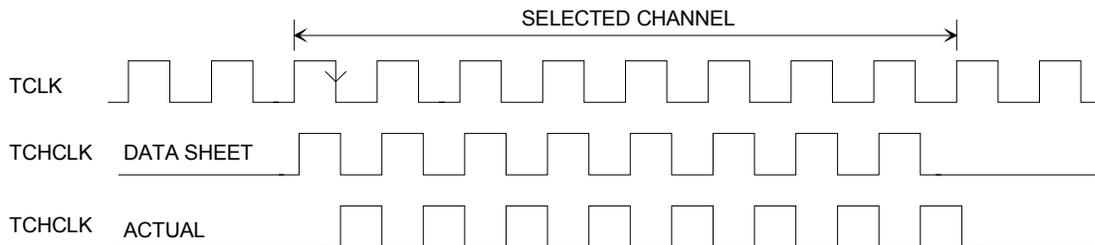
Use the Sa bit mappings as implemented in the DS2155 revision A3:

E1TCR2 A3 rev	Sa4S	Sa5S	Sa6S	Sa7S	Sa8S	AEBE	AAIS	ARA
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4. TRANSMIT FRACTIONAL SUPPORT

Description:

The transmit fractional support (alternate function of the TCHCLK pin) does not operate as described in the data sheet. Transmit data at the TSER pin is sampled on the falling edge of TCLK. In fractional support mode the TCHCLK pin should output a clock (gated version of TCLK) during a selected channel or channels. The rising edge of this clock could be used to present data to the TSER pin for sampling in the falling edge of TCLK. However, TCHCLK is delayed one-half clock in this rev of the DS2155. Its rising edge occurs AFTER the sampling time of the corresponding bit time of TCLK, as shown below.



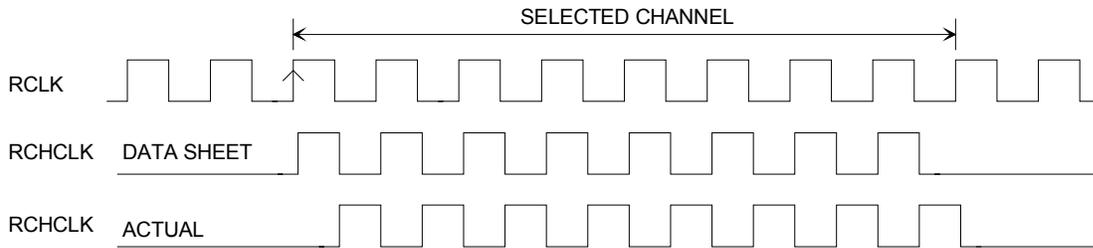
Work Around:

There is no known software work around for this issue.

5. RECEIVE FRACTIONAL SUPPORT

Description:

The receive fractional support (alternate function of the RCHCLK pin) does not operate as described in the data sheet. Receive data at the RSER pin is updated on the rising edge of RCLK. In fractional support mode the RCHCLK pin should output a clock (gated version of RCLK) during a selected channel or channels. The falling edge of this clock could be used by the backplane to sample data output on the RSER pin. However, RCHCLK is delayed one half clock in this rev of the DS2155.



Work Around:

As an alternate method, the backplane can use the rising edge RCHCLK to sample data output from RSER.

6. HDLC FIFO

Description:

HDLC FIFOs cannot be read from or written to at full bus speed. Writing at a speed $>4.7\text{MHz}$ can cause data corruption in the FIFOs.

Work Around:

Keep the HDLC read and write speed below 4.7MHz.

7. HDLC TIMING

Description:

While in framer loopback mode, received HDLC data can be corrupted when MCLK and TCLK rising edges are $<30\text{ns}$ apart. When not in framer loopback mode, data can be corrupted if the edges of RCLK and the internally generated 8XCLK occur simultaneously.

Work Around:

Separate the rising edges of MCLK and TCLK by more than 30ns when in framer loopback. When not in framer loopback mode, placing the jitter attenuator in the receive path (LIC1 = 00h) phase-locks the 8XCLK with RCLK and avoids data corruption.

8. HDLC SS7 SUPPORT

Description:

The SS7 support features “transmit loop” and “receive FISU discard” are not available in the DS2155 A3 revision.

Work Around:

There is no known software work around for this issue.

9. TCLK JITTER

Description:

More than 0.1UI of jitter on the transmit clock (TCLK or TCLKI) can cause an isolated 1 to be transmitted as a doubled 1. In normal operation this situation does not occur. If TCLK is derived from RCLK, the jitter attenuator typically is in the receive path so jitter is far below 0.1UI. If an independent TCLK source has jitter $>0.05UI$, the jitter attenuator must be placed in the transmit path. Therefore, the transmit LIU should never see a transmit clock with more than 0.05UI of jitter.

Work Around:

Enable the jitter attenuator in the transmit path if using a system clock for TCLK, or the receive path if using a recovered clock.

10. T1 LINE BUILD OUT

Description:

Line build outs 3 and 4 may not meet the short-haul template requirements.

Work Around:

There is no work around for line build outs 3 and 4.

11. FRAMER CRC ERROR COUNT

Description:

The potential exists for the CRC error counter to miss a CRC error if it occurs on a timer boundary.

Work Around:

There is no known software work around for this issue.

12. AUTOMATIC GAIN CONTROL ON TRANSMITTER

Description:

The output pulse may not meet template in automatic gain-control mode.

Work Around:

Use the nonautomatic gain mode as described in the TLBC register in Section 25.7 of the data sheet.

13. E1 HDLC CONTROLLERS ARE NOT TESTED BELOW ROOM TEMPERATURE

Description:

When operating in E1 mode, the HDLC controllers may not function properly at temperatures below room temperature.

Work Around:

Avoid operation at temperatures below room temperature if using the HDLC controllers in E1 mode.

14. SOFTWARE HDLC RESET FUNCTION

Description:

The soft reset function of the HDLC controllers may not issue a reset if the RHR bit is applied for less than 1 μ s.

Work Around:

The RHR bit must be applied for at least 1 μ s to ensure a reset occurs.

15. HDLC CRC ERROR

Description:

The receive packet-status information register reports a "101" (packet too short) status when the controller receives a flag message or six consecutive 1's in the message body, instead of reporting a CRC error.

Work Around:

There is no known software work around for this issue.

16. CSU FILTERS NOT TESTED BELOW ROOM TEMPERATURE

Description:

The functionality of the output CSU filters is not tested below room temperature due to the long start-up time required for the circuitry.

Work Around:

10s is normally sufficient time for the CSU filters to start and function properly over the specified temperature range.

17.2.048 OUTPUT SIGNAL IN G.703 OPERATION IS STRONGER THAN SPECIFIED

Description:

The output waveform in G.703 operation is not attenuated to the correct signal level.

Work Around:

This is a specification issue. Actual performance in a G.703 application is not impaired.

18. WRITING TO THE HDLC TRANSMIT FIFO REQUIRES VERIFICATION

Description:

The potential exists for the data written into the HDLC transmit FIFO user ports (registers H1TF and H2TF) not to be transferred into the HDLC transmit FIFOs.

Work Around:

Method 1—For messages less than 128 bytes in length:

- 1) Disable the transmitting of HDLC messages by setting all HxTCSx registers to 0.
- 2) For each byte to be written to the transmit FIFO:
 - Retrieve the value of the transmit bytes available in the H1TFBA or H2TFBA register and store it.
 - Write the byte of HDLC data into the H1TF or H2TF register.
 - Compare the current value of H1TFBA or H2TFBA to the stored value.
 - If the current value has not been decremented by one, re-write byte of data into H1TF or H2TF.
- 3) Enable the transmitting of HDLC messages by setting the appropriate HxTCSx bits.

Method 2—Allows transmission of messages longer than 128 bytes in length:

- 1) Use the transmit multiframe-event interrupt to identify the location in time of a transmitted multiframe boundary.
- 2) Wait the appropriate amount of time from a multiframe boundary interrupt to ensure that the following write operation does not occur within a timeslot used to transmit HDLC data.
- 3) Use the procedure from Step 2 in Method 1 for each byte of data until one multiframe worth of HDLC data has been loaded into the transmit HDLC FIFO.
- 4) Repeat Steps 2 and 3 until the message is completed and can be terminated with an end of message.

Method 3—Hardware mode, also allows transmission of long messages:

- 1) Use the rising edge of the 8XCLK pin to synchronize writing to the HDLC HxTF registers. The write operation must be completed prior to the falling edge of 8XCLK.

19. HDLC OPENING BYTE INDICATORS:

Description:

Under certain conditions, the HDLC opening byte indicators (H1OBT and H2OBT) in the INFO4 register may not work correctly.

Work Around:

Poll the corresponding receive packet start (RPS) bit in the H1TTBBS and H2TTBBS registers.

20. BERT DIRECTION BIT DOES NOT WORK

Description:

Setting the BERT Direction bit (BIC.1) does not correctly map the BERT into the system side of the device.

Work Around:

Do not use this bit. There is no known work around for this issue.

21. TRANSMIT ELASTIC STORE SLIP

Description:

When the transmit elastic store is enabled and a slip occurs, the transmit framer restarts the insertion of the multiframe alignment pattern. This may cause the remote port to lose sync.

Work Around:

There is no known work around for this issue.

22. RECEIVE ELASTIC STORE

Description:

When operating in T1 mode with the receive elastic store enabled and RSYSCCLK at 2.048MHz, blue alarms and Loop codes will not be detected.

Work Around:

There is no known work around for this issue.

23. ELASTIC STORE OPERATION IN E1 MODE

Description:

When operating in E1 mode with either elastic store enabled, data in the first four channels can be corrupted if both the input and output elastic-store clocks are precisely edge aligned.

Work Around:

There is no known work around for this issue.

24. DEVICE ID REGISTER READS INCORRECT VALUE

Description:

The device ID register (IDR) contains an incorrect value of B0h, which would have been reserved for revision A1.

Work Around:

There is no known work around for this issue.

25. BERT DALY PATTERN SYNCHRONIZATION

Description:

If a BRLOS occurs while switching from the Daly pattern to any other BERT pattern after being synchronized to the Daly pattern, the DS2155 BERT may not resynchronize to the new pattern.

Work Around:

Before switching out of the Daly pattern, place the device in framer loopback by setting FLB = 1. After switching to the new pattern, remove the loopback by setting FLB = 0.

26. ELASTIC STORE IN E1 TO E1 OPERATION

Description:

When using the elastic stores to absorb phase or frequency differences in E1 operating mode with an E1 rate backplane, the first four channels might experience bit errors when the rising edges of the system clock (TSYSCLK, RSYSCLK) and the backplane clock (TCLK, RCLK) are precisely synchronized.

Work Around:

Separate the rising edges of the system and backplane clocks so that they are more than 60ns apart. Alternatively, do not use the elastic stores when both the system and backplane are operating at the E1 rate.

27. INPUT LEVEL UNDER THRESHOLD (ILUT) BIT IS NOT FUNCTIONAL

Description:

The input level under threshold bit (ILUT) in Status Register 1 (SR1.7) is not functional. Due to a digital logic error, this bit does not function correctly and will always be set.

Work Around:

There is no known work around for this issue.

28. TSTRST PIN WILL HOLD THE PART IN RESET WHILE ASSERTED

Description:

The TSTRST pin will hold the part in reset when the pin is asserted (active high) and not just on a low to high transition as stated in the data sheet. As stated in the data sheet, a low-to-high transition will cause a reset to the part, and leaving the TSTRST pin high will tri-state all the output and IO pins. In addition to tri-stating the output and IO pins, leaving the TSTRST pin high will also hold the part in a reset state that does not allow access to the configuration registers or the parallel port.

Work Around:

Do not leave the TSTRST pin asserted if access to the configuration registers is required.