**FEATURES**

- Very Low Standby Current: 10µA
- Available in Space-Saving 8-Lead MSOP Package
- Output Currents: Up to 5A
- Wide V\textsubscript{IN} Range: 2.8V to 20V Operation
- V\textsubscript{OUT} Range: 1.23V to 18V
- High Efficiency: Over 93% Possible
- ±2% Output Accuracy
- Very Low Dropout Operation: 100% Duty Cycle
- Current Mode Operation for Excellent Line and Load Transient Response
- Defeatable Burst Mode\textsuperscript{TM} Operation
- Short-Circuit Protected
- Optional Programmable Soft-Start
- Micropower Shutdown: I\textsubscript{Q} = 2µA

**APPLICATIONS**

- Cellular Telephones and Wireless Modems
- 1- to 4-Cell Lithium-Ion-Powered Applications
- Portable Instruments
- Battery-Powered Equipment
- Battery Chargers
- Scanners

**DESCRIPTION**

The LTC\textsuperscript{®}1771 is a high efficiency current mode step-down DC/DC controller that draws as little as 10µA DC supply current to regulate the output at no load while maintaining high efficiency for loads up to several amps.

The LTC1771 drives an external P-channel power MOSFET using a current mode, constant off-time architecture. An external sense resistor is used to program the operating current level. Current mode control provides short-circuit protection, excellent transient response and controlled start-up behavior. Burst Mode operation enables the LTC1771 to maintain high efficiency down to extremely low currents. Shutdown mode further reduces the supply current to a mere 2µA. For low noise applications, Burst Mode operation can be easily disabled with the MODE pin.

Wide input supply range of 2.8V to 18V (20V maximum) and 100% duty cycle operation for low dropout make the LTC1771 ideal for a wide variety of battery-powered applications where maximizing battery life is important.

The LTC1771’s availability in both 8-lead MSOP and SO packages provides for a minimum area solution.

\* LTC and LT are registered trademarks of Linear Technology Corporation.

Burst Mode is a trademark of Linear Technology Corporation.

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**TYPICAL APPLICATION**

![Figure 1. High Efficiency Step-Down Converter](figure1.png)

**LTC1771 Efficiency**

![LTC1771 Efficiency Graph](efficiency.png)
LTC1771

ABSOLUTE MAXIMUM RATINGS *(Note 1)*

Input Supply Voltage (V_IN) ......................... –0.3V to 20V
Peak Driver Output Current < 10μs (PGATE) ........... 1A
RUN/SS Voltage ................................... –0.3V to (V_IN + 0.3V)*
MODE Voltage ....................................... –0.3V to 20V
I_TH, V_FB Voltage .................................. –0.3V to 5V
SENSE Voltage (V_IN > 12V) ...................... (V_IN – 12V) to (V_IN + 0.3V)*
SENSE Voltage (V_IN ≤ 12V) ........................ –0.3V to (V_IN + 0.3V)*

Junction Temperature (Note 2) ....................... 125°C
Operating Temperature Range (Note 3)
  LTC1771E ........................................ –40°C to 85°C
  LTC1771I ........................................ –40°C to 85°C
Storage Temperature Range ......................... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) .............. 300°C

*RUN/SS and SENSE cannot exceed 20V.

PACKAGE/ORDER INFORMATION

<table>
<thead>
<tr>
<th>ORDER PART NUMBER</th>
<th>TOP VIEW</th>
</tr>
</thead>
<tbody>
<tr>
<td>LTC1771EMS8</td>
<td></td>
</tr>
<tr>
<td>LTC1771ES8</td>
<td></td>
</tr>
<tr>
<td>LTC1771I</td>
<td></td>
</tr>
<tr>
<td>LTC1771IS8</td>
<td></td>
</tr>
</tbody>
</table>

ORDER PART NUMBER

ART VIEW

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

The • denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_IN = 10V, V_RUN = open unless otherwise specified.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_FB</td>
<td>Feedback Voltage</td>
<td>(Note 5)</td>
<td>• 1.205</td>
<td>1.230</td>
<td>1.255</td>
<td>V</td>
</tr>
<tr>
<td>I_FB</td>
<td>Feedback Current</td>
<td>(Note 5)</td>
<td>• 1</td>
<td>10</td>
<td>nA</td>
<td></td>
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<tr>
<td>I_SUPPLY</td>
<td>No-Load Supply Current</td>
<td>V_IN = 10V, I_LOAD = 0 (Note 6)</td>
<td>10</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ΔV_LINEREG</td>
<td>Reference Voltage Line Regulation</td>
<td>V_IN = 5V to 15V (Note 5)</td>
<td>• 0.003</td>
<td>0.03</td>
<td>%/V</td>
<td></td>
</tr>
<tr>
<td>ΔV_LOADREG</td>
<td>Output Voltage Load Regulation</td>
<td>I_TH = 0.5V to 2V, Burst Disabled (Note 5)</td>
<td>• 0.25</td>
<td>1</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>I_Q</td>
<td>Input DC Supply Current</td>
<td>(Note 4)</td>
<td>• 150</td>
<td>235</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Active Mode (PGATE = 0V)</td>
<td>V_IN = 2.8V to 18V</td>
<td>9</td>
<td>15</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Sleep Mode (Note 6)</td>
<td>V_IN = 2.8V to 18V, V_FB = 1.5V</td>
<td>2</td>
<td>6</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Shutdown</td>
<td>V_IN = 2.8V to 18V, V_FB = 0V</td>
<td>175</td>
<td>275</td>
<td>μA</td>
<td></td>
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<tr>
<td></td>
<td>Short Circuit</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ΔVSENSE(MAX)</td>
<td>Maximum Current Sense Threshold</td>
<td>V_FB = V_REF – 20mV</td>
<td>• 110</td>
<td>140</td>
<td>180</td>
<td>mV</td>
</tr>
<tr>
<td>ΔVSENSE(MIN)</td>
<td>Minimum Current Sense Threshold</td>
<td>V_FB = V_REF + 20mV, Burst Disabled</td>
<td>• –25</td>
<td>mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ΔVSENSE(SLEEP)</td>
<td>Sleep Current Sense Threshold</td>
<td>I_TH = 1V</td>
<td>• 50</td>
<td>mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>t_OFF</td>
<td>Switch Off Time</td>
<td>V_FB at Regulated Value</td>
<td>• 3</td>
<td>3.5</td>
<td>4</td>
<td>μs</td>
</tr>
<tr>
<td></td>
<td>V_FB = 0V</td>
<td></td>
<td>70</td>
<td>μs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_MODE</td>
<td>Mode Pin Threshold</td>
<td>V_MODE Rising</td>
<td>• 0.5</td>
<td>1.3</td>
<td>2</td>
<td>V</td>
</tr>
</tbody>
</table>
**ELECTRICAL CHARACTERISTICS**

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are $T_A = 25^\circ C$. $V_{IN} = 10V$, $V_{RUN} = \text{open unless otherwise specified.}$

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{RUN/SS}$</td>
<td>RUN/SS Pin Threshold</td>
<td>$V_{RUN/SS}$ Rising</td>
<td>●</td>
<td>0.5</td>
<td>1.0</td>
<td>2</td>
</tr>
<tr>
<td>$I_{RUN}$</td>
<td>Source Current</td>
<td>$V_{RUN} = 0V$, $V_{IN} = 2.8V$ to $18V$</td>
<td>0.3</td>
<td>1</td>
<td>3</td>
<td>μA</td>
</tr>
<tr>
<td>$C_{LOAD}$</td>
<td>PGATE Rise Time (Note 7)</td>
<td>$C_{LOAD} = 2000pF$</td>
<td>70</td>
<td>140</td>
<td>70</td>
<td>140</td>
</tr>
<tr>
<td>$C_{LOAD}$</td>
<td>PGATE Fall Time</td>
<td>$C_{LOAD} = 2000pF$</td>
<td>70</td>
<td>140</td>
<td>70</td>
<td>140</td>
</tr>
</tbody>
</table>

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

**Note 2:** $T_J$ is calculated from the ambient temperature $T_A$ and power dissipation $P_D$ according to the following formulas:

- LTC1771S8: $T_J = T_A + (P_D)(110^\circ C/W)$
- LTC1771MS8: $T_J = T_A + (P_D)(150^\circ C/W)$

**Note 3:** The LTC1771E is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTC1771I is guaranteed and tested over the –40°C to 85°C operating temperature range.

**Note 4:** Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Applications Information.

**Note 5:** The LTC1771 is tested in a feedback loop that servos $V_{FB}$ to the balance point for the error amplifier ($V_{ITH} = 1.23V$).

**Note 6:** No-load supply current consists of sleep mode current (9μA typical) plus a small switching component necessary to overcome Schottky diode leakage and feedback resistor current.

**Note 7:** $t_R$ and $t_F$ are measured at 10% to 90% levels.

---

**TYPICAL PERFORMANCE CHARACTERISTICS**

**Efficiency vs Input Voltage**

![Efficiency vs Input Voltage](image1)

**Efficiency vs Load Current**

![Efficiency vs Load Current](image2)

**Line Regulation**

![Line Regulation](image3)
TYPICAL PERFORMANCE CHARACTERISTICS

**Load Regulation**

**Active Mode Quiescent Current vs Input Voltage**

**Sleep Quiescent Current vs Input Voltage**

**Shutdown Quiescent Current vs Input Voltage**

**Run/SS Current vs Input Voltage**

**Current Sense Voltage vs Temperature**

**Reference Voltage vs Temperature**

**Load Step Transient Response**

**Burst Mode Operation**
**PIN FUNCTIONS**

**RUN/SS (Pin 1):** The voltage level on this pin controls shutdown/run mode (ground = shutdown, open/high = run). Connecting an external capacitor to this pin provides soft-start.

**I_{TH} (Pin 2):** Error Amplifier Compensation Point. The current comparator threshold increases with this control voltage. Nominal voltage range for this pin is 0V to 3V.

**V_{FB} (Pin 3):** Feedback of Output Voltage for Comparison to Internal 1.23V Reference. An external resistive divider across the output is returned to this pin.

**GND (Pin 4):** Ground Pin.

**PGATE (Pin 5):** High Current Gate Driver for External P-Channel MOSFET Switch. Voltage swing is from ground to V_{IN}.

**V_{IN} (Pin 6):** Main Input Voltage Supply Pin.

**SENSE (Pin 7):** Current Sense Input for Monitoring Switch Current. Maximum switch current and Burst Mode threshold is programmed with an external resistor between SENSE and V_{IN}.

**MODE (Pin 8):** Burst Mode Enable/Disable Pin. Connecting this pin to V_{IN} (or above 2V) enables Burst Mode operation, while connecting this pin to ground disables Burst Mode operation. Do not leave floating.

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**FUNCTIONAL BLOCK DIAGRAM**

[Diagram of the LTC1771 block diagram with pins and connections labeled.]
Main Control Loop

The LTC1771 uses a constant off-time, current mode step-down architecture. During normal operation, the P-channel MOSFET is turned on at the beginning of each cycle and turned off when the current comparator C triggers the 1-shot timer. The external MOSFET switch stays off for the 3.5μs 1-shot duration and then turns back on again to begin a new cycle. The peak inductor current at which C triggers the 1-shot is controlled by the voltage on Pin 3 (I_{TH}), the output of the error amplifier EA. An external resistive divider connected between V_{OUT} and ground allows EA to receive an output feedback voltage V_{FB}. When the load current increases, it causes a slight decrease in V_{FB} relative to the 1.23V reference, which in turn causes the I_{TH} voltage to increase until the average inductor current matches the new load current.

The main control loop is shut down by pulling Pin 1 (RUN/SS) low. Releasing RUN/SS allows an internal 1μA current source to charge soft-start capacitor CSS. When CSS reaches 1V, the main control loop is enabled with the I_{TH} voltage clamped at approximately 40% of its maximum value. As CSS continues to charge, I_{TH} is gradually released allowing normal operation to resume.

Burst Mode Operation

The LTC1771 provides outstanding low current efficiency and ultralow no-load supply current by using Burst Mode operation when the MODE pin is pulled above 2V. During Burst Mode operation, short burst cycles of normal switching are followed by a longer idle period with the switch off and the load current is supplied by the output capacitor. During this idle period, only the minimum required circuitry—1.23V reference and error amp—are left on, and the supply current is reduced to 9μA. At no load, the output capacitor is still discharged very slowly by leakage current in the Schottky diode and feedback resistor current resulting in very low frequency burst cycles that add a few more microamps to the supply current.

Burst Mode operation is provided by clamping the minimum I_{TH} voltage at 1V which represents about 25% of maximum load current. If the load falls below this level, i.e. the I_{TH} voltage tries to fall below 1V, the burst comparator B switches state signaling the LTC1771 to enter sleep mode. During this time, EA is reduced to 10% of its normal operating current and the external compensation capacitor is disconnected and clamped to 1V so that the EA can drive its output with the lower available current. As the load discharges the output capacitor, the internal I_{TH} voltage increases. When it exceeds 1V the burst comparator exits sleep mode, reconnects the external compensation components to the error amplifier output, and returns EA to full power along with the other necessary circuitry. This scheme (patent pending) allows the EA to be reduced to such a low operating current during sleep mode without adding unacceptable delay to wake up the LTC1771 due to the compensation capacitor on I_{TH} required for stability in normal operation.

Burst Mode operation can be disabled by pulling the MODE pin to ground. In this mode of operation, the burst comparator B is disabled and the I_{TH} voltage allowed to go all the way to 0V. The load can now be reduced to about 1% of maximum load before the loop skips cycles to maintain regulation. This mode provides a low noise output spectrum, useful for reducing both audio and RF interference, at the expense of reduced efficiency at light loads.

Off-Time

The off-time duration is 3.5μs when the feedback voltage is close to the reference voltage; however, as the feedback voltage drops, the off-time lengthens and reaches a maximum value of about 70μs when V_{FB} is zero. This ensures that the inductor current has enough time to decay when the reverse voltage across the inductor is low such as during short circuit, thus protecting the MOSFET and inductor.
The basic LTC1771 application circuit is shown in Figure 1 on the first page. External component selection is driven by the load requirement and begins with the selection of \( R_{SENSE} \). Once \( R_{SENSE} \) is known, \( L \) can be chosen. Next, the MOSFET and \( D_1 \) are selected. The inductor is chosen based largely on the desired amount of ripple current and for Burst Mode operation. Finally \( C_{IN} \) is selected for its ability to handle the required RMS input current and \( C_{OUT} \) is chosen with low enough ESR to meet the output voltage ripple and transient specifications.

**R\(_{SENSE}\) Selection**

\( R_{SENSE} \) is chosen based on the required output current. The LTC1771 current comparator has a maximum threshold of 140mV/\( R_{SENSE} \). The current comparator threshold sets the peak inductor current, yielding a maximum average output current \( I_{MAX} \) equal to the peak less half the peak-to-peak ripple current \( \Delta I_L \). For best performance when Burst Mode operation is enabled, choose \( \Delta I_L \) equal to 35% of peak current. Allowing a margin for variations in the LTC1771 and external components gives the following equation for choosing \( R_{SENSE} \):

\[
R_{SENSE} = \frac{100\text{mV}}{I_{MAX}}
\]

At higher supply voltages, the peak currents may be slightly higher due to overshoot from current comparator delay and can be predicted from the second term in the following equation:

\[
I_{PEAK} = \frac{0.14}{R_{SENSE}} + 0.5\left(\frac{V_{IN} - V_{OUT}}{L(\mu H)}\right)^{1/2}
\]

**Inductor Value Selection**

Once \( R_{SENSE} \) is known, the inductor value can be determined. The inductance value has a direct effect on ripple current. The ripple current decreases with higher inductance and increases with higher \( V_{OUT} \). The ripple current during continuous mode operation is set by the off-time and inductance to be:

\[
\Delta I_L(\text{CONT}) = t_{OFF}\left(\frac{V_{OUT} + V_D}{L}\right)
\]

where \( t_{OFF} = 3.5\mu s \). However, the ripple current at low loads during Burst Mode operation is:

\[
\Delta I_L(\text{BURST}) = 35\% \text{ of } I_{PEAK} = 0.05/R_{SENSE}
\]

For best efficiency when Burst Mode operation is enabled, choose:

\[
\Delta I_L(\text{CONT}) \leq \Delta I_L(\text{BURST})
\]

so that the inductor current is continuous during the burst periods. This sets a minimum inductor value of:

\[
L_{\text{MIN}} = (75\mu H)(V_{OUT} + V_D)(R_{SENSE})
\]

When burst is disabled, ripple currents less than \( \Delta I_L(\text{BURST}) \) can be achieved by choosing \( L > L_{\text{MIN}} \). Lower ripple current reduces output voltage ripple and core losses, but too low of ripple current will adversely effect efficiency.

**Inductor Core Selection**

Once the value of \( L \) is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite, molypermalloy or Kool M\text{™} cores. Actual core loss is independent of core size for a fixed inductor value, but is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates “hard,” which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent increase in voltage ripple. Do not allow the core to saturate!

Molypermalloy (from Magnetics, Inc.) is a very good, low loss core material for toroids, but it is more expensive than ferrite. A reasonable compromise from the same manufacturer is Kool M\text{™}. Toroids are space efficient, especially when you can use several layers of wire. Because they generally lack a bobbin, mounting is more difficult. However, designs for surface mount are available that do not increase the height significantly.

Kool M\text{™} is a registered trademark of Magnetics, Inc.
**Power MOSFET Selection**

An external P-channel power MOSFET must be selected for use with the LTC1771. The main selection criteria for the power MOSFET are the threshold voltage $V_{GS(TH)}$ and the “on” resistance $R_{DS(ON)}$, reverse transfer capacitance and total gate charge.

Since the LTC1771 can operate down to input voltages as low as 2.8V, a sublogic level threshold MOSFET ($R_{DS(ON)}$ guaranteed at $V_{GS} = 2.5V$) is required for applications that work close to this voltage. When these MOSFETs are used, make sure that the input supply to the LTC1771 is less than the absolute maximum $V_{GS}$ rating (typically 12V), as the MOSFET gate will see the full supply voltage.

The required $R_{DS(ON)}$ of the MOSFET is governed by its allowable power dissipation. For applications that may operate the LTC1771 in dropout, i.e. 100% duty cycle, at its worst case the required $R_{DS(ON)}$ is given by:

$$R_{DS(ON)} = \frac{P_{P}}{(I_{OUT(MAX)})^2(1 + \delta_{P})}$$

where $P_{P}$ is the allowable power dissipation and $\delta_{P}$ is the temperature dependency of $R_{DS(ON)}$. $(1 + \delta_{P})$ is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs temperature curve, but $0.005/^\circ C$ can be used as an approximation for low voltage MOSFETs.

In applications where the maximum duty cycle is less than 100% and the LTC1771 is in continuous mode, the $R_{DS(ON)}$ is governed by:

$$R_{DS(ON)} = \frac{P_{P}}{(DC)I_{OUT}^2(1 + \delta_{P})}$$

where $DC = \frac{V_{OUT} + V_{D}}{V_{IN} + V_{D}}$ is the maximum operating duty cycle of the LTC1771.

**Catch Diode Selection**

The catch diode carries load current during the off-time. The average diode current is therefore dependent on the P-channel switch duty cycle. At high input voltages the diode conducts most of the time. As $V_{IN}$ approaches $V_{OUT}$ the diode conducts only a small fraction of the time. The most stressful condition for the diode is when the output is short-circuited. Under this condition, the diode must safely handle $I_{PEAK}$ at close to 100% duty cycle.

To maximize both low and high current efficiencies, a fast switching diode with low forward drop and low reverse leakage should be used. Low reverse leakage current is critical to maximize low current efficiency since the leakage can potentially exceed the magnitude of the LTC1771 supply current. Low forward drop is critical for high current efficiency since loss is proportional to forward drop. The effect of reverse leakage and forward drop on no-load supply current and efficiency for various Schottky diodes is shown in Table 1. As can be seen, these are conflicting parameters and the user must weigh the importance of each spec in choosing the best diode for the application.

<table>
<thead>
<tr>
<th>DIODE</th>
<th>LEAKAGE ((V_{R} = 3.3V))</th>
<th>$V_F$ @ 1A</th>
<th>NO-LOAD SUPPLY CURRENT</th>
<th>EFFICIENCY AT 10V/1A</th>
</tr>
</thead>
<tbody>
<tr>
<td>MBR0540</td>
<td>0.25$\mu$A</td>
<td>0.50V</td>
<td>10.4$\mu$A</td>
<td>86.3%</td>
</tr>
<tr>
<td>UPS5817</td>
<td>2.8$\mu$A</td>
<td>0.41V</td>
<td>11.8$\mu$A</td>
<td>88.2%</td>
</tr>
<tr>
<td>MBR0520</td>
<td>3.7$\mu$A</td>
<td>0.36V</td>
<td>12.2$\mu$A</td>
<td>88.4%</td>
</tr>
<tr>
<td>MBR120T3</td>
<td>4.4$\mu$A</td>
<td>0.43V</td>
<td>12.2$\mu$A</td>
<td>87.9%</td>
</tr>
<tr>
<td>MBM120LT3</td>
<td>8.3$\mu$A</td>
<td>0.32V</td>
<td>14.0$\mu$A</td>
<td>89.4%</td>
</tr>
<tr>
<td>MBR320</td>
<td>19.7$\mu$A</td>
<td>0.29V</td>
<td>20.0$\mu$A</td>
<td>89.8%</td>
</tr>
</tbody>
</table>

**C\textsubscript{IN} and C\textsubscript{OUT} Selection**

At higher load currents, when the inductor current is continuous, the source current of the P-channel MOSFET is a square wave of duty cycle $V_{OUT}/V_{IN}$. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum capacitor current is given by:

$$C_{IN} \text{ required } I_{RMS} = \frac{I_{MAX}V_{OUT}(V_{IN} - V_{OUT})^{1/2}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturer’s
APPLICATIONS INFORMATION

Ripple current ratings are often based on 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Do not underspecify this component. An additional 0.1μF ceramic capacitor is also helpful on VIN for high frequency decoupling.

The selection of COUT is driven by the required effective series resistance (ESR). Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple (ΔVOUT) in continuous mode is approximated by:

\[
\Delta V_{OUT} \approx I_{RIPPLE} \left( \frac{ESR + \frac{1}{8fC_{OUT}}}{fC_{OUT}} \right)
\]

where f is the operating frequency, COUT is the output capacitance and I_RIPPLE is the ripple current in the inductor. For output ripple less than 100mV, assure COUT required ESR is <2RSENSE.

The first condition relates to the ripple current into the ESR of the output capacitance while the second term guarantees that the output capacitance does not significantly discharge during the operating frequency period due to ripple current. The choice of using smaller output capacitance increases the ripple voltage due to the discharging term but can be compensated for by using capacitors of very low ESR to maintain the ripple voltage at or below 50mV. The ITH pin OPTI-LOOP™ compensation components can be optimized to provide stable, high performance transient response regardless of the output capacitors selected.

When running into dropout, extra input and output capacitance may be necessary for optimal performance due to the drop in frequency as the duty cycle approaches 100%. Compare Figure 1 to the low dropout regulators shown in the Typical Applications section for recommended CIN, COUT, CFF and Cc values for low dropout regulators vs regulators not requiring low dropout.

Manufacturers such as Nichicon, United Chemicon and Sanyo should be considered for high performance through-hole capacitors. The OS-CON semiconductor dielectric capacitor available from Sanyo has the lowest ESR for its size of any aluminum electrolytic at a somewhat higher price. Typically once the ESR requirement is satisfied, the RMS current rating generally far exceeds the I_{RIPPLE} requirement.

In surface mount applications multiple capacitors may have to be paralleled to meet the ESR or RMS current handling requirements of the application. Aluminum electrolytics and dry tantalum capacitors are both available in surface mount configurations. In case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS, AVX TPSV and KEMET T510 series of surface mount tantalums, available in case heights ranging from 2mm to 4mm. Other capacitor types include Sanyo OS-CON, Sanyo POSCAP, Nichicon PL series and Panasonic SP.

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting efficiency and which change would produce the most improvement. Efficiency can be expressed as:

Efficiency = 100% – (L1 + L2 +L3 + ...)

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in the LTC1771 circuits: the LTC1771 DC bias current, MOSFET gate charge current, I^2R losses and catch diode losses.

1. The DC bias current is 9μA at no load and increases proportionally with load up to a constant 150μA during continuous mode. This bias current is so small that this loss is negligible at loads above a milliamp but at no load accounts for nearly all of the loss.

2. The MOSFET gate charge current results from switching the gate capacitance of the power MOSFET switch. Each time the gate is switched from high to low to high again, a packet of charge dQ moves from VIN to ground. The resulting dQ/dt is the current out of VIN which is typically much larger than the DC bias current. In

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APPLICATIONS INFORMATION

continuous mode, \( I_{GATECHG} = f_{QP} \) where \( Q_P \) is the gate charge of the internal switch. Both the DC bias and gate charge losses are proportional to \( V_{IN} \) and thus their effects will be more pronounced at higher supply voltages.

3. \( I^2R \) losses are predicted from the internal switch, inductor and current sense resistor. In continuous mode the average output current flows through \( L \) but is “chopped” between the P-channel MOSFET in series with \( R_{SENSE} \) and the output diode. The MOSFET \( R_{DS(ON)} \) plus \( R_{SENSE} \) multiplied by the duty cycle can be summed with the resistance of \( L \) to obtain \( I^2R \) losses.

4. The catch diode loss is proportional to the forward drop as the diode conducts current during the off-time and is more pronounced at high supply voltages where the off-time is long. However, as discussed in the Catch Diode section, diodes with lower forward drops often have higher leakage currents, so although efficiency is improved, the no-load supply current will increase. The diode loss is calculated by multiplying the forward voltage drop times the diode duty cycle multiplied by the load current.

Other losses including \( C_{IN} \) and \( C_{OUT} \) ESR dissipative losses, and inductor core losses, generally account for less than 2% total additional loss.

Output Voltage Programming

The output voltage is programmed with an external divider from \( V_{OUT} \) to \( V_{FB} \) (Pin 1) as shown in Figure 2. The regulated voltage is determined by:

\[
V_{OUT} = 1.23 \left( 1 + \frac{R_2}{R_1} \right)
\]

To minimize no-load supply current, resistor values in the megohm range should be used. The increase in supply current due to the feedback resistors can be calculated from:

\[
\Delta I_{VIN} = \frac{V_{OUT}}{R_1 + R_2} \left( \frac{V_{OUT}}{V_{IN}} \right)
\]

A 5pF feedforward capacitor across \( R_2 \) is recommended to minimize output voltage ripple in Burst Mode operation.

Run/Soft-Start Function

The RUN/SS pin is a dual purpose pin that provides the soft-start function and a means to shut down the LTC1771. Soft-start reduces the input surge current from \( V_{IN} \) by gradually increasing the internal current limit. Power supply sequencing can also be accomplished using this pin.

An internal 1\( \mu \)A current source charges up an external capacitor \( C_{SS} \). When the voltage on the RUN/SS reaches 1V, the LTC1771 begins operating. As the voltage on the RUN/SS continues to ramp from 1V to 2.2V, the internal current limit is also ramped at a proportional linear rate. The current limits begins near 40% maximum load at \( V_{RUN/SS} = 1V \) and ends at maximum load at \( V_{RUN/SS} = 2.2V \). The output current thus ramps up slowly, reducing the starting surge current required from the input power supply. If the RUN/SS has been pulled all the way to ground, there will be a delay before the current limit starts increasing and is given by:

\[
t_{DELAY} = \frac{C_{SS}}{I_{CHG}}
\]

where \( I_{CHG} = 1\mu A \). Pulling the RUN/SS pin below 0.5V puts the LTC1771 into a low quiescent current shutdown (\( I_Q < 2\mu A \)).

Foldback Current Limiting

As described in the Catch Diode Selection, the worst-case dissipation for diode occurs with a short-circuit output, when the diode conducts the current limit value almost continuously. In most applications this will not cause excessive heating, even for extended fault intervals. However, when heat sinking is at a premium or higher forward voltage drop diodes are being used, foldback current
limiting should be added to reduce the current in proportion to the severity of the fault.

Foldback current limiting is implemented by adding two diodes in series between the output and the $I_{TH}$ pin as shown in the Functional Diagram. In a hard short ($V_{OUT} = 0V$) the current will be reduced to approximately 25% of the maximum output current.

**Minimum On-Time Considerations**

Minimum on-time $t_{ON(MIN)}$ is the smallest amount of time that the LTC1771 is capable of turning the top MOSFET on and off again. It is determined by internal timing delays and the amount of gate charge required to turn on the P-channel MOSFET. Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure that:

$$t_{ON} = t_{OFF} \left( \frac{V_{OUT} + V_D}{V_{IN} - V_{OUT}} \right) > t_{ON(MIN)}$$

where $t_{OFF} = 3.5\mu s$ and $t_{ON(MIN)}$ is generally about $0.4\mu s$ for the LTC1771.

As the on-time approaches $t_{ON(MIN)}$, the LTC1771 will remain in Burst Mode operation for an increasingly larger portion of the load range (see Figure 3) and at or below $t_{ON(MIN)}$ will remain in Burst Mode operation 100% of the time. The output voltage will continue to be regulated, but the ripple current and ripple voltage will increase.

**Mode Pin**

Burst Mode operation is disabled by pulling MODE (Pin 8) below 0.5V. Disabling Burst Mode operation provides a low noise output spectrum, useful for reducing both audio and RF interference. It does this by keeping the frequency constant (for fixed $V_{IN}$) down to much lower load current (1% to 2% of $I_{MAX}$) and reducing the amount of output voltage and current ripple at light loads. When Burst Mode operation is disabled, efficiency is reduced at light loads and no load supply current increases to 175µA.

**Low Supply Operation**

Although the LTC1771 can function down to 2.8V, the maximum allowable output current is reduced when $V_{IN}$ decreases below 3.2V. Figure 4 shows the amount of change as the supply is reduced below 3.2V, where 100% of maximum load equals $0.1/R_{SENSE}$. To ensure adequate output current at $V_{IN} < 3.2V$, simply lower $R_{SENSE}$ by the same percentage as the current reduction in Figure 4.

**PC Board Layout Checklist**

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC1771. These items are also illustrated graphically in the layout diagram of Figure 5. Check the following in your layout:

1. Is the Schottky diode closely connected to the drain of the external MOSFET and the input cap ground?
**APPLICATIONS INFORMATION**

2. Is the 0.1 μF input decoupling capacitor *closely* connected between V\textsubscript{IN} (Pin 6) and ground (Pin 4)? This capacitor carries the high frequency peak currents.

3. Does the V\textsubscript{FB} pin connect directly to the feedback resistors? The resistive divider R1 and R2 must be connected between the (+) plate of C\textsubscript{OUT} and signal ground. Locate the feedback resistors right next to the LTC1771. The V\textsubscript{FB} line should not be routed close to any nodes with high slew rates.

4. Is the 1000 pF decoupling capacitor for the current sense resistor connected as close as possible to Pins 6 and 7? Ensure accurate current sensing with Kelvin connections to the sense resistor.

5. Is the (+) plate of C\textsubscript{IN} *closely* connected to the sense resistor? This capacitor provides the AC current to the MOSFET.

6. Are the signal and power grounds segregated? The signal ground consists of the (–) plate of C\textsubscript{OUT}, Pin 4 of the LTC1771 and the resistive divider. The power ground consists of the Schottky diode anode and the (–) plate of C\textsubscript{IN} which should have as short lead lengths as possible.

7. Keep the switching node (SW) and the gate node (PGATE) away from sensitive small signal nodes, especially the voltage sensing feedback pin (V\textsubscript{FB}), and minimize their PC trace area.

**Design Example**

As a design example, assume V\textsubscript{IN} = 10V (nominal), V\textsubscript{IN} = 15V\textsubscript{(MAX)}, V\textsubscript{OUT} = 3.3V, and I\textsubscript{MAX} = 2A. With this information, we can easily calculate all the important components.

\[ R_{\text{SENSE}} = 100 \text{mV}/2A = 0.05 \Omega \]

To optimize low current efficiency, MODE pin is tied to V\textsubscript{IN} to enable Burst Mode operation, thus the minimum inductance necessary is:

\[ L_{\text{MIN}} = 70 \mu\text{H}(3.3V + 0.5)(0.05 \Omega) = 13.3 \mu\text{H} \]

15 μH is chosen for the application.

\[ \Delta L = 3.5 \mu\text{s} \left( \frac{3.3V + 0.5V}{15 \mu\text{H}} \right) = 0.89\text{A} \]

For the feedback resistors, choose R1 = 1M to minimize supply current. R2 can then be calculated to be:

\[ R2 = (V\text{OUT}/1.23 – 1) \cdot R1 = 1.68\text{M} \]

Assume that the MOSFET dissipation is to be limited to P\textsubscript{P} = 0.25W.

If \( T_A = 70^\circ \text{C} \) and the thermal resistance of the MOSFET is 83°C/W, then the junction temperatures will be 91°C and \( \delta_p = 0.33 \). The required R\textsubscript{DS(on)} for the MOSFET can now be calculated:

\[ P - \text{Channel} \quad R_{\text{DS(on)}} = \frac{0.25W}{\left( \frac{3.3V + 0.5V}{10V + 0.5V} \right)^2(1.33)} = 0.130\Omega \]

Since the gate of the MOSFET will see the full input voltage, a MOSFET must be selected whose V\textsubscript{GS(MAX)} > 15V. A P-channel MOSFET that meets both the V\textsubscript{GS(MAX)} and R\textsubscript{DS(on)} requirement is the Si6447DQ.

The most stringent requirement for the Schottky diode occurs when V\textsubscript{OUT} = 0V (i.e., short circuit) at maximum V\textsubscript{IN}. In this case the worst-case dissipation rises to:

\[ P_D = I_{SC(AVG)}(V_D) \left( \frac{V_{IN}}{V_{IN} + V_D} \right) \]
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With a 0.05Ω sense resistor $I_{SC(AVG)} = 2A$ will result, increasing the 0.5V Schottky diode dissipation to 1W. $C_{IN}$ is chosen for a RMS current rating of at least 1A at temperature. $C_{OUT}$ is chosen with an ESR of 0.05Ω for low output ripple. The output voltage ripple due to ESR is approximately:

$$V_{ORIPPLE} = (R_{ESR})(\Delta I_L) = 0.05\Omega \times (0.89A_{P-P}) = 45mV_{P-P}$$

TYPICAL APPLICATIONS

3.3V to 2.5V/1A Regulator with Burst Mode Operation Enabled

![Diagram of 3.3V to 2.5V/1A Regulator]

- $C_{IN}$: AVX TPSD226M025R0200
- $C_{OUT}$: SANYO POSCAP 6TPB150M
- D1: MICROSEMI UPS5817
- L1: SUMIDA CR75-220

Low Dropout 5V/2A Regulator with Burst Mode Operation Disabled

![Diagram of Low Dropout 5V/2A Regulator]

- $C_{IN}$: AVX TPSD226M025R0200
- $C_{OUT}$: SANYO POSCAP 6TPB150M
- D1: MICROSEMI UPS5817
- L1: SUMIDA CR75-220
**Low Dropout Single Cell Lithium-Ion to 3V**

**12V/1A Zeta Converter**

**2.5V/1A Regulator with Foldback Current Limit**
TYPICAL APPLICATIONS

4-NiCd/NiMH Battery Charger

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PACKAGE DESCRIPTION

Dimension in inches (millimeters) unless otherwise noted.

MS8 Package
8-Lead Plastic MSOP
(LTC DWG # 05-08-1660)

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)
5V/1A Zeta Converter

### RELATED PARTS

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<tr>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
<th>COMMENTS</th>
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</thead>
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<tr>
<td>LTC1147 Series</td>
<td>High Efficiency Step-Down Switching Regulator Controllers</td>
<td>100% DC, 3.5V ≤ VIN ≤ 16V</td>
</tr>
<tr>
<td>LTC1174/LTC1174-3.3/LTC1174-5</td>
<td>High Efficiency Step-Down and Inverting DC/DC Converters</td>
<td>Selectable IPEAK = 300mA or 600mA</td>
</tr>
<tr>
<td>LTC1265</td>
<td>1.2A High Efficiency Step-Down DC/DC Converter</td>
<td>Burst Mode Operation, Internal MOSFET</td>
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<tr>
<td>LTC1474/LTC1475</td>
<td>Low Quiescent Current Step-Down Regulators</td>
<td>Monolithic, IQ = 10μA, 400mA, MS8</td>
</tr>
<tr>
<td>LTC1574/LTC1574-3.3/LTC1574-5</td>
<td>High Efficiency Step-Down DC/DC Converters with Internal Schottky Diode</td>
<td>LTC1174 with Internal Schottky Diode</td>
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<tr>
<td>LTC1622</td>
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<tr>
<td>LTC1624</td>
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<td>95% DC, 3.5V to 36V VIN</td>
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<td>LT**1761 Series</td>
<td>100mA, Low Noise, LDO Micropower Regulators in SOT-23</td>
<td>20μA Quiescent Current, 20μVRMS Noise</td>
</tr>
<tr>
<td>LT1763 Series</td>
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<td>30μA Quiescent Current, 20μVRMS Noise</td>
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<tr>
<td>LTC1772</td>
<td>Constant Frequency Step-Down DC/DC Controller</td>
<td>SOT-23, 2.2V to 9.8V VIN</td>
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<tr>
<td>LTC1877</td>
<td>High Efficiency Monolithic Step-Down Regulator</td>
<td>550kHz, MS8, VIN Up to 10V, IQ = 10μA, IOUT to 600mA</td>
</tr>
<tr>
<td>LTC1878</td>
<td>High Efficiency Monolithic Step-Down Regulator</td>
<td>550kHz, MS8, VIN Up to 6V, IQ = 10μA, IOUT to 600mA</td>
</tr>
</tbody>
</table>

**NOTES:***
- VIN: 2.8V to 12V
- VOUT: 5V ± 1A
- MODE: RUN/SS
- GND: 0V
- PGATE: 3.3V
- VIN (V): 2.8, 3.3, 5, 7.5, 10, 12
- ILOAD(MAX) (A): 0.8, 1.1, 1.7, 2.3, 2.7, 2.9

**COMPONENTS:**
- C0: AVX TPSD338M020R0200
- COUT: SANYO POSCAP 10TPB100M
- C1: AVX TPSD107M010R065
- D1: MICROSEMI UPS817
- L1A, L1B: COILTRONICS CTX10-4, BH ELECTRONICS S10-1013

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**SHARP THROTTLE**: LTC1771 1000pF

**SHARP THROTTLE**: LTC1771 TA03

**SHARP THROTTLE**: LTC1772 1000pF

**SHARP THROTTLE**: LTC1771 1000pF

**SHARP THROTTLE**: LTC1771 TA03

**SHARP THROTTLE**: LTC1772 1000pF