FEATURES

- 90MHz Gain Bandwidth, f = 100kHz
- 22V/µs Slew Rate
- Settling Time: 900ns (AV = –1, 150µV, 10V Step)
- Low Distortion, –96.5dB for 100kHz, 10VP-P
- Maximum Input Offset Voltage: 75µV
- Maximum Input Offset Voltage Drift: 2µV/°C
- Maximum (–) Input Bias Current: 10nA
- Minimum DC Gain: 1000V/mV
- Minimum Output Swing into 2k: ±12.8V
- Unity Gain Stable
- Input Noise Voltage: 5nV/√Hz
- Input Noise Current: 0.6pA/√Hz
- Total Input Noise Optimized for 1k < R_S < 20k
- Specified at ±5V and ±15V

APPLICATIONS

- 16-Bit DAC Current-to-Voltage Converter
- Precision Instrumentation
- ADC Buffer
- Low Distortion Active Filters
- High Accuracy Data Acquisition Systems
- Photodiode Amplifiers

DESCRIPTION

The LT®1468 is a precision high speed operational amplifier with 16-bit accuracy and 900ns settling to 150µV for 10V signals. This unique blend of precision and AC performance makes the LT1468 the optimum choice for high accuracy applications such as DAC current-to-voltage conversion and ADC buffers. The initial accuracy and drift characteristics of the input offset voltage and inverting input bias current are tailored for inverting applications.

The 90MHz gain bandwidth ensures high open-loop gain at frequency for reducing distortion. In noninverting applications such as an ADC buffer, the low distortion and DC accuracy allow full 16-bit AC and DC performance.

The 22V/µs slew rate of the LT1468 improves large-signal performance in applications such as active filters and instrumentation amplifiers compared to other precision op amps.

The LT1468 is manufactured on a complementary bipolar process. It is available in a space saving 3mm × 3mm leadless package, as well as small outline and DIP packages.

**TYPICAL APPLICATION**

16-Bit DAC I-to-V Converter

OFFSET: V_OS + I_B (6kΩ) < 1LSB
SETTLING TIME TO 150µV = 1.7µs
SETTLING LIMITED BY 6k AND 20pF TO COMPENSATE DAC OUTPUT CAPACITANCE
**LT1468**

**ABSOLUTE MAXIMUM RATINGS (Note 1)**

- Total Supply Voltage ($V^+\text{ to } V^-$).................................36V
- Maximum Input Current (Note 2)................................10mA
- Output Short-Circuit Duration (Note 3)............ Indefinite
- Operating Temperature Range ................. –40°C to 85°C

**ORDER INFORMATION**

<table>
<thead>
<tr>
<th>LEAD FREE FINISH</th>
<th>TAPE AND REEL</th>
<th>PART MARKING*</th>
<th>PACKAGE DESCRIPTION</th>
<th>SPECIFIED TEMPERATURE RANGE</th>
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<tr>
<td>LT1468CN8#PBF</td>
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<td>0°C to 70°C</td>
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</tr>
</tbody>
</table>

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: [http://www.linear.com/leadfree/](http://www.linear.com/leadfree/)

For more information on tape and reel specifications, go to: [http://www.linear.com/tapeandreel/](http://www.linear.com/tapeandreel/)
## Electrical Characteristics

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ C$. $V_{CM} = 0V$ unless otherwise noted.

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<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
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<td>$V_{OS}$</td>
<td>Input Offset Voltage</td>
<td>N8, S8</td>
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<td>Input Offset Current</td>
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<td>$I_{B^-}$</td>
<td>Inverting Input Bias Current</td>
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<td>Noninverting Input Bias Current</td>
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<td>Input Noise Voltage</td>
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<td>Input Resistance</td>
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<td>Common Mode Rejection Ratio</td>
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<td>$V_{CM} = \pm 2.5V$</td>
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<td>PSRR</td>
<td>Power Supply Rejection Ratio</td>
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<td>Large-Signal Voltage Gain</td>
<td>$V_{OUT} = \pm 12.5V$</td>
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<td>$R_L = 10k$</td>
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<td>5000</td>
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<td>$R_L = 2k$</td>
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<td>$R_L = 2k$</td>
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<td>$R_L = 10k$</td>
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<td>150</td>
<td>$\Omega$</td>
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<td>$\mu V$</td>
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<td>$V_{OUT}$</td>
<td>Output Swing</td>
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<td>$\mu V$</td>
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<td></td>
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<td>150</td>
<td>$\mu V$</td>
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<td></td>
<td>$R_L = 10k$</td>
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<td>mA</td>
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<td>$\pm 22$</td>
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<td>$I_{OUT}$</td>
<td>Output Current</td>
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<td>$\pm 15$</td>
<td>mA</td>
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<td>$V_{OUT} = \pm 2.5V$</td>
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<td>$\pm 40$</td>
<td>mA</td>
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<tr>
<td>$I_{SC}$</td>
<td>Short-Circuit Current</td>
<td>$V_{OUT} = 0V, V_{IN} = \pm 0.2V$</td>
<td>$15V$</td>
<td>$\pm 25$</td>
<td>mA</td>
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<tr>
<td>SR</td>
<td>Slew Rate</td>
<td>$A = -1, R_L = 2k$ (Note 5)</td>
<td>$15V$</td>
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<td>$A = -1, R_L = 2k$ (Note 5)</td>
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<td>11</td>
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<td>Full-Power Bandwidth</td>
<td>$10V$ Peak, (Note 6)</td>
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<td>$3V$ Peak, (Note 6)</td>
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<td>GBW</td>
<td>Gain Bandwidth</td>
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<td>90</td>
<td>MHz</td>
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<td></td>
<td></td>
<td>$f = 100kHz, R_L = 2k$</td>
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<td>88</td>
<td>MHz</td>
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<td>THD</td>
<td>Total Harmonic Distortion</td>
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<td>$A = 2, V_o = 10VP_p, f = 1kHz$</td>
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<td>$t_{r}, t_{f}$</td>
<td>Rise Time, Fall Time</td>
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<td>$A = 1, 10%$ to $90%, 0.1V$</td>
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<td>%</td>
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<td>$A = 1, 0.1V$</td>
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<td>%</td>
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<td></td>
<td>$A = 1, 50% V_{IN}$ to $50% V_{OUT}, 0.1V$</td>
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<td>9</td>
<td>ns</td>
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<td></td>
<td></td>
<td>$A = 1, 50% V_{IN}$ to $50% V_{OUT}, 0.1V$</td>
<td>$15V$</td>
<td>10</td>
<td>ns</td>
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**ELECTRICAL CHARACTERISTICS**  
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<td>$R_O$</td>
<td>Output Resistance</td>
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<td>$I_S$</td>
<td>Supply Current</td>
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<td>$V_{OS}$</td>
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<td>Input Offset Current</td>
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<td>$I_{OS}'$</td>
<td>Inverting Input Bias Current</td>
</tr>
<tr>
<td>$I_{OS}''$</td>
<td>Noninverting Input Bias Current</td>
</tr>
<tr>
<td>CMRR</td>
<td>Common Mode Rejection Ratio</td>
</tr>
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<td>PSRR</td>
<td>Power Supply Rejection Ratio</td>
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<tr>
<td>$A_{VOL}$</td>
<td>Large-Signal Voltage Gain</td>
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<td>$V_{OUT}$</td>
<td>Output Swing</td>
</tr>
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<td>$I_{OUT}$</td>
<td>Output Current</td>
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<td>$I_{SC}$</td>
<td>Short-Circuit Current</td>
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<td>SR</td>
<td>Slew Rate</td>
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<td>GBW</td>
<td>Gain Bandwidth</td>
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<tr>
<td>$I_S$</td>
<td>Supply Current</td>
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The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ C$. $0^\circ C \leq T_A \leq 70^\circ C$, $V_{CM} = 0V$ unless otherwise noted.

### SYMBOL | PARAMETER | CONDITIONS | $V_{SUPPLY}$ | MIN | TYP | MAX | UNITS
---|---|---|---|---|---|---|---
$I_s$ | Settling Time | $10V$ Step, $0.01\%$, $A_V = -1$ | $\pm 15V$ | $760$ | $900$ | $770$ | $ns$
| | | $5V$ Step, $150\mu V$, $A_V = -1$ | $\pm 15V$ | $900$ | $ns$ | $ns$ | $ns$
| | $A_V = 1$, $f = 100kHz$ | $\pm 15V$ | $0.02$ | $\Omega$ | $\Omega$ | $\Omega$ | $\Omega$
$R_O$ | | $\pm 15V$ | $3.9$ | $5.2$ | $3.6$ | $5.0$ | $mA$
$I_S$ | Supply Current | $\pm 15V$ | $\Omega$ | $\Omega$ | $\Omega$ | $\Omega$ | $\Omega$

| SYMBOL | PARAMETER | CONDITIONS | $V_{SUPPLY}$ | MIN | TYP | MAX | UNITS
---|---|---|---|---|---|---|---
$V_{OS}$ | Input Offset Voltage | N8, S8 | $\pm 15V$ | $150$ | $250$ | $\mu V$ | $\mu V$
| | | LT1468A, DD Package | $\pm 15V$ | $150$ | $250$ | $\mu V$ | $\mu V$
| | | LT1468, DD Package | $\pm 15V$ | $300$ | $400$ | $\mu V$ | $\mu V$
$V_{OS}$ | Input Offset Voltage Drift | $\pm 5V$ to $\pm 15V$ | $0.7$ | $2.0$ | $\mu V/°C$ | $\mu V/°C$
$I_{OS}$ | Input Offset Current | $\pm 5V$ to $\pm 15V$ | $65$ | $\mu A$ | $\mu A$ | $\mu A$ | $\mu A$
| | | $\pm 5V$ to $\pm 15V$ | $60$ | $pA/°C$ | $pA/°C$ | $pA/°C$ | $pA/°C$
$I_{OS}'$ | Inverting Input Bias Current | $\pm 5V$ to $\pm 15V$ | $\pm 15$ | $nA$ | $nA$ | $nA$ | $nA$
$I_{OS}''$ | Noninverting Input Bias Current | $\pm 5V$ to $\pm 15V$ | $\pm 50$ | $mA$ | $mA$ | $mA$ | $mA$
CMRR | Common Mode Rejection Ratio | $V_{CM} = \pm 12.5V$ | $\pm 15V$ | $94$ | $94$ | $db$ | $db$
| | | $V_{CM} = \pm 2.5V$ | $\pm 5V$ | $\pm 50$ | $nA$ | $nA$ | $nA$
PSRR | Power Supply Rejection Ratio | $V_S = \pm 4.5V$ to $15V$ | $98$ | $dB$ | $dB$ | $dB$ | $dB$
$A_{VOL}$ | Large-Signal Voltage Gain | $V_{OUT} = \pm 12.5V$, $R_L = 10k$ | $\pm 15V$ | $500$ | $V/mV$ | $V/mV$
| | | $V_{OUT} = \pm 12.5V$, $R_L = 2k$ | $\pm 15V$ | $250$ | $V/mV$ | $V/mV$
| | | $V_{OUT} = \pm 2.5V$, $R_L = 10k$ | $\pm 5V$ | $500$ | $V/mV$ | $V/mV$
| | | $V_{OUT} = \pm 2.5V$, $R_L = 2k$ | $\pm 5V$ | $250$ | $V/mV$ | $V/mV$
$V_{OUT}$ | Output Swing | $R_L = 10k$ | $\pm 15V$ | $\pm 12.9$ | $V$ | $V$
| | | $R_L = 2k$ | $\pm 15V$ | $\pm 12.7$ | $V$ | $V$
| | | $R_L = 10k$ | $\pm 5V$ | $\pm 2.9$ | $V$ | $V$
| | | $R_L = 2k$ | $\pm 5V$ | $\pm 2.7$ | $V$ | $V$
$I_{OUT}$ | Output Current | $V_{OUT} = \pm 12.5V$ | $\pm 15V$ | $\pm 12.5$ | $mA$ | $mA$
| | | $V_{OUT} = \pm 2.5V$ | $\pm 5V$ | $\pm 12.5$ | $mA$ | $mA$
$I_{SC}$ | Short-Circuit Current | $V_{OUT} = 0V$, $V_{IM} = \pm 0.2V$ | $\pm 15V$ | $17$ | $mA$ | $mA$
SR | Slew Rate | $A_V = -1$, $R_L = 2k$ (Note 5) | $\pm 5V$ | $13$ | $V/\mu s$ | $V/\mu s$
| | | $\pm 5V$ | $9$ | $MHz$ | $MHz$
GBW | Gain Bandwidth | $f = 100kHz$, $R_L = 2k$ | $\pm 15V$ | $55$ | $MHz$ | $MHz$
| | | $\pm 5V$ | $50$ | $MHz$ | $MHz$
$I_S$ | Supply Current | $\pm 15V$ | $6.5$ | $mA$ | $mA$
| | | $\pm 5V$ | $6.3$ | $mA$ | $mA$
## ELECTRICAL CHARACTERISTICS

The • denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$, $-40°C \leq T_A \leq 85°C$, $V_{CM} = 0V$ unless otherwise noted.

### SYMBOL | PARAMETER | CONDITIONS | $V_{SUPPLY}$ | MIN | TYP | MAX | UNITS
--- | --- | --- | --- | --- | --- | --- | ---
$V_{OS}$ | Input Offset Voltage | N8, S8 | ±15V | 230 | 300 | μV | μV
| | | LT1468A, DD Package | ±15V | 230 | 300 | μV | μV
| | | LT1468, DD Package | ±15V | 400 | 500 | μV | μV

Input $V_{OS}$ Drift | (Note 7) | ±5V to ±15V | 0.7 | 2.5 | μV/°C

$I_{OS}$ | Input Offset Current | ±5V to ±15V | 80 | nA

Input Offset Current Drift | ±5V to ±15V | 120 | pA/°C

$I^+$ | Inverting Input Bias Current | ±5V to ±15V | ±30 | nA

Negative Input Current Drift | ±5V to ±15V | 80 | pA/°C

$I^-$ | Noninverting Input Bias Current | ±5V to ±15V | ±60 | nA

CMRR | Common Mode Rejection Ratio | $V_{CM} = ±12.5V$ | 92 | dB
| | | $V_{CM} = ±2.5V$ | 92 | dB

PSRR | Power Supply Rejection Ratio | $V_S = ±4.5V$ to ±15V | 96 | dB

$A_{VOL}$ | Large-Signal Voltage Gain | $V_{OUT} = ±12V$, $R_L = 10k$ | 300 | V/mV
| | | $V_{OUT} = ±10V$, $R_L = 2k$ | 150 | V/mV
| | | $V_{OUT} = ±2.5V$, $R_L = 10k$ | 300 | V/mV
| | | $V_{OUT} = ±2.5V$, $R_L = 2k$ | 150 | V/mV

$V_{OUT}$ | Output Swing | $R_L = 10k$ | ±15V | ±12.8 | V
| | | $R_L = 2k$ | ±15V | ±12.6 | V
| | | $R_L = 10k$ | ±5V | ±2.8 | V
| | | $R_L = 2k$ | ±5V | ±2.6 | V

$I_{OUT}$ | Output Current | $V_{OUT} = ±12.5V$ | ±15V | ±7 | mA
| | | $V_{OUT} = ±2.5V$ | ±5V | ±7 | mA

$I_{SC}$ | Short-Circuit Current | $V_{OUT} = 0V$, $V_{IN} = ±0.2V$ | ±15V | ±12 | mA

SR | Slew Rate | $A_V = -1$, $R_L = 2k$ (Note 5) | ±15V | 9 | V/μs
| | | ±5V | 6 | V/μs

GBW | Gain Bandwidth | $f = 100kHz$, $R_L = 2k$ | ±15V | 45 | MHz
| | | ±5V | 40 | MHz

$I_S$ | Supply Current | ±15V | 7.0 | mA
| | | ±5V | 6.8 | mA

### Notes:

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The inputs are protected by back-to-back diodes and two 100Ω series resistors. If the differential input voltage exceeds 0.7V, the input current should be limited to 10mA. Input voltages outside the supplies will be clamped by ESD protection devices and input currents should also be limited to 10mA.

**Note 3:** A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

**Note 4:** The LT1468C is guaranteed to meet specified performance from 0°C to 70°C and is designed, characterized and expected to meet these extended temperature limits, but is not tested at −40°C and at 85°C. The LT1468i is guaranteed to meet the extended temperature limits.

**Note 5:** Slew rate is measured between ±8V on the output with ±12V input for ±15V supplies and ±2V on the output with ±3V input for ±5V supplies.

**Note 6:** Full power bandwidth is calculated from the slew rate measurement: $FPBW = SR/2\pi f_P$.

**Note 7:** This parameter is not 100% tested.
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Supply Voltage and Temperature

Input Common Mode Range vs Supply Voltage

Input Bias Current vs Input Common Mode Voltage

Input Bias Current vs Temperature

Input Voltage Spectral Density

0.1Hz to 10Hz Voltage Noise

Warm-Up Drift vs Time

Open-Loop Gain vs Resistive Load

Open-Loop Gain vs Temperature
TYPICAL PERFORMANCE CHARACTERISTICS

Gain and Phase vs Frequency

Power Supply Rejection Ratio vs Frequency

Common Mode Rejection Ratio vs Frequency

Frequency Response vs Supply Voltage, AV = 1

Frequency Response vs Supply Voltage, AV = –1

Frequency Response vs Capacitive Load, AV = 1

Frequency Response vs Capacitive Load, AV = –1

Slew Rate vs Supply Voltage

Slew Rate vs Temperature
TYPICAL PERFORMANCE CHARACTERISTICS

Total Harmonic Distortion + Noise vs Frequency

- THD + Noise (%)
  - 0.010
  - 0.001
  - 0.0001
- Frequency (Hz)
  - 20
  - 100
  - 1k
  - 10k
  - 20k

Total Harmonic Distortion + Noise vs Amplitude

- THD + Noise (dB)
  - 0
  - –80
  - –100
  - –120
- Output Signal (V_rms)
  - 0.1
  - 1
  - 10
  - 100
  - 1k
  - 10k

Undistorted Output Swing vs Frequency, ±15V

- Output Voltage Swing (V_p-p)
  - 20
  - 25
  - 30
- Frequency (kHz)
  - 1
  - 10
  - 100
  - 1k
  - 10k
  - 100k

Small-Signal Transient, \( A_v = 1 \)

- Time (ms)
  - 20ms

Small-Signal Transient, \( A_v = -1 \)

- Time (ms)
  - 20ms

Large-Signal Transient, \( A_v = 1 \)

- Time (ms)
  - 20ms

Large-Signal Transient, \( A_v = -1 \)

- Time (ms)
  - 20ms

Total Noise vs Unmatched Source Resistance

- Total Noise
  - 10
  - 100
  - 1k
  - 10k
  - 100k
- Source Resistance, \( R_s (\Omega) \)
  - 0.1
  - 1
  - 10
  - 100
The LT1468 may be inserted directly into many operational amplifier applications improving both DC and AC performance, provided that the nulling circuitry is removed. The suggested nulling circuit for the LT1468 is shown below.

Make no connection to Pin 8. This pin is used for factory trim of the inverting input current.

The parallel combination of the feedback resistor and gain setting resistor on the inverting input can combine with the input capacitance to form a pole that can cause peaking or even oscillations. For feedback resistors greater than 2k, a feedback capacitor of the value:

\[ C_F > \frac{(R_G)(C_{IN}/R_F)}{ } \]

should be used to cancel the input pole and optimize dynamic performance. For applications where the DC noise gain is one, and a large feedback resistor is used, \( C_F \) should be greater than or equal to \( C_{IN} \). An example would be a DAC I-to-V converter as shown on the front page of this data sheet where the DAC can have many tens of pF of output capacitance. Another example would be a gain of \(-1\) with 5k resistors; a 5pF to 10pF capacitor should be added across the feedback resistor. The frequency response in a gain of \(-1\) is shown in the Typical Performance curves with 2k and 5.1k resistors with a 5pF feedback capacitor.

**Layout and Passive Components**

The LT1468 requires attention to detail in board layout in order to maximize DC and AC performance. For best AC results (for example fast settling time) use a ground plane, short lead lengths, and RF-quality bypass capacitors (0.01μF to 0.1μF) in parallel with low ESR bypass capacitors (1μF to 10μF tantalum). For best DC performance, use “star” grounding techniques, equalize input trace lengths and minimize leakage (i.e., 1.5GΩ of leakage between an input and a 15V supply will generate 10nA—equal to the maximum \( I_{B^-} \) specification.)

Board leakage can be minimized by encircling the input circuitry with a guard ring operated at a potential close to that of the inputs. For inverting configurations tie the ring to ground, in noninverting connections tie the ring to the inverting input (note the input capacitance will increase which may require a compensating capacitor as discussed below.)

Microvolt level error voltages can also be generated in the external circuitry. Thermocouple effects caused by temperature gradients across dissimilar metals at the contacts to the inputs can exceed the inherent drift of the amplifier. Air currents over device leads should be minimized, package leads should be short, and the two input leads should be as close together as possible and maintained at the same temperature.

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APPLICATIONS INFORMATION

Input Considerations

Each input of the LT1468 is protected with a 100Ω series resistor and back-to-back diodes across the bases of the input devices. If the inputs can be pulled apart, the input current should be limited to less than 10mA with an external series resistor. Each input also has two ESD clamp diodes—one to each supply. If an input is driven above the supply, limit the current with an external resistor to less than 10mA.

The LT1468 employs bias current cancellation at the inputs. The inverting input current is trimmed at zero common mode voltage to minimize errors in inverting applications such as I-to-V converters. The noninverting input current is not trimmed and has a wider variation and therefore a larger maximum value. As the input offset current can be greater than either input current, the use of balanced source resistance is NOT recommended as it actually degrades DC accuracy and also increases noise.

The input bias currents vary with common mode voltage as shown in the Typical Performance Characteristics. The cancellation circuitry was not designed to track this common mode voltage because the settling time would have been adversely affected.

The LT1468 inputs can be driven to the negative supply and to within 0.5V of the positive supply without phase reversal. As the input moves closer than 0.5V to the positive supply, the output reverses phase.

Total Input Noise

The curve of Total Noise vs Unmatched Source Resistance in the Typical Performance Characteristics shows that with source resistance below 1k, the voltage noise of the amplifier dominates. In the 1k to 20k region the increase in noise is due to the source resistance. Above 20k the input current noise component is larger than the resistor noise.

Capacitive Loading

The LT1468 drives capacitive loads of up to 100pF in unity gain and 300pF in a gain of –1. When there is a need to drive a larger capacitive load, a small series resistor should be inserted between the output and the load. In addition, a capacitor should be added between the output and the inverting input as shown in Driving Capacitive Loads.

Settling Time

The LT1468 is a single stage amplifier with an optimal thermal layout that leads to outstanding settling performance. Measuring settling, even at the 12-bit level is very challenging, and at the 16-bit level requires a great deal of subtlety and expertise. Fortunately, there are two excellent Linear Technology reference sources for settling measurements, Application Notes 47 and 74. Appendix B of AN47 is a vital primer on 12-bit settling measurements, and AN74 extends the state of the art while concentrating on settling time with a 16-bit current output DAC input.

Input Stage Protection

![Input Stage Protection Diagram]

Driving Capacitive Loads

![Driving Capacitive Loads Diagram]
APPLICATIONS INFORMATION

The 150μV settling curve in the Typical Performance Characteristics is measured using the Differential Amplifier method of AN74 followed by a clamped, nonsaturating gain of 100. The total gain of 500 allows a resolution of 100μV/DIV with an oscilloscope setting of 0.05V/DIV.

The settling of the DAC I-to-V converter on the front page was measured using the exact methods of AN74. The optimum nulling of the DAC output capacitance requires 20pF across the 6k feedback resistor. The theoretical limit for 16-bit settling is 11.1 times this RC time constant or 1.33μs. The actual settling time is 1.7μs at the output of the LT1468. The LT1468 is the fastest Linear Technology amplifier in this application.

The optional noise filter adds a slight delay of 100ns, but reduces the noise bandwidth to 1.6MHz which increases the output resolution for 16-bit accuracy.

Distortion

The LT1468 has outstanding distortion performance as shown in the Typical Performance curves of Total Harmonic Distortion + Noise vs Frequency and Amplitude. The high open-loop gain and inherently balanced architecture reduce errors to yield 16-bit accuracy to frequencies as high as 100kHz. An example of this performance is the Typical Application titled 100kHz Low Distortion Bandpass Filter. This circuit is useful for cleaning up the output of a high performance signal generator such as the B & K type 1051 or HP3326A.

Another key application for LT1468 is buffering the input to a 16-bit A/D converter. In a gain of 1 or 2 this straightforward circuit provides uncorrupted AC and DC levels to the converter, while buffering the A/D input sample-and-hold circuit from high source impedance which can reduce the maximum sampling rate. The front page graph shows better than 16-bit distortion for a gain of 2 with a 10VP-P output.

SIMPLIFIED SCHEMATIC
DD Package
8-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1698 Rev C)

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

Recommended Solder Pad Pitch and Dimensions
Apply Solder Mask to Areas That Are Not Soldered

Controlled Permits Copying and Distribution in the US only.

NON-CONTRACTUAL DOCUMENT—CURRENT As of 2022-09-16.
**PACKAGE DESCRIPTION**

### N8 Package

8-Lead PDIP (Narrow 0.300)

**PACKAGE DESCRIPTION**

**NOTE:**
1. DIMENSIONS ARE IN INCHES
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

### S8 Package

8-Lead Plastic Small Outline (Narrow 0.150)

**PACKAGE DESCRIPTION**

**NOTE:**
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)
# REVISION HISTORY
(Revision history begins at Rev B)

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<tr>
<th>REV</th>
<th>DATE</th>
<th>DESCRIPTION</th>
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<tr>
<td>B</td>
<td>10/09</td>
<td>Change to Both Packages in Pin Configuration</td>
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**Typical Applications**

**Instrumentation Amplifier**

\[
\text{GAIN = } \left[ \frac{R_4}{R_3} \right] \left[ 1 + \frac{1}{2} \left( \frac{R_2}{R_1} + \frac{R_3}{R_4} \right) \right] = 102
\]

TRIM R5 FOR GAIN

TRIM R1 FOR COMMON MODE REJECTION

BW = 480kHz

**100kHz Low Distortion Bandpass Filter**

100kHz Distortion

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<thead>
<tr>
<th>SIGNAL LEVEL</th>
<th>RL</th>
<th>2ND HARMONIC</th>
<th>3RD HARMONIC</th>
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<tr>
<td>1VRMS</td>
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<td>3.5VRMS</td>
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**RELATED PARTS**

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<tr>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
<th>COMMENTS</th>
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<tr>
<td>LT1167</td>
<td>Precision Instrumentation Amplifier</td>
<td>Single Resistor Gain Set, 0.04% Max Gain Error, 10ppm Max Gain Nonlinearity</td>
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<tr>
<td>LTC1595/LTC1596</td>
<td>16-Bit Serial Multiplying I\textsubscript{OUT} DACs</td>
<td>±1LSB Max INL/DNL, Low Glitch, DAC8043 16-Bit Upgrade</td>
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<tr>
<td>LTC1597</td>
<td>16-Bit Parallel Multiplying I\textsubscript{OUT} DAC</td>
<td>±1LSB Max INL/DNL, Low Glitch, On-Chip Bipolar Resistors</td>
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<tr>
<td>LTC1604</td>
<td>16-Bit, 333ksps Sampling ADC</td>
<td>±2.5V Input, SINAD = 90dB, THD = –100dB</td>
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<tr>
<td>LTC1605</td>
<td>Single 5V, 16-Bit, 100ksps Sampling ADC</td>
<td>Low Power, ±10V Inputs, Parallel/Byte Interface</td>
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<tr>
<td>LT1469</td>
<td>Dual 90MHz 16-Bit Accurate Op Amp</td>
<td>Dual Version of LT1468</td>
</tr>
<tr>
<td>LT1800</td>
<td>80MHz, 25V/μs Low Power Rail-to-Rail Precision Op Amp</td>
<td>( V_S \leq \pm 5V, I_{CC} = 1.6mA, V_{DS} \leq 350\mu V )</td>
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<td>LT6220</td>
<td>60MHz, 20V/μs Low Power Rail-to-Rail Precision Op Amp</td>
<td>( V_S \leq \pm 5V, I_{CC} = 0.9mA, V_{DS} \leq 350\mu V )</td>
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<tr>
<td>LT1722</td>
<td>200MHz, 70V/μs Low Noise Precision Op Amp</td>
<td>( V_S \leq \pm 5V, e_n = 3.8nV/\sqrt{Hz}, –85dBc at 1MHz )</td>
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<tr>
<td>LTC6244HV</td>
<td>Dual 50MHz, Low Noise, Precision CMOS Op Amp</td>
<td>( V_S \leq \pm 5V, V_{DS} \leq 100\mu V, I_B \leq 75pA )</td>
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