The LTC®1435 is a synchronous step-down switching regulator controller that drives external N-channel power MOSFETs using a fixed frequency architecture. Burst Mode™ operation provides high efficiency at low load currents. A maximum duty cycle limit of 99% provides low dropout operation which extends operating time in battery-operated systems.

The operating frequency is set by an external capacitor allowing maximum flexibility in optimizing efficiency. A secondary winding feedback control pin, SFB, guarantees regulation regardless of load on the main output by forcing continuous operation. Burst Mode operation is inhibited when the SFB pin is pulled low which reduces noise and RF interference.

Soft start is provided by an external capacitor which can be used to properly sequence supplies. The operating current level is user-programmable via an external current sense resistor. Wide input supply range allows operation from 3.5V to 30V (36V maximum).

APPLICATIONS
- Notebook and Palmtop Computers, PDAs
- Cellular Telephones and Wireless Modems
- Portable Instruments
- Battery-Operated Devices
- DC Power Distribution Systems
**LTC1435**

**ABSOLUTE MAXIMUM RATINGS**

- Input Supply Voltage ($V_{IN}$) ......................... 36V to –0.3V
- Topside Driver Supply Voltage (Boost) ...... 42V to –0.3V
- Switch Voltage (SW) ........................................ $V_{IN} + 5V$ to –5V
- $V_{EXTVCC}$ Voltage ........................................ 10V to –0.3V
- Sense+, Sense– Voltages .......... $INTVCC + 0.3V$ to –0.3V
- $I_{TH}, V_{OSENSE}$ Voltages .............................. 2.7V to –0.3V
- SFB, Run/SS Voltages .............................. 10V to –0.3V
- Peak Driver Output Current < 10µs (TG, BG) ............. 2A
- $V_{EXTVCC}$ Output Current ........................................ 50mA
- Operating Ambient Temperature Range
  - LTC1435C............................................... 0°C to 70°C
  - LTC1435I............................................ –40°C to 85°C
- Junction Temperature (Note 1) ..................... 125°C
- Storage Temperature Range ................. –65°C to 150°C
- Lead Temperature (Soldering, 10 sec) .......... 300°C

**PACKAGE/ORDER INFORMATION**

- Order Part Number
- LTC1435CG
- LTC1435CS
- LTC1435iG
- LTC1435iS

**ELECTRICAL CHARACTERISTICS**

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Consult factory for Military grade parts.
**ELECTRICAL CHARACTERISTICS**

The ● denotes specifications which apply over the full operating temperature range.

- LTC1435CG/LTC1435CS: 0°C ≤ T_A ≤ 70°C
- LTC1435IG/LTC1435IS: −40°C ≤ T_A ≤ 85°C

**Note 1:** T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

LTC1435CG/LTC1435IG: T_J = T_A + (P_D)(130°C/W)
LTC1435CS/LTC1435IS: T_J = T_A + (P_D)(110°C/W)

**Note 2:** The LTC1435 is tested in a feedback loop which servos V_OSENSE to the balance point for the error amplifier (V_TH = 1.19V).

**Note 3:** Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Applications Information.

**Note 4:** Oscillator frequency is tested by measuring the C_OSC charge and discharge currents and applying the formula:

\[ f_{OSC} (kHz) = \left( \frac{8.4(10^9)}{C_{OSC} (PF)} + 1 \right) \left( \frac{1}{I_{CHG}} + \frac{1}{I_{DIS}} \right)^{-1} \]

**TYPICAL PERFORMANCE CHARACTERISTICS**

**Efficiency vs Input Voltage**

- V_OUT = 3.3V
- V_OUT = 5V

**V_IN – V_OUT Dropout Voltage vs Load Current**

- RSENSE = 0.033Ω
- V_OUT DROP OF 5%

**Load Regulation**

- V_IN = 10V
- V_OUT = 5V
- RSENSE = 0.033Ω

**V_TH Pin Voltage vs Output Current**

- Burst Mode OPERATION
- CONTINUOUS MODE

**TA = 25°C, V_IN = 15V, V_RUN/SS = 5V unless otherwise noted.**
TYPICAL PERFORMANCE CHARACTERISTICS

Input Supply and Shutdown Current vs Input Voltage

INTVCC Regulation vs INTVCC Load Current

EXTVCC Switch Drop vs INTVCC Load Current

Normalized Oscillator Frequency vs Temperature

RUN/SS Pin Current vs Temperature

SFB Pin Current vs Temperature

Maximum Current Sense Threshold Voltage vs Temperature

Transient Response

Transient Response
TYPICAL PERFORMANCE CHARACTERISTICS

PIN FUNCTIONS

COSC (Pin 1): External capacitor COSC from this pin to ground sets the operating frequency.

RUN/SS (Pin 2): Combination of Soft Start and Run Control Inputs. A capacitor to ground at this pin sets the ramp time to full current output. The time is approximately 0.5s/μF. Forcing this pin below 1.3V causes the device to be shut down. In shutdown all functions are disabled.

ITH (Pin 3): Error Amplifier Compensation Point. The current comparator threshold increases with this control voltage. Nominal voltage range for this pin is 0V to 2.5V.

SFB (Pin 4): Secondary Winding Feedback Input. Normally connected to a feedback resistive divider from the secondary winding. This pin should be tied to: ground to force continuous operation; INTVCC in applications that don’t use a secondary winding; and a resistive divider from the output in applications using a secondary winding.

SGND (Pin 5): Small-Signal Ground. Must be routed separately from other grounds to the (–) terminal of COUT.

VSENSE (Pin 6): Receives the feedback voltage from an external resistive divider across the output.

SENSE– (Pin 7): The (–) Input to the Current Comparator.

SENSE+ (Pin 8): The (+) Input to the Current Comparator. Built-in offsets between SENSE– and SENSE+ pins in conjunction with RSENSE set the current trip thresholds.

EXTVCC (Pin 9): Input to the Internal Switch Connected to INTVCC. This switch closes and supplies VCC power whenever EXTVCC is higher than 4.7V. See EXTVCC connection in Applications Information section. Do not exceed 10V on this pin. Connect to VOUT if VOUT ≥ 5V.

PGND (Pin 10): Driver Power Ground. Connects to source of bottom N-channel MOSFET and the (–) terminal of CIN.

BG (Pin 11): High Current Gate Drive for Bottom N-Channel MOSFET. Voltage swing at this pin is from ground to INTVCC.

INTVCC (Pin 12): Output of the Internal 5V Regulator and EXTVCC Switch. The driver and control circuits are powered from this voltage. Must be closely decoupled to power ground with a minimum of 2.2µF tantalum or electrolytic capacitor.

VIN (Pin 13): Main Supply Pin. Must be closely decoupled to the IC’s signal ground pin.

SW (Pin 14): Switch Node Connection to Inductor. Voltage swing at this pin is from a Schottky diode (external) voltage drop below ground to VIN.

BOOST (Pin 15): Supply to Topside Floating Driver. The bootstrap capacitor is returned to this pin. Voltage swing at this pin is from INTVCC to VIN + INTVCC.

TG (Pin 16): High Current Gate Drive for Top N-Channel MOSFET. This is the output of a floating driver with a voltage swing equal to INTVCC superimposed on the switch node voltage SW.
Operation
(Refer to Functional Diagram)

Main Control Loop

The LTC1435 uses a constant frequency, current mode step-down architecture. During normal operation, the top MOSFET is turned on each cycle when the oscillator sets the RS latch, and turned off when the main current comparator I1 resets the RS latch. The peak inductor current at which I1 resets the RS latch is controlled by the voltage on the ITH pin, which is the output of error amplifier EA. The VSENSE pin, described in the Pin Functions section, allows EA to receive an output feedback voltage VFB from an external resistive divider. When the load current increases, it causes a slight decrease in VFB relative to the 1.19V reference, which in turn causes the ITH voltage to increase until the average inductor current matches the new load current. While the top MOSFET is off, the bottom MOSFET is turned on until either the inductor current starts to reverse, as indicated by current comparator I2, or the beginning of the next cycle.

The top MOSFET driver is biased from floating bootstrap capacitor CB, which normally is recharged during each off cycle. However, when VIN decreases to a voltage close to VOUT, the loop may enter dropout and attempt to turn on the top MOSFET continuously. The dropout detector counts the number of oscillator cycles that the top MOSFET remains on and periodically forces a brief off period to allow CB to recharge.

The main control loop is shut down by pulling the RUN/SS pin low. Releasing RUN/SS allows an internal 3μA current source to charge soft start capacitor CSS. When CSS reaches 1.3V, the main control loop is enabled with the ITH voltage clamped at approximately 30% of its maximum value. As CSS continues to charge, ITH is gradually released allowing normal operation to resume.

Comparator OV guards against transient overshoots > 7.5% by turning off the top MOSFET and keeping it off until the fault is removed.

Low Current Operation

The LTC1435 is capable of Burst Mode operation in which the external MOSFETs operate intermittently based on load demand. The transition to low current operation begins when comparator I2 detects current reversal and turns off the bottom MOSFET. If the voltage across RSENSE does not exceed the hysteresis of I2 (approximately 20mV) for one full cycle, then on following cycles the top and bottom drives are disabled. This continues until an inductor current peak exceeds 20mV/RSENSE or the ITH voltage exceeds 0.6V, either of which causes drive to be returned to the TG pin on the next cycle.

Two conditions can force continuous synchronous operation, even when the load current would otherwise dictate low current operation. One is when the common mode voltage of the SENSE+ and SENSE− pins is below 1.4V and the other is when the SFB pin is below 1.19V. The latter condition is used to assist in secondary winding regulation as described in the Applications Information section.

INTVCC/EXTVCC Power

Power for the top and bottom MOSFET drivers and most of the other LTC1435 circuitry is derived from the INTVCC pin. The bottom MOSFET driver supply pin is internally connected to INTVCC in the LTC1435. When the EXTVCC pin is open, an internal 5V low dropout regulator supplies INTVCC power. If EXTVCC is taken above 4.8V, the 5V regulator is turned off and an internal switch is turned on to connect EXTVCC to INTVCC. This allows the INTVCC power to be derived from a high efficiency external source such as the output of the regulator itself or a secondary winding, as described in the Applications Information section.
The basic LTC1435 application circuit is shown in Figure 1, High Efficiency Step-Down Converter. External component selection is driven by the load requirement and begins with the selection of R\text{SENSE}. Once R\text{SENSE} is known, C\text{OSC} and L can be chosen. Next, the power MOSFETs and D1 are selected. Finally, C\text{IN} and C\text{OUT} are selected. The circuit shown in Figure 1 can be configured for operation up to an input voltage of 28V (limited by the external MOSFETs).

**R\text{SENSE} Selection for Output Current**

R\text{SENSE} is chosen based on the required output current. The LTC1435 current comparator has a maximum threshold of 150mV/R\text{SENSE} and an input common mode range of SGND to INTV\text{CC}. The current comparator threshold sets the peak of the inductor current, yielding a maximum average output current I\text{MAX} equal to the peak value less half the peak-to-peak ripple current \(\Delta I_L\).

Allowing a margin for variations in the LTC1435 and external component values yields:

\[
R\text{SENSE} = \frac{100\text{mV}}{I\text{MAX}}
\]

The LTC1435 works well with values of R\text{SENSE} from 0.005\text{Ω} to 0.2\text{Ω}.

**C\text{OSC} Selection for Operating Frequency**

The LTC1435 uses a constant frequency architecture with the frequency determined by an external oscillator capacitor C\text{OSC}. Each time the topside MOSFET turns on, the voltage C\text{OSC} is reset to ground. During the on-time, C\text{OSC} is charged by a fixed current. When the voltage on the capacitor reaches 1.19V, C\text{OSC} is reset to ground. The process then repeats.

The value of C\text{OSC} is calculated from the desired operating frequency:

\[
C\text{OSC} (\text{pF}) = \left[ \frac{1.37 \times 10^4}{\text{Frequency (kHz)}} \right] - 11
\]

A graph for selecting C\text{OSC} vs frequency is given in Figure 2. As the operating frequency is increased the gate charge losses will be higher, reducing efficiency (see Efficiency Considerations). The maximum recommended switching frequency is 400kHz.

**Inductor Value Calculation**

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. So why would anyone ever choose to operate at lower frequencies with larger components? The answer is efficiency. A higher frequency generally results in lower efficiency because of MOSFET gate charge losses. In addition to this basic trade-off, the effect of inductor value on ripple current and low current operation must also be considered.

The inductor value has a direct effect on ripple current. The inductor ripple current \(\Delta I_L\) decreases with higher inductance or frequency and increases with higher \(V_{IN}\) or \(V_{OUT}\):

\[
\Delta I_L = \frac{1}{(f)(L)} V_{OUT} \left(1 - \frac{V_{OUT}}{V_{IN}}\right)
\]

Accepting larger values of \(\Delta I_L\) allows the use of low inductances, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is \(\Delta I_L = 0.4(I\text{MAX})\). Remember, the maximum \(\Delta I_L\) occurs at the maximum input voltage.

The inductor value also has an effect on low current operation. The transition to low current operation begins when the inductor current reaches zero while the bottom
MOSFET is on. Lower inductor values (higher $\Delta L$) will cause this to occur at higher load currents, which can cause a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductance values will cause the burst frequency to decrease.

The Figure 3 graph gives a range of recommended inductor values vs operating frequency and $V_{OUT}$.

![Figure 3. Recommended Inductor Values](image)

**Figure 3. Recommended Inductor Values**

### Inductor Core Selection

Once the value for $L$ is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite, molypermalloy or Kool Mu® cores. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates “hard,” which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. **Do not allow the core to saturate!**

Molypermalloy (from Magnetics, Inc.) is a very good, low loss core material for toroids, but it is more expensive than ferrite. A reasonable compromise from the same manufacturer is Kool Mu. Toroids are very space efficient, especially when you can use several layers of wire. Because they generally lack a bobbin, mounting is more difficult. However, designs for surface mount are available which do not increase the height significantly.

### Power MOSFET and D1 Selection

Two external power MOSFETs must be selected for use with the LTC1435: an N-channel MOSFET for the top (main) switch and an N-channel MOSFET for the bottom (synchronous) switch.

The peak-to-peak gate drive levels are set by the INTVCC voltage. This voltage is typically 5V during start-up (see EXTVCC Pin Connection). Consequently, logic level threshold MOSFETs must be used in most LTC1435 applications. The only exception is applications in which EXTVCC is powered from an external supply greater than 8V (must be less than 10V), in which standard threshold MOSFETs ($V_{GS(TH)} < 4V$) may be used. Pay close attention to the $BV_{DSS}$ specification for the MOSFETs as well; many of the logic level MOSFETs are limited to 30V or less.

Selection criteria for the power MOSFETs include the “ON” resistance $R_{SD(ON)}$, reverse transfer capacitance $C_{RSS}$, input voltage and maximum output current. When the LTC1435 is operating in continuous mode the duty cycles for the top and bottom MOSFETs are given by:

$$
\text{Main Switch Duty Cycle} = \frac{V_{OUT}}{V_{IN}}
$$

$$
\text{Synchronous Switch Duty Cycle} = \frac{(V_{IN} - V_{OUT})}{V_{IN}}
$$

The MOSFET power dissipations at maximum output current are given by:

$$
P_{\text{MAIN}} = \frac{V_{OUT}}{V_{IN}} (I_{MAX})^2 (1 + \delta) R_{DS(ON)} + k(V_{IN})^{1.85} (I_{MAX})(C_{RSS})(f)
$$

$$
P_{\text{SYNC}} = \frac{V_{IN} - V_{OUT}}{V_{IN}} (I_{MAX})^2 (1 + \delta) R_{DS(ON)}
$$

---

Kool Mu® is a registered trademark of Magnetics, Inc.
where $\delta$ is the temperature dependency of $R_{DS(ON)}$ and $k$ is a constant inversely related to the gate drive current.

Both MOSFETs have $I^2R$ losses while the topology N-channel equation includes an additional term for transition losses, which are highest at high input voltages. For $V_{IN} < 20V$ the high current efficiency generally improves with larger MOSFETs, while for $V_{IN} > 20V$ the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower $C_{RSS}$ actually provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage or during a short circuit when the duty cycle in this switch is nearly 100%. Refer to the Foldback Current Limiting section for further applications information.

The term $(1 + \delta)$ is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs Temperature curve, but $\delta = 0.005/°C$ can be used as an approximation for low voltage MOSFETs. $C_{RSS}$ is usually specified in the MOSFET characteristics. The constant $k = 2.5$ can be used to estimate the contributions of the two terms in the main switch dissipation equation.

The Schottky diode D1 shown in Figure 1 conducts during the dead-time between the conduction of the two large power MOSFETs. This prevents the body diode of the bottom MOSFET from turning on and storing charge during the dead-time, which could cost as much as 1% in efficiency. A 1A Schottky is generally a good size for 3A regulators.

$C_{IN}$ and $C_{OUT}$ Selection

In continuous mode, the source current of the top N-channel MOSFET is a square wave of duty cycle $V_{OUT}/V_{IN}$. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN \ required} \ I_{RMS} = I_{MAX} \left[\frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN}}\right]^{1/2}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturer’s ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor or to choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. Always consult the manufacturer if there is any question.

The selection of $C_{OUT}$ is driven by the required effective series resistance (ESR). Typically, once the ESR requirement is satisfied the capacitance is adequate for filtering. The output ripple ($\Delta V_{OUT}$) is approximated by:

$$\Delta V_{OUT} \approx \Delta I_{L} \left(ESR + \frac{1}{4fC_{OUT}}\right)$$

where $f$ = operating frequency, $C_{OUT}$ = output capacitance and $\Delta I_{L}$ = ripple current in the inductor. The output ripple is highest at maximum input voltage since $\Delta I_{L}$ increases with input voltage. With $\Delta I_{L} = 0.4I_{OUT(MAX)}$ the output ripple will be less than 100mV at max $V_{IN}$ assuming:

$$C_{OUT \ required} \ ESR < 2R_{SENSE}$$

Manufacturers such as Nichicon, United Chemicon and Sanyo should be considered for high performance through-hole capacitors. The OS-CON semiconductor dielectric capacitor available from Sanyo has the lowest ESR(size) product of any aluminum electrolytic at a somewhat higher price. Once the ESR requirement for $C_{OUT}$ has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement.

In surface mount applications multiple capacitors may have to be paralleled to meet the ESR or RMS current handling requirements of the application. Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface mount tantalum, available in case heights ranging from 2mm to 4mm. Other capacitor types include Sanyo OS-CON, Nichicon PL series and Sprague 593D and 595D series. Consult the manufacturer for other specific recommendations.
APPLICATIONS INFORMATION

INTVCC Regulator

An internal P-channel low dropout regulator produces the 5V supply which powers the drivers and internal circuitry within the LTC1435. The INTVCC pin can supply up to 15mA and must be bypassed to ground with a minimum of 2.2μF tantalum or low ESR electrolytic. Good bypassing is necessary to supply the high transient currents required by the MOSFET gate drivers.

High input voltage applications, in which large MOSFETs are being driven at high frequencies, may cause the maximum junction temperature rating for the LTC1435 to be exceeded. The IC supply current is dominated by the gate charge supply current when not using an output derived EXTVCC source. The gate charge is dependent on operating frequency as discussed in the Efficiency Considerations section. The junction temperature can be estimated by using the equations given in Note 1 of the Electrical Characteristics. For example, the LTC1435 is limited to less than 17mA from a 30V supply:

\[ T_J = 70°C + (17mA)(30V)(100°C/W) = 126°C \]

To prevent maximum junction temperature from being exceeded, the input supply current must be checked when operating in continuous mode at maximum \( V_{IN} \).

EXTVCC Connection

The LTC1435 contains an internal P-channel MOSFET switch connected between the EXTVCC and INTVCC pins. The switch closes and supplies the INTVCC power whenever the EXTVCC pin is above 4.8V, and remains closed until EXTVCC drops below 4.5V. This allows the MOSFET driver and control power to be derived from the output during normal operation (4.8V < \( V_{OUT} < 9V \)) and from the internal regulator when the output is out of regulation (start-up, short circuit). Do not apply greater than 10V to the EXTVCC pin and ensure that EXTVCC \( \leq V_{IN} \).

Significant efficiency gains can be realized by powering INTVCC from the output, since the \( V_{IN} \) current resulting from the driver and control currents will be scaled by a factor of Duty Cycle/Efficiency. For 5V regulators this supply means connecting the EXTVCC pin directly to \( V_{OUT} \). However, for 3.3V and other lower voltage regulators, additional circuitry is required to derive INTVCC power from the output.

The following list summarizes the four possible connections for EXTVCC:

1. EXTVCC left open (or grounded). This will cause INTVCC to be powered from the internal 5V regulator resulting in an efficiency penalty of up to 10% at high input voltages.

2. EXTVCC connected directly to \( V_{OUT} \). This is the normal connection for a 5V regulator and provides the highest efficiency.

3. EXTVCC connected to an output-derived boost network. For 3.3V and other low voltage regulators, efficiency gains can still be realized by connecting EXTVCC to an output-derived voltage which has been boosted to greater than 4.8V. This can be done with either the inductive boost winding as shown in Figure 4a or the capacitive charge pump shown in Figure 4b. The charge pump has the advantage of simple magnetics.

4. EXTVCC connected to an external supply. If an external supply is available in the 5V to 10V range (EXTVCC \( \leq V_{IN} \)), it may be used to power EXTVCC providing it is compatible with the MOSFET gate drive requirements. When driving standard threshold MOSFETs, the external supply must always be present during operation to prevent MOSFET failure due to insufficient gate drive.

![Figure 4a. Secondary Output Loop and EXTVCC Connection](LTC1435+1904a)
**Topside MOSFET Driver Supply (C_B, D_B)**

An external bootstrap capacitor C_B connected to the Boost pin supplies the gate drive voltage for the topside MOSFET. Capacitor C_B in the Functional Diagram is charged through diode D_B from INTVCC when the SW pin is low. When the topside MOSFET is to be turned on, the driver places the C_B voltage across the gate source of the MOSFET. This enhances the MOSFET and turns on the topside switch. The switch node voltage SW rises to VIN and the Boost pin rises to VIN + INTVCC. The value of the boost capacitor C_B needs to be 100 times greater than the total input capacitance of the topside MOSFET. In most applications 0.1 µF is adequate. The reverse breakdown on D_B must be greater than V_IN(MAX).

**Output Voltage Programming**

The output voltage is set by a resistive divider according to the following formula:

\[
V_{OUT} = 1.19V \left( 1 + \frac{R2}{R1} \right)
\]

The external resistor divider is connected to the output as shown in Figure 5 allowing remote voltage sensing.

**Run/Soft Start Function**

The RUN/SS pin is a dual purpose pin which provides the soft start function and a means to shut down the LTC1435.

Soft start reduces surge currents from V_IN by gradually increasing the internal current limit. Power supply sequencing can also be accomplished using this pin.

An internal 3µA current source charges up an external capacitor C_SS. When the voltage on RUN/SS reaches 1.3V the LTC1435 begins operating. As the voltage on RUN/SS continues to ramp from 1.3V to 2.4V, the internal current limit is also ramped at a proportional linear rate. The current limit begins at approximately 50mV/R_SENSE (at V_RUN/SS = 1.3V) and ends at 150mV/R_SENSE (V_RUN/SS ≥ 2.7V). The output current thus ramps up slowly, charging the output capacitor. If RUN/SS has been pulled all the way to ground there is a delay before starting of approximately 500ms/µF, followed by an additional 500ms/µF to reach full current.

\[
t_{DELAY} = 5(10^5)C_{SS}\text{ Seconds}
\]

Pulling the RUN/SS pin below 1.3V puts the LTC1435 into a low quiescent current shutdown (IQ < 25µA). This pin can be driven directly from logic as shown in Figure 6. Diode D1 in Figure 6 reduces the start delay but allows C_SS to ramp up slowly for the soft start function; this diode and C_SS can be deleted if soft start is not needed. The RUN/SS pin has an internal 6V Zener clamp (See Functional Diagram).
APPLICATIONS INFORMATION

Foldback Current Limiting

As described in Power MOSFET and D1 Selection, the worst-case dissipation for either MOSFET occurs with a short-circuited output, when the synchronous MOSFET conducts the current limit value almost continuously. In most applications this will not cause excessive heating, even for extended fault intervals. However, when heat sinking is at a premium or higher \( R_{DS(ON)} \) MOSFETs are being used, foldback current limiting should be added to reduce the current in proportion to the severity of the fault.

Foldback current limiting is implemented by adding diode \( D_{FB} \) between the output and the \( I_{TH} \) pin as shown in the Functional Diagram. In a hard short (\( V_{OUT} = 0V \)) the current will be reduced to approximately 25% of the maximum output current. This technique may be used for all applications with regulated output voltages of 1.8V or greater.

SFB Pin Operation

When the SFB pin drops below its ground referenced 1.19V threshold, continuous mode operation is forced. In continuous mode, the large N-channel main and synchronous switches are used regardless of the load on the main output.

In addition to providing a logic input to force continuous synchronous operation, the SFB pin provides a means to regulate a flyback winding output. Continuous synchronous operation allows power to be drawn from the auxiliary windings without regard to the primary output load. The SFB pin provides a way to force continuous synchronous operation as needed by the flyback winding.

The secondary output voltage is set by the turns ratio of the transformer in conjunction with a pair of external resistors returned to the SFB pin as shown in Figure 4a. The secondary regulated voltage, \( V_{SEC} \), in Figure 4a is given by:

\[
V_{SEC} = (N + 1)V_{OUT} > 1.19 \left(1 + \frac{R6}{R5}\right)
\]

where \( N \) is the turns ratio of the transformer and \( V_{OUT} \) is the main output voltage sensed by \( VOSENSE \).

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as:

\[
\text{Efficiency} = 100\% - (L1 + L2 + L3 + \ldots)
\]

where \( L1, L2, \ldots \) are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC1435 circuits. LTC1435 \( V_{IN} \) current, \( INTVCC \) current, \( I^2R \) losses, and topside MOSFET transition losses.

1. The \( V_{IN} \) current is the DC supply current given in the electrical characteristics which excludes MOSFET driver and control currents. \( V_{IN} \) current results in a small (< 1%) loss which increases with \( V_{IN} \).

2. \( INTVCC \) current is the sum of the MOSFET driver and control currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge \( dQ \) moves from \( INTVCC \) to ground. The resulting \( dQ/dt \) is a current out of \( INT V_{CC} \) which is typically much larger than the control circuit current. In continuous mode, \( I\text{GATECHG} = f(Q_T + Q_B) \), where \( Q_T \) and \( Q_B \) are the gate charges of the topside and bottom side MOSFETs.

By powering \( EXTVCC \) from an output-derived source, the additional \( V_{IN} \) current resulting from the driver and control currents will be scaled by a factor of Duty Cycle/Efficiency. For example, in a 20V to 5V application, 10mA of \( INTVCC \) current results in approximately 3mA of \( V_{IN} \) current. This reduces the midcurrent loss from 10% or more (if the driver was powered directly from \( V_{IN} \)) to only a few percent.

3. \( I^2R \) losses are predicted from the DC resistances of the MOSFET, inductor and current shunt. In continuous mode the average output current flows through \( L \) and \( R_{SENSE} \), but is “chopped” between the topside main...
APPLICATIONS INFORMATION

MOSFET and the synchronous MOSFET. If the two MOSFETs have approximately the same R_DS(ON), then the resistance of one MOSFET can simply be summed with the resistances of L and Rsense to obtain I^2R losses. For example, if each R_DS(ON) = 0.05Ω, R_L = 0.15Ω, and R_sense = 0.05Ω, then the total resistance is 0.25Ω. This results in losses ranging from 3% to 10% as the output current increases from 0.5A to 2A. I^2R losses cause the efficiency to drop at high output currents.

4. Transition losses apply only to the topside MOSFET(s), and only when operating at high input voltages (typically 20V or greater). Transition losses can be estimated from:

\[ \text{Transition Loss} = 2.5 (V_{IN})^{1.85}(I_{MAX})(C_{RSS})(f) \]

Other losses, including C^in and C^out ESR dissipative losses, Schottky conduction losses during dead-time, and inductor core losses, generally account for less than 2% total additional loss.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_out immediately shifts by an amount equal to \( (\Delta I_{LOAD})(ESR) \), where ESR is the effective series resistance of C_out. \( \Delta I_{LOAD} \) also begins to charge or discharge C_out which generates a feedback error signal. The regulator loop then acts to return V_out to its steady-state value. During this recovery time V_out can be monitored for overshoot or ringing which would indicate a stability problem. The I^th external components shown in the Figure 1 circuit will provide adequate compensation for most applications.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_out, causing a rapid drop in V_out. No regulator can deliver enough current to prevent this problem if the load switch resistance is low and it is driven quickly. The only solution is to limit the rise time of the switch drive so that the load rise time is limited to approximately (25)(C_LOAD). Thus a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

Automotive Considerations: Plugging into the Cigarette Lighter

As battery-powered devices go mobile, there is a natural interest in plugging into the cigarette lighter in order to conserve or even recharge battery packs during operation. But before you connect, be advised: you are plugging into the supply from hell. The main battery line in an automobile is the source of a number of nasty potential transients, including load dump, reverse battery and double battery.

Load dump is the result of a loose battery cable. When the cable breaks connection, the field collapse in the alternator can cause a positive spike as high as 60V which takes several hundred milliseconds to decay. Reverse battery is just what it says, while double battery is a consequence of tow truck operators finding that a 24V jump start cranks cold engines faster than 12V.

The network shown in Figure 7 is the most straightforward approach to protect a DC/DC converter from the ravages of an automotive battery line. The series diode prevents current from flowing during reverse battery, while the transient suppressor clamps the input voltage during load dump. Note that the transient suppressor should not conduct during double battery operation, but must still clamp the input voltage below breakdown of the converter. Although the LT1435 has a maximum input voltage of 36V, most applications will be limited to 30V by the MOSFET BV_DSS.

Figure 7. Automotive Application Protection
APPLICATIONS INFORMATION

Design Example

As a design example, assume $V_{IN} = 12\text{V(nominal)}$, $V_{IN} = 22\text{V(max)}$, $V_{OUT} = 3.3\text{V}$, $I_{MAX} = 3\text{A}$ and $f = 250\text{kHz}$, $R_{SENSE}$ and $C_{OSC}$ can immediately be calculated:

$$R_{SENSE} = \frac{100\text{mV}}{3\text{A}} = 0.033\Omega$$
$$C_{OSC} = \frac{1.37(10^4)}{250} - 11 = 43\text{pF}$$

Referring to Figure 3, a 10\(\mu\text{H}\) inductor falls within the recommended range. To check the actual value of the ripple current the following equation is used:

$$\Delta I = \frac{V_{OUT}}{(f)(L)} \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

The highest value of the ripple current occurs at the maximum input voltage:

$$\Delta I = \frac{3.3\text{V}}{250\text{kHz}(10\mu\text{H})} \left(1 - \frac{3.3\text{V}}{22\text{V}}\right) = 1.12\text{A}$$

The power dissipation on the topside MOSFET can be easily estimated. Choosing a Siliconix Si4412DY results in: $R_{DS(ON)} = 0.042\Omega$, $C_{RSS} = 100\text{pF}$. At maximum input voltage with $T(estimated) = 50^\circ\text{C}$:

$$P_{MAIN} = \frac{3.3\text{V}}{22\text{V}} \left[3^2 \left[1 + (0.005)(50^\circ\text{C} - 25^\circ\text{C})\right](0.042\Omega) + 2.5(22\text{V})^{1.85}(3\text{A})(100\text{pF})(250\text{kHz}) = 122\text{mW}$$

The most stringent requirement for the synchronous N-channel MOSFET occurs when $V_{OUT} = 0$ (i.e. short circuit). In this case the worst-case dissipation rises to:

$$P_{SYNC} = \left(I_{SC(AVG)}\right)^2 (1 + \delta) R_{DS(ON)}$$

With the 0.033\(\Omega\) sense resistor $I_{SC(AVG)} = 4\text{A}$ will result, increasing the Si4412DY dissipation to 950mW at a die temperature of 105\(^\circ\text{C}\).

$C_{IN}$ is chosen for an RMS current rating of at least 1.5A at temperature. $C_{OUT}$ is chosen with an ESR of 0.03\(\Omega\) for low output ripple. The output ripple in continuous mode will be highest at the maximum input voltage. The output voltage ripple due to ESR is approximately:

$$V_{ORIPPLE} = R_{ESR}(\Delta I) = 0.03\Omega(1.112\text{A}) = 34\text{mV}_{P\cdot P}$$

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC1435. These items are also illustrated graphically in the layout diagram of Figure 8. Check the following in your layout:

1. Are the signal and power grounds segregated? The LTC1435 signal ground pin must return to the (–) plate of $C_{OUT}$. The power ground connects to the source of the bottom N-channel MOSFET, anode of the Schottky diode, and (–) plate of $C_{IN}$, which should have as short lead lengths as possible.

2. Does the $V_{OSENSE}$ pin connect directly to the feedback resistors? The resistive divider R1, R2 must be connected between the (+) plate of $C_{OUT}$ and signal ground. The 100pF capacitor should be as close as possible to the LTC1435.

3. Are the SENSE− and SENSE+ leads routed together with minimum PC trace spacing? The filter capacitor between SENSE+ and SENSE− should be as close as possible to the LTC1435.

4. Does the (+) plate of $C_{IN}$ connect to the drain of the topside MOSFET(s) as closely as possible? This capacitor provides the AC current to the MOSFET(s).

5. Is the $INTV_{CC}$ decoupling capacitor connected closely between $INTV_{CC}$ and the power ground pin? This capacitor carries the MOSFET driver peak currents.

6. Keep the switching node SW away from sensitive small-signal nodes. Ideally the switch node should be placed at the furthest point from the LTC1435.

7. SGND should be exclusively used for grounding external components on $C_{OSC}$, $I_{TH}$, $V_{OSENSE}$ and SFB pins.
TYPICAL APPLICATIONS

Dual Output 5V and Synchronous 12V Application
TYPICAL APPLICATIONS

3.3V/4.5A Converter with Foldback Current Limiting

Dual Output 5V and 12V Application
Constant-Current/Constant-Voltage High Efficiency Battery Charger

Current Programming Equation

\[ \text{IBATT} = \frac{(\text{IPROG})(R6) - 0.04}{10(R1)} \]

Efficiency

- \( V_{IN} = 24V \)
- \( V_{BATT} = 16V \)
- \( V_{BATT} = 12V \)
- \( V_{BATT} = 6V \)
**PACKAGE DESCRIPTION**

Dimensions in inches (millimeters) unless otherwise noted.

G Package
16-Lead Plastic SSOP (0.209)
(LTC DWG # 05-08-1640)

S Package
16-Lead Plastic Small Outline
(Narrow 0.150)
(LTC DWG # 05-08-1610)

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Low Dropout 2.9V/3A Converter

Related Parts

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<th>Part Number</th>
<th>Description</th>
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</thead>
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<td>Dual High Efficiency Synchronous Step-Down Switching Regulators</td>
<td>Dual Synchronous, $V_{IN} \leq 20V$</td>
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<tr>
<td>LTC1148HV/LTC1148</td>
<td>High Efficiency Synchronous Step-Down Switching Regulator Controllers</td>
<td>Synchronous, $V_{IN} \leq 20V$</td>
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<tr>
<td>LTC1159</td>
<td>High Efficiency Synchronous Step-Down Switching Regulator</td>
<td>Synchronous, $V_{IN} \leq 40V$, For Logic Threshold FETs</td>
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<tr>
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<td>1.5A, 500kHz Step-Down Switching Regulators</td>
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<tr>
<td>LTC1430</td>
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<td>Full-Featured Single Controller</td>
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<td>Full-Featured Dual Controllers</td>
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<td>Constant-Voltage/Constant-Current Battery Charger</td>
<td>1.3A, Li-Ion, NiCd, NiMH, Pb-Acid Charger</td>
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