The LTC®1278 is a 1.6µs, 500ksps, sampling 12-bit A/D converter that draws only 75mW from a single 5V or ±5V supplies. This easy-to-use device comes complete with a 200ns sample-and-hold, a precision reference and an internally trimmed clock. Unipolar and bipolar conversion modes add to the flexibility of the ADC. The low power dissipation is made even more attractive by a 8.5mW power-down feature. Instant wake-up from shutdown allows the converter to be powered down even during brief inactive periods.

The LTC1278 converts 0V to 5V unipolar inputs from a single 5V supply and ±2.5V bipolar inputs from ±5V supplies. Maximum DC specs include ±1LSB INL and ±1LSB DNL. Outstanding guaranteed AC performance includes 70dB S/(N + D) and 78dB THD at the input frequency of 100kHz over temperature.

The internal clock is trimmed for 1.6µs conversion time. The clock automatically synchronizes to each sample command, eliminating problems with asynchronous clock noise found in competitive devices. A separate convert start input and a data ready signal (BUSY) ease connections to FIFOs, DSPs and microprocessors.
LTC1278

**Absolute Maximum Ratings**

AVDD = DVDD = VDD (Notes 1, 2)

Supply Voltage (VDD) .............................................. 12V

Negative Supply Voltage (VSS)

Bipolar Operation Only ........................................ -6V to GND

Total Supply Voltage (VDD to VSS)

Bipolar Operation Only ....................................... 12V

Analog Input Voltage (Note 3)

Unipolar Operation ................... –0.3V to VDD + 0.3V

Bipolar Operation............... VSS – 0.3V to VDD + 0.3V

Digital Input Voltage (Note 4)

Unipolar Operation ................................–0.3V to 12V

Bipolar Operation........................... VSS – 0.3V to 12V

Digital Output Voltage

Unipolar Operation ...................  – 0.3V to VDD + 0.3V

Bipolar Operation................ VSS – 0.3V to VDD + 0.3V

Power Dissipation ............................................. 500mW

Operating Temperature Range

LTC1278-4C, LTC1278-5C ..................... 0°C to 70°C

LTC1278-4I ....................................... – 40°C to 85°C

Storage Temperature Range .......... –65°C to 150°C

Lead Temperature (Soldering, 10 sec).......... 300°C

**Converter Characteristics**

With Internal Reference (Notes 5, 6)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>LTC1278-4/LTC1278-5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution (No Missing Codes)</td>
<td>12</td>
<td>Bit</td>
</tr>
<tr>
<td>Integral Linearity Error</td>
<td>±1 LSB</td>
<td></td>
</tr>
<tr>
<td>Differential Linearity Error</td>
<td>±1 LSB</td>
<td></td>
</tr>
<tr>
<td>Offset Error</td>
<td>±4 LSB</td>
<td>±6 LSB</td>
</tr>
<tr>
<td>Gain Error</td>
<td>±15 LSB</td>
<td></td>
</tr>
<tr>
<td>Gain Error Tempco</td>
<td>±10 ppm/°C</td>
<td>±45 ppm/°C</td>
</tr>
</tbody>
</table>

**Analog Input**  

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>LTC1278-4/LTC1278-5</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_IN</td>
<td>Analog Input Range (Note 9)</td>
<td>4.95V ≤ VDD ≤ 5.25V (Unipolar) 4.75V ≤ VDD ≤ 5.25V, –5.25V ≤ VSS ≤ –2.45V (Bipolar)</td>
<td>±0 to 5 V ±2.5 V</td>
</tr>
<tr>
<td>I_IN</td>
<td>Analog Input Leakage Current</td>
<td>CS = High</td>
<td>±1 µA</td>
</tr>
<tr>
<td>C_IN</td>
<td>Analog Input Capacitance</td>
<td>Between Conversions (Sample Mode) During Conversions (Hold Mode)</td>
<td>45 pF 5 pF</td>
</tr>
</tbody>
</table>
## DYNAMIC ACCURACY (Note 5)

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>LTC1278-4/LTC1278-5</th>
</tr>
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<tbody>
<tr>
<td></td>
<td>Signal-to-Noise Plus Distortion Ratio</td>
<td>100kHz Input Signal</td>
<td>○ 70 72 dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>250kHz Input Signal</td>
<td>○ 70 dB</td>
</tr>
<tr>
<td>THD</td>
<td>Total Harmonic Distortion</td>
<td>100kHz Input Signal</td>
<td>● –80 –78 dB</td>
</tr>
<tr>
<td></td>
<td>First 5 Harmonics</td>
<td>250kHz Input Signal</td>
<td>● –74 dB</td>
</tr>
<tr>
<td></td>
<td>Peak Harmonic or Spurious Noise</td>
<td>100kHz Input Signal</td>
<td>● –84 –78 dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>250kHz Input Signal</td>
<td>● –74 dB</td>
</tr>
<tr>
<td>IMD</td>
<td>Intermodulation Distortion</td>
<td>$f_{IN1} = 99.37kHz, f_{IN2} = 102.4kHz$</td>
<td>● –82 dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$f_{IN1} = 249.37kHz, f_{IN2} = 252.4kHz$</td>
<td>● –70 dB</td>
</tr>
<tr>
<td></td>
<td>Full Power Bandwidth</td>
<td></td>
<td>4 MHz</td>
</tr>
<tr>
<td></td>
<td>Full Linear Bandwidth (S/(N + D) \geq 68dB)</td>
<td></td>
<td>350 kHz</td>
</tr>
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## INTERNAL REFERENCE CHARACTERISTICS (Note 5)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>LTC1278-4/LTC1278-5</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{REF}$ Output Voltage</td>
<td>$I_{OUT} = 0$</td>
<td>2.400 2.420 2.440 V</td>
</tr>
<tr>
<td>$V_{REF}$ Output Tempco</td>
<td>$I_{OUT} = 0$</td>
<td>● ±10 ±45 ppm/°C</td>
</tr>
<tr>
<td>$V_{REF}$ Line Regulation</td>
<td>$4.95V \leq V_{DD} \leq 5.25V$</td>
<td>0.01 LSB/V</td>
</tr>
<tr>
<td></td>
<td>$-5.25V \leq V_{SS} \leq -4.95V$</td>
<td>0.01 LSB/V</td>
</tr>
<tr>
<td>$V_{REF}$ Load Regulation</td>
<td>$0V \leq</td>
<td>I_{OUT}</td>
</tr>
</tbody>
</table>

## DIGITAL INPUTS AND DIGITAL OUTPUTS (Note 5)

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>LTC1278-4/LTC1278-5</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IN}$</td>
<td>High Level Input Voltage</td>
<td>$V_{DD} = 5.25V$</td>
<td>● 2.4 V</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Low Level Input Voltage</td>
<td>$V_{DD} = 4.95V$</td>
<td>● 0.8 V</td>
</tr>
<tr>
<td>$I_{IN}$</td>
<td>Digital Input Current</td>
<td>$V_{IN} = 0V$ to $V_{DD}$</td>
<td>● ±10 μA</td>
</tr>
<tr>
<td>$C_{IN}$</td>
<td>Digital Input Capacitance</td>
<td></td>
<td>5 pF</td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>High Level Output Voltage</td>
<td>$V_{DD} = 4.95V$</td>
<td>● 4.7 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_{O} = -10\mu A$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_{D} = -200\mu A$</td>
<td></td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Low Level Output Voltage</td>
<td>$V_{DD} = 4.95V$</td>
<td>● 0.95 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_{O} = 160\mu A$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_{D} = 1.8mA$</td>
<td></td>
</tr>
<tr>
<td>$I_{OZ}$</td>
<td>High Z Output Leakage D11 to D0</td>
<td>$V_{OUT} = 0V$ to $V_{DD}, CS$ High</td>
<td>● ±10 μA</td>
</tr>
<tr>
<td>$C_{OZ}$</td>
<td>High Z Output Capacitance D11 to D0</td>
<td>CS High (Note 9)</td>
<td>● 15 pF</td>
</tr>
<tr>
<td>$I_{SOURCE}$</td>
<td>Output Source Current</td>
<td>$V_{OUT} = 0V$</td>
<td>–10 mA</td>
</tr>
<tr>
<td>$I_{SINK}$</td>
<td>Output Sink Current</td>
<td>$V_{OUT} = V_{DD}$</td>
<td>10 mA</td>
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## LTC1278

### Power Requirements (Note 5)

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>LTC1278-4/LTC1278-5</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>VDD</td>
<td>Positive Supply Voltage (Notes 10, 11)</td>
<td>Unipolar</td>
<td>4.95</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bipolar</td>
<td></td>
<td>4.75</td>
</tr>
<tr>
<td></td>
<td>VSS</td>
<td>Negative Supply Voltage (Note 10)</td>
<td>Bipolar Only</td>
<td>−2.45</td>
</tr>
<tr>
<td></td>
<td>IDD</td>
<td>Positive Supply Current</td>
<td>$f_{\text{SAMPLE}} = 500\text{ksps}$</td>
<td>15.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SHDN = 0V</td>
<td></td>
<td>1.7</td>
</tr>
<tr>
<td></td>
<td>ISS</td>
<td>Negative Supply Current</td>
<td>$f_{\text{SAMPLE}} = 500\text{ksps}$</td>
<td>0.12</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SHDN = 0V</td>
<td></td>
<td>75.0</td>
</tr>
<tr>
<td></td>
<td>PD</td>
<td>Power Dissipation</td>
<td>$f_{\text{SAMPLE}} = 500\text{ksps}$</td>
<td>8.5</td>
</tr>
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</table>

### Timing Characteristics (Note 5)

<table>
<thead>
<tr>
<th>SYMBOL</th>
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<th>CONDITIONS</th>
<th>LTC1278-4/LTC1278-5</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$f_{\text{SAMPLE(MAX)}}$</td>
<td>Maximum Sampling Frequency</td>
<td></td>
<td>kHz</td>
</tr>
<tr>
<td></td>
<td>$f_{\text{SAMPLE(MIN)}}$</td>
<td>Minimum Throughput Time (Acquisition Time Plus Conversion Time)</td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td></td>
<td>$t_{\text{CONV}}$</td>
<td>Conversion Time</td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td></td>
<td>$t_{\text{ACQ}}$</td>
<td>Acquisition Time</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>$t_1$</td>
<td>CS↓ to RD↓ Setup Time</td>
<td>(Notes 9, 10)</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>$t_2$</td>
<td>CS↓ to CONVST↓ Setup Time</td>
<td>(Notes 9, 10)</td>
<td>20</td>
</tr>
<tr>
<td></td>
<td>$t_3$</td>
<td>SHDN↑ to CONVST↓ Wake-Up Time</td>
<td>(Note 10)</td>
<td>350</td>
</tr>
<tr>
<td></td>
<td>$t_4$</td>
<td>CONVST Low Time</td>
<td>(Notes 10, 12)</td>
<td>40</td>
</tr>
<tr>
<td></td>
<td>$t_5$</td>
<td>CONVST↓ to BUSY↓ Delay</td>
<td>$C_L = 100\text{pF}$</td>
<td>40</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Commercial</td>
<td></td>
<td>130</td>
</tr>
<tr>
<td></td>
<td>$t_6$</td>
<td>Data Ready Before BUSY↑</td>
<td>$C_L = 100\text{pF}$</td>
<td>20</td>
</tr>
<tr>
<td></td>
<td>$t_7$</td>
<td>Wait Time RD↓ After BUSY↑</td>
<td>Mode 2, (see Figure 14) (Note 9)</td>
<td>−20</td>
</tr>
<tr>
<td></td>
<td>$t_8$</td>
<td>Data Access Time After RD↓</td>
<td>$C_L = 20\text{pF}$ (Note 9)</td>
<td>50</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Commercial</td>
<td></td>
<td>110</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Industrial</td>
<td></td>
<td>70</td>
</tr>
<tr>
<td></td>
<td></td>
<td>70</td>
<td>125</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>$t_9$</td>
<td>Bus Relinquish Time</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>$t_{10}$</td>
<td>RD Low Time</td>
<td>(Note 9)</td>
<td>$t_8$</td>
</tr>
<tr>
<td></td>
<td>$t_{11}$</td>
<td>CONVST High Time</td>
<td>(Notes 9, 12)</td>
<td>40</td>
</tr>
<tr>
<td></td>
<td>$t_{12}$</td>
<td>Aperture Delay of Sample-and-Hold</td>
<td>Jitter &lt;50ps</td>
<td>15</td>
</tr>
</tbody>
</table>
**TYPICAL PERFORMANCE CHARACTERISTICS**

**Integral Nonlinearity vs Output Code**

- **Input Frequency:** 10k, 100k, 1M, 2M Hz
- **f\_{SAMPLE} = 500kHz**

**Differential Nonlinearity vs Output Code**

- **Input Frequency:** 10k, 100k, 1M, 2M Hz
- **f\_{SAMPLE} = 500kHz**

**ENOBs and S/(N + D) vs Input Frequency**

- **Nyquist Frequency**
- **f\_{SAMPLE} = 500kHz**

---

**Note 7:** Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

**Note 8:** Bipolar offset is the offset voltage measured from –1/2LSB when the output code flickers between 0000 0000 0000 and 1111 1111 1111.

**Note 9:** Guaranteed by design, not subject to test.

**Note 10:** Recommended operating conditions.

**Note 11:** A\_IN must not exceed V\_DD or fall below V\_SS by more than 50mV for specified accuracy. Therefore the minimum supply voltage for the unipolar mode is 4.95V. The minimum for the bipolar mode is 4.75V, –2.45V.

**Note 12:** The falling CONVST edge starts a conversion. If CONVST returns high at a bit decision point during the conversion it can create small errors. For best performance ensure that CONVST returns high either within 120ns after conversion start (i.e., before the first bit decision) or after BUSY rises (i.e., after the last bit test). See mode 1a and 1b (Figures 12 and 13) timing diagrams.
TYPICAL PERFORMANCE CHARACTERISTICS

S/(N + D) vs Input Frequency and Amplitude

Signal-to-Noise Ratio (without Harmonics) vs Input Frequency

Distortion vs Input Frequency

Spurious Free Dynamic Range vs Input Frequency

Intermodulation Distortion Plot

Acquisition Time vs Source Impedance

Supply Current vs Temperature

Power Supply Feedthrough vs Ripple Frequency

Reference Voltage vs Load Current
**PIN FUNCTIONS**

**AIN (Pin 1):** Analog Input. 0V to 5V (Unipolar), ±2.5V (Bipolar).

**VREF (Pin 2):** 2.42V Reference Output. Bypass to AGND (10µF tantalum in parallel with 0.1µF ceramic).

**AGND (Pin 3):** Analog Ground.

**D11 to D4 (Pins 11 to 4):** Three-State Data Outputs. D11 is the Most Significant Bit.

**DGND (Pin 12):** Digital Ground.

**D3 to D0 (Pins 13 to 16):** Three-State Data Outputs.

**DVDD (Pin 17):** Digital Power Supply, 5V. Tie to AVDD pin.

**SHDN (Pin 18):** Power Shutdown.

**CONVST (Pin 19):** Conversion Start Signal. This active low signal starts a conversion on its falling edge (to recognize CONVST, CS has to be low).

**RD (Pin 20):** READ Input. This enables the output drivers when CS is low.

**CS (Pin 21):** The CHIP SELECT input must be low for the ADC to recognize CONVST and RD inputs.

**BUSY (Pin 22):** The BUSY output shows the converter status. It is low when a conversion is in progress.

**VSS (Pin 23):** Negative Supply. –5V for bipolar operation. Bypass to AGND with 0.1µF ceramic. Analog ground for unipolar operation.

**AVDD (Pin 24):** Positive Supply, 5V. Bypass to AGND (10µF tantalum in parallel with 0.1µF ceramic).

---

**FUNCTIONAL BLOCK DIAGRAM**

- **AIN**
- **Csample**
- **2.42V REF**
- **VREF**
- **AGND**
- **DGND**
- **12-BIT CAPACITIVE DAC**
- **COMPARATOR**
- **SUCCESSIVE APPROXIMATION REGISTER**
- **OUTPUT LATCHES**
- **CONTROL LOGIC**
- **AVDD**
- **DVDD**
- **VSS**
- **Csample**
- **0V FOR UNIPOLAR MODE OR –5V FOR BIPOLAR MODE**
LTC1278

TEST CIRCUITS

Load Circuits for Access Timing

Load Circuits for Output Float Delay

Timing Diagrams

CS to RD Setup Timing

CS to CONVST Setup Timing

SHDN to CONVST Wake-Up Timing

Applications Information

Conversion Details

The LTC1278 uses a successive approximation algorithm and an internal sample-and-hold circuit to convert an analog signal to a 12-bit parallel output. The ADC is complete with a precision reference and an internal clock. The control logic provides easy interface to microprocessors and DSPs. (Please refer to the Digital Interface section for the data format.)

Conversion start is controlled by the CS and CONVST inputs. At the start of conversion the successive approximation register (SAR) is reset. Once a conversion cycle has begun it cannot be restarted.

During conversion, the internal 12-bit capacitive DAC output is sequenced by the SAR from the most significant bit (MSB) to the least significant bit (LSB). Referring to Figure 1, the A\textsubscript{IN} input connects to the sample-and-hold capacitor during the acquire phase, and the comparator offset is nulled by the feedback switch. In this acquire phase, a minimum delay of 200ns will provide enough time for the sample-and-hold capacitor to acquire the analog signal. During the convert phase, the comparator feedback switch opens, putting the comparator into the
APPLICATIONS INFORMATION

The LTC1278 has excellent high speed sampling capability. FFT (Fast Fourier Transform) test techniques are used to test the ADC’s frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using an FFT algorithm, the ADC’s spectral content can be examined for frequencies outside the fundamental. Figure 2 shows a typical LTC1278 FFT plot.

Figure 2. LTC1278 Nonaveraged, 4096 Point FFT Plot

Signal-to-Noise Ratio

The Signal-to-Noise plus Distortion Ratio \( S/(N + D) \) is the ratio between the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other frequency components at the A/D output. The output is band limited to frequencies from above DC and below half the sampling frequency. Figure 2 shows a typical spectral content with a 500kHz sampling rate and a 100kHz input. The dynamic performance is excellent for input frequencies up to the Nyquist limit of 250kHz.

Effective Number of Bits

The Effective Number of Bits (ENOBs) is a measurement of the resolution of an ADC and is directly related to the \( S/(N + D) \) by the equation:

\[
N = \frac{S}{N + D} - 1.76 \times 6.02
\]

where \( N \) is the Effective Number of Bits of resolution and \( S/(N + D) \) is expressed in dB. At the maximum sampling rate of 500kHz the LTC1278 maintains very good ENOBs up to the Nyquist input frequency of 250kHz. Refer to Figure 3.

Total Harmonic Distortion

Total Harmonic Distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency. THD is expressed as:

\[
THD = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 \ldots + V_N^2}}{V_1}
\]

where \( V_1 \) is the RMS amplitude of the fundamental frequency and \( V_2 \) through \( V_N \) are the amplitudes of the second through \( N \)th harmonics. THD versus input
frequency is shown in Figure 4. The LTC1278 has good
distortion performance up to the Nyquist frequency and
beyond.

Intermodulation Distortion

If the ADC input signal consists of more than one spectral
component, the ADC transfer function nonlinearity can
produce intermodulation distortion (IMD) in addition to
THD. IMD is the change in one sinusoidal input caused by
the presence of another sinusoidal input at a different
frequency.

If two pure sine waves of frequencies $f_a$ and $f_b$ are applied
to the ADC input, nonlinearities in the ADC transfer func-
tion can create distortion products at sum and difference
frequencies of $mf_a \pm nf_b$, where $m$ and $n = 0, 1, 2, 3$, etc.
For example, the 2nd order IMD terms include $(fa + fb)$ and
$(fa – fb)$ while the 3rd order IMD terms include $(2fa + fb),
(2fa – fb), (fa + 2fb)$, and $(fa – 2fb)$. If the two input sine
waves are equal in magnitude, the value (in decibels) of
the 2nd order IMD products can be expressed by the
following formula:

$$IMD (fa \pm fb) = 20 \log \frac{\text{Amplitude at (fa } \pm \text{ fb)}}{\text{Amplitude at fa}}$$

Figure 5 shows the IMD performance at a 100kHz input.

Peak Harmonic or Spurious Noise

The peak harmonic or spurious noise is the largest spec-
tral component excluding the input signal and DC. This
value is expressed in decibels relative to the RMS value of
a full-scale input signal.

Full Power and Full Linear Bandwidth

The full power bandwidth is that input frequency at which
the amplitude of the reconstructed fundamental is re-
duced by 3dB for a full-scale input signal.

The full linear bandwidth is the input frequency at which
the $S/(N + D)$ has dropped to 68dB (11 effective bits). The
LTC1278 has been designed to optimize input bandwidth,
allowing ADC to undersample input signals with frequen-
cies above the converter’s Nyquist Frequency. The noise
floor stays very low at high frequencies; $S/(N + D)$ be-
comes dominated by distortion at frequencies far beyond
Nyquist.

Driving the Analog Input

The analog input of the LTC1278 is easy to drive. It draws
only one small current spike while charging the sample-
and-hold capacitor at the end of conversion. During con-
version the analog input draws no current. The only
requirement is that the amplifier driving the analog input
must settle after the small current spike before the next
conversion starts. Any op amp that settles in 200ns to small current transients will allow maximum speed operation. If slower op amps are used, more settling time can be provided by increasing the time between conversions. Suitable devices capable of driving the ADC’s A_IN input include the LT1360, LT1220, LT1223 and LT1224 op amps.

Internal Reference

The LTC1278 has an on-chip, temperature compensated, curvature corrected, bandgap reference, which is factory trimmed to 2.42V. It is internally connected to the DAC and is available at Pin 2 to provide up to 1mA current to an external load.

For minimum code transition noise the reference output should be decoupled with a capacitor to filter wideband noise from the reference (10µF tantalum in parallel with a 0.1µF ceramic).

The V_REF pin can be driven with a DAC or other means to provide input span adjustment in bipolar mode. The V_REF pin must be driven to at least 2.45V to prevent conflict with the internal reference. The reference should be driven to no more than 4.8V to keep the input span within the ±5V supplies.

Figure 6 shows an LT1006 op amp driving the reference pin. (In the unipolar mode, the input span is already 0V to 5V with the internal reference so driving the reference is not recommended, since the input span will exceed the supply and codes will be lost at the full scale.) Figure 7 shows a typical reference, the LT1019A-2.5 connected to the LTC1278. This will provide an improved drift (equal to the maximum 5ppm/°C of the LT1019A-2.5) and a ±2.582V full scale.

UNIPOLAR/BIPOLAR OPERATION AND ADJUSTMENT

Figure 8a shows the ideal input/output characteristics for the LTC1278. The code transitions occur midway between successive integer LSB values (i.e., 0.5LSB, 1.5LSB, 2.5LSB, ... FS – 1.5LSB). The output code is naturally binary with 1LSB = FS/4096 = 5V/4096 = 1.22mV. Figure 8b shows the input/output transfer characteristics for the bipolar mode in two’s complement format.
APPLICATIONS INFORMATION

Unipolar Offset and Full-scale Error Adjustments

In applications where absolute accuracy is important, then offset and full-scale errors can be adjusted to zero. Offset error must be adjusted before full-scale error. Figure 9a shows the extra components required for full-scale error adjustment. If both offset and full-scale adjustments are needed, the circuit in Figure 9b can be used. For zero offset error apply 0.61mV (i.e., 1/2LSB) at the input and adjust the offset trim until the LTC1278 output code flickers between 0000 0000 0000 and 0000 0000 0001. For zero full-scale error apply an analog input of 4.99817V (i.e., FS – 1 1/2LSBs) at the input and R5 is adjusted until the output code flickers between 1111 1111 1110 and 1111 1111 1111.

Bipolar Offset and Full-scale Error Adjustments

Bipolar offset and full-scale errors are adjusted in a similar fashion to the unipolar case. Again, bipolar offset must be adjusted before full-scale error. Bipolar offset error adjustment is achieved by trimming the offset of the op amp driving the analog input of the LTC1278 while the input voltage is 1/2LSB below ground. This is done by applying an input voltage of −0.61mV (−0.5LSB) to the input in Figure 9c and adjusting the R8 until the ADC output code flickers between 0000 0000 0000 and 1111 1111 1111. For full-scale adjustment, an input voltage of 2.49817V (FS − 1.5LSBs) is applied to the input and R5 is adjusted until the output code flickers between 0111 1111 1110 and 0111 1111 1111.

BOARD LAYOUT AND BYPASSING

Wire wrap boards are not recommended for high resolution or high speed A/D converters. To obtain the best performance from the LTC1278, a printed circuit board is required. Layout for the printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track or underneath the ADC. The analog input should be screened by AGND.

High quality tantalum and ceramic bypass capacitors should be used at the AVDD and VREF pins as shown in Figure 10. For the bipolar mode, a 0.1µF ceramic provides adequate bypassing for the VSS pin. The capacitors must be located as close to the pins as possible. The traces connecting the pins and the bypass capacitors must be kept short and should be made as wide as possible.

Input signal leads to AIN and signal return leads from AGND (Pin 3) should be kept as short as possible to minimize input noise coupling. In applications where this is not possible, a shielded cable between source and ADC is recommended.
APPLICATIONS INFORMATION

Also, since any potential difference in grounds between the signal source and ADC appears as an error voltage in series with the input signal, attention should be paid to reducing the ground circuit impedances as much as possible.

A single point analog ground separate from the logic system ground should be established with an analog ground plane at Pin 3 (AGND) or as close as possible to the ADC. Pin 12 (DGND) and all other analog grounds should be connected to this single analog ground point. No other digital grounds should be connected to this analog ground point. Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC and the foil width for these tracks should be as wide as possible. In applications where the ADC data outputs and control signals are connected to a continuously active microprocessor bus, it is possible to get errors in conversion results. These errors are due to feedthrough from the microprocessor to the successive approximation comparator. The problem can be eliminated by forcing the microprocessor into a WAIT state during conversion or by using three-state buffers to isolate the ADC data bus.

DIGITAL INTERFACE

The A/D converter is designed to interface with microprocessors as a memory mapped device. The CS and RD control inputs are common to all peripheral memory interfacing. A separate CONVST is used to initiate a conversion.

Internal Clock

The A/D converter has an internal clock that eliminates the need of synchronization between the external clock and the CS and RD signals found in other ADCs. The internal clock is factory trimmed to achieve a typical conversion time of 1.6µs. No external adjustments are required, and with the typical acquisition time of 250ns, throughput performance of 500ksps is assured.

Power Shutdown

The LTC1278 provides a shutdown feature that will save power when the ADC is in inactive periods. To power down the ADC, Pin 18 (SHDN) needs to be driven low. When in power shutdown mode, the LTC1278 will not start a conversion even though the CONVST goes low. All the

Figure 10. Power Supply Grounding Practice

Figure 11. Internal Logic for Control Inputs CS, RD, CONVST and SHDN
power is off except the Internal Reference which is still active and provides 2.42V output voltage to the other circuitry. In this mode the ADC draws 8.5mW instead of 75mW (for minimum power, the logic inputs must be within 600mV of the supply rails). The wake-up time from the power shutdown to active state is 350ns.

**Timing and Control**

Conversion start and data read operations are controlled by three digital inputs: CS, CONVST and RD. Figure 11 shows the logic structure associated with these inputs. A logic “0” for CONVST will start a conversion after the ADC has been selected (i.e., CS is low). Once initiated it cannot be restarted until the conversion is complete. Converter status is indicated by the BUSY output, and this is low while conversion is in progress.

Figures 12 through 16 show several different modes of operation. In modes 1a and 1b (Figures 12 and 13) CS and RD are both tied low. The falling CONVST starts the conversion. The data outputs are always enabled and data can be latched with the BUSY rising edge. Mode 1a shows operation with a narrow low going CONVST pulse. Mode 1b shows high going CONVST pulse.

In mode 2 (Figure 14) CS is tied low. The falling CONVST signal again starts the conversion. Data outputs are in three-state until read by MPU with the RD signal. Mode 2 can be used for operation with a shared MPU databus.

In Slow memory and ROM modes (Figures 15 and 16) CS is tied low and CONVST and RD are tied together. The MPU starts conversion and read the output with the RD signal. Conversions are started by the MPU or DSP (no external sample clock).

In Slow memory mode the processor takes RD (= CONVST) low and starts the conversion. BUSY goes low forcing the processor into a WAIT state. The previous conversion result appears on the data outputs. When the conversion is complete, the new conversion results appear on the data outputs; BUSY goes high releasing the processor, and the processor takes RD (= CONVST) back high and reads the new conversion data.

In ROM mode, the processor takes RD (= CONVST) low which starts a conversion and reads the previous conversion result. After the conversion is complete, the processor can read the new result (which will initiate another conversion).
Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.
**PACKAGE DESCRIPTION**

Dimensions in inches (millimeters) unless otherwise noted.

### N Package
24-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)

![Diagram of N Package]

### SW Package
24-Lead Plastic Small Outline (Wide 0.300)
(LTC DWG # 05-08-1620)

![Diagram of SW Package]

**RELATED PARTS**

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>LTC1274/LTC1277</td>
<td>12-Bit, 10mW, 100ksps A/D Converters with 1µA Shutdown</td>
<td>Complete with Clock Reference</td>
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<tr>
<td>LTC1279</td>
<td>12-Bit, 600ksps Sampling A/D Converter with Shutdown</td>
<td>70dB SINAD at Nyquist, Low Power</td>
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<tr>
<td>LTC1400</td>
<td>12-Bit, 400ksps Serial A/D Converter</td>
<td>Complete High Speed 12-Bit ADC in SO-8</td>
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<tr>
<td>LTC1409</td>
<td>12-Bit, 800ksps Sampling A/D Converter with Shutdown</td>
<td>Fast, Complete Low Power ADC</td>
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<tr>
<td>LTC1415</td>
<td>12-Bit, 1.25Msps Sampling A/D Converter with Shutdown</td>
<td>Single 5V Supply, Low Power: 55mW</td>
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<tr>
<td>LTC1419</td>
<td>14-Bit, 800ksps Sampling A/D Converter with Shutdown</td>
<td>81.5dB SINAD, Low Power: 150mW</td>
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