FEATURES

- Very Low Noise: 0.75µV_P-P Typ, 0.1Hz to 10Hz
- DC to 1Hz Noise Lower Than OP-07
- Full Output Swing into 1k Load
- Offset Voltage: 10µV Max
- Offset Voltage Drift: 50nV/°C Max
- Common Mode Rejection Ratio: 110dB Min
- Power Supply Rejection Ratio: 115dB Min
- No External Components Required
- Pin Compatible with Standard 8-Pin Op Amps
- Available in Standard 8-Pin Plastic DIP and 8-Pin SO Packages

APPLICATIONS

- Electronic Scales
- Strain Gauge Amplifiers
- Thermocouple Amplifiers
- High Resolution Data Acquisition
- Low Noise Transducers
- Instrumentation Amplifiers

DESCRIPTION

The LTC1250 is a high performance, very low noise zero-drift operational amplifier. The LTC1250’s combination of low front-end noise and DC precision makes it ideal for use with low impedance bridge transducers. The LTC1250 features typical input noise of 0.75µV_P-P from 0.1Hz to 10Hz, and 0.2µV_P-P from 0.1Hz to 1Hz. The LTC1250 has DC to 1Hz noise of 0.35µV_P-P, surpassing that of low noise bipolar parts including the OP-07, OP-77, and LT1012. The LTC1250 uses the industry-standard single op amp pinout, and requires no external components or nulling signals, allowing it to be a plug-in replacement for bipolar op amps.

The LTC1250 incorporates an improved output stage capable of driving 4.3V into a 1k load with a single 5V supply; it will swing ±4.9V into 5k with ±5V supplies. The input common mode range includes ground with single power supply voltages above 12V. Supply current is 3mA with a ±5V supply, and overload recovery times from positive and negative saturation are 0.5ms and 1.5ms, respectively. The internal nulling clock is set at 5kHz for optimum low frequency noise and offset drift; no external connections are necessary.

The LTC1250 is available in a standard 8-pin plastic DIP and 8-pin SO packages.

TYPICAL APPLICATION

Differential Bridge Amplifier

Input Referred Noise 0.1Hz to 10Hz
**LTC1250**

### ABSOLUTE MAXIMUM RATINGS (Note 1)
- Total Supply Voltage ($V^+ \text{ to } V^-$) ............................. 18V
- Input Voltage ........................ ($V^+ + 0.3V$) to ($V^- - 0.3V$)
- Output Short Circuit Duration ......................... Indefinite
- Storage Temperature Range ................  –65°C to 150°C
- Lead Temperature (Soldering, 10 sec.) ............... 300°C

### Operating Temperature Range
- LTC1250M (OBSOLETE) ............... –55°C to 125°C
- LTC1250C ................................. 0°C TO 70°C

### PACKAGE/ORDER INFORMATION

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>LTC1250M</th>
<th>LTC1250C</th>
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<td>$V_{OS}$</td>
<td>Input Offset Voltage</td>
<td>$T_A = 25^\circ C$ (Note 2)</td>
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<td>$\Delta V_{OS}$</td>
<td>Average Input Offset Drift</td>
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<td>±0.01</td>
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<td>$e_n$</td>
<td>Input Noise Voltage (Note 3)</td>
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<td>$I_B$</td>
<td>Input Bias Current</td>
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<td>Common Mode Rejection Ratio</td>
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<td>PSRR</td>
<td>Power Supply Rejection Ratio</td>
<td>$V_S = \pm 2.375V$ to $\pm 8V$</td>
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<td>$A_{VOL}$</td>
<td>Large-Signal Voltage Gain</td>
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<td>Maximum Output Voltage Swing</td>
<td>$R_L = 1k$</td>
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<td>$R_L = 100k$</td>
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<td>Slew Rate</td>
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<td>$I_S$</td>
<td>Supply Current</td>
<td>No Load, $T_A = 25^\circ C$</td>
<td>±3.0</td>
<td>±4.0</td>
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Consult LTC Marketing for parts specified with wider operating temperature ranges.

### ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, $V_{IN} = \pm 5V$, otherwise specifications are at $T_A = 25^\circ C$.

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**Notes:**
1. ABSOLUTE AXI U RATI GSW WW U
2. Total Supply Voltage ($V^+ \text{ to } V^-$) ............................. 18V
3. Input Voltage ........................ ($V^+ + 0.3V$) to ($V^- - 0.3V$)
4. Output Short Circuit Duration ......................... Indefinite
5. Storage Temperature Range ................  –65°C to 150°C
6. Lead Temperature (Soldering, 10 sec.) ............... 300°C
7. Operating Temperature Range
   - LTC1250M (OBSOLETE) ............... –55°C to 125°C
   - LTC1250C ................................. 0°C TO 70°C
8. | ORDER PART NUMBER | LTC1250CN8 | LTC1250CS8 |
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<td>8-LEAD PLASTIC SO</td>
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<td>$T_{JMAX} = 110^\circ C$, $\theta JA = 130^\circ CW$</td>
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<td>$T_{JMAX} = 150^\circ C$, $\theta JA = 100°C$</td>
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Consult the N8 or S8 for Alternative Source

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**1250b**
ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, \( V_{IN} = \pm 5 \text{V} \), otherwise specifications are at \( T_A \).

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**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

**Note 2:** These parameters are guaranteed by design. Thermocouple effects preclude measurement of these voltage levels during automated testing.

**Note 3:** 0.1Hz to 10Hz noise is specified DC coupled in a 10s window; 0.1Hz to 1Hz noise is specified in a 100s window with an RC high-pass filter at 0.1Hz. The LTC1250 is sample tested for noise; for 100% tested parts contact LTC Marketing Dept.

**Note 4:** At \( T \leq 0\degree \text{C} \) these parameters are guaranteed by design and not tested.

TYPICAL PERFORMANCE CHARACTERISTICS

Input Noise vs Supply Voltage

Supply Current vs Supply Voltage

Sampling Frequency vs Supply Voltage

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1250-G01

1250-G02

1250-G03
TYPICAL PERFORMANCE CHARACTERISTICS

Transient Response

Output Swing vs Load Resistance, Dual Supplies

Output Voltage Swing vs Load Resistance, Single Supply

Output Swing vs Output Current, ±5V Supply

Output Swing vs Output Current, Single 5V Supply

Short-Circuit Current vs Temperature

TEST CIRCUITS

Offset Test Circuit

DC to 10Hz Noise Test Circuit
(for DC to 1Hz Multiply All Capacitor Values by 10)
**Input Noise**

The LTC1250, like all CMOS amplifiers, exhibits two types of low frequency noise: thermal noise and 1/f noise. The LTC1250 uses several design modifications to minimize these noise sources. Thermal noise is minimized by raising the $g_m$ of the front-end transistors by running them at high bias levels and using large transistor geometries. 1/f noise is combated by optimizing the zero-drift nulling loop to run at twice the 1/f corner frequency, allowing it to reduce the inherently high CMOS 1/f noise to near thermal levels at low frequencies. The resultant noise spectrum is quite low at frequencies below the internal 5kHz clock frequency, approaching the best bipolar op amps at 10Hz and surpassing them below 1Hz (Figure 1). All this is accomplished in an industry-standard pinout; the LTC1250 requires no external capacitors, no nulling or clock signals, and conforms to industry-standard 8-pin DIP and 8-pin SO packages.

Larger values of $C_F$, commonly used in band-limited DC circuits, may actually increase low frequency noise. The nulling circuitry in the LTC1250 closes a loop that includes the external feedback network during part of its cycle. This loop must settle to its final value within $150\mu s$ or it will not fully cancel the 1/f noise spectrum and the low frequency noise of the part will rise. If the loop is underdamped (large $R_F$, no $C_F$) it will ring for more than $150\mu s$ and the noise and offset will suffer.

The solution is to add $C_F$ as above but beware! Too large a value of $C_F$ will overdamp the loop, again preventing it from reaching a final value by the $150\mu s$ deadline. This condition doesn’t affect the LTC1250’s offset or output stability, but 1/f noise begins to rise. As a rule of thumb, the $R_F C_F$ feedback pole should be $\geq 7$kHz ($1/150\mu s$, the frequency at which the loop settles) for best 1/f performance; values between 100pF and 500pF work well with feedback resistors below 100k. This ensures adequate gain at 7kHz for the LTC1250 to properly null. High value feedback resistors (above 1M) may require experimentation to find the correct value because parasitics, both in the feedback network and the LTC1250's inputs, can affect stability with a feedback network impedance as low as 1.9k. This effect can be eliminated by adding a capacitor across the feedback resistor, adding a zero which cancels the input pole (Figure 2). The value of this capacitor should be:

$$C_F \geq \frac{55\text{pF}}{A_V}$$

where $A_V = $ closed-loop gain. Note that $C_F$ is not dependent on the value of $R_F$. Circuits with higher gain ($A_V > 50$) or low loop impedance should not require $C_F$ for stability.

**Input Capacitance and Compensation**

The large input transistors create a parasitic 55pF capacitance from each input to $V^+$. This input capacitance will react with the external feedback resistors to form a pole which can affect amplifier stability. In low gain, high impedance configurations, the pole can land below the unity-gain frequency of the feedback network and degrade phase margin, causing ringing, oscillation, and other unpleasantness. This is true of any op amp, however, the 55pF capacitance at the LTC1250’s inputs can affect stability with a feedback network impedance as low as 1.9k. This effect can be eliminated by adding a capacitor across the feedback resistor, adding a zero which cancels the input pole (Figure 2). The value of this capacitor should be:

$$C_F \geq \frac{55\text{pF}}{A_V}$$

where $A_V = $ closed-loop gain. Note that $C_F$ is not dependent on the value of $R_F$. Circuits with higher gain ($A_V > 50$) or low loop impedance should not require $C_F$ for stability.
APPLICATIONS INFORMATION

LTC1250 and on the PC board, play an increasing role. Low value resistors (below 5k) may not require a capacitor at all.

**Input Bias Current**

The inputs of the LTC1250, like all zero-drift op amps, draw only small switching spikes of AC bias current; DC leakage current is negligible except at very high temperatures. The large front-end transistors cause switching spikes 3 to 4 times greater than standard zero-drift op amps: the ±50pA bias current spec is still many times better than most bipolar parts. The spikes don’t match from one input pin to the other, and are sometimes (but not always) of opposite polarity. As a result, matching the impedances at the inputs (Figure 3) will not cancel the bias current, and may cause additional errors. Don’t do it.

![Figure 3. Extra Resistor Will Not Cancel Bias Current Errors](image)

**Output Drive**

The LTC1250 includes an enhanced output stage which provides nearly symmetrical output source/sink currents. This output is capable of swinging a minimum of ±4V into a 1k load with ±5V supplies, and can sink or source >20mA into low impedance loads. Lightly loaded ($R_L \geq 100k$), the LTC1250 will swing to within millivolts of either rail. In single supply applications, it will typically swing 4.3V into a 1k load with a 5V supply.

**Minimizing External Errors**

The input noise, offset voltage, and bias current specs for the LTC1250 are all well below the levels of circuit board parasitics. Thermocouples between the copper pins of the LTC1250 and the tin/lead solder used to connect them can overwhelm the offset voltage of the LTC1250, especially if a soldering iron has been around recently. Note also that when the LTC1250’s output is heavily loaded, the chip may dissipate substantial power, raising the temperature of the package and aggravating thermocouples at the inputs. Although the LTC1250 will maintain its specified accuracy under these conditions, care must be taken in the layout to prevent or compensate circuit errors. Be especially careful of air currents when measuring low frequency noise; nearby moving objects (like people) can create very large noise peaks with an unshielded circuit board. For more detailed explanations and advice on how to avoid these errors, see the LTC1051/LTC1053 data sheet.

**Sampling Behavior**

The LTC1250’s zero-drift nulling loop samples the input at $\approx 5kHz$, allowing it to process signals below 2kHz with no aliasing. Signals above this frequency may show aliasing behavior, although wideband internal circuitry generally keeps errors to a minimum. The output of the LTC1250 will have small spikes at the clock frequency and its harmonics; these will vary in amplitude with different feedback configurations. Low frequency or band-limited systems should not be affected, but systems with higher bandwidth (oversampling A/Ds, for example) may need to filter out these clock artifacts. Output spikes can be minimized with a large feedback capacitor, but this will adversely affect noise performance (see Input Capacitance and Compensation on the previous page). Applications which require spike-free output in addition to minimum noise will need a low-pass filter after the LTC1250; a simple RC will usually do the job (Figure 4). The LTC1051/LTC1053 data sheet includes more information about zero-drift amplifier sampling behavior.

![Figure 4. RC Output Pole Limits Bandwidth to 330Hz](image)
Single Supply Operation

The LTC1250 will operate with single supply voltages as low as 4.5V, and the output swings to within millivolts of either supply when lightly loaded. The input stage will common mode to within 250mV of ground with a single 5V supply, and will common mode to ground with single supplies above 11V. Most bridge transducers bias their inputs above ground when powered from single supplies, allowing them to interface directly to the LTC1250 in single supply applications. Single-ended, ground-referenced signals will need to be level shifted slightly to interface to the LTC1250’s inputs.

Fault Conditions

The LTC1250 is designed to withstand most external fault conditions without latch-up or damage. However, unusually severe fault conditions can destroy the part. All pins are protected against faults of ±25mA or 5V beyond either supply, whichever comes first. If the external circuitry can exceed these limits, series resistors or voltage clamp diodes should be included to prevent damage.

The LTC1250 includes internal protection against ESD damage. All data sheet parameters are maintained to 1kV ESD on any pin; beyond 1kV, the input bias and offset currents will increase, but the remaining specs are unaffected and the part remains functional to 5kV at the input pins and 8kV at the output pin. Extreme ESD conditions should be guarded against by using standard antistatic precautions.
J8 Package
8-Lead CERDIP (Narrow .300 Inch, Hermetic)
(Reference LTC DWG # 05-08-1110)

NOTE: LEAD DIMENSIONS APPLY TO SOLDER DIP/PLATE OR TIN PLATE LEADS.

OBSOLETE PACKAGE
N8 Package
8-Lead PDIP (Narrow .300 Inch)
(Reference LTC DWG # 05-08-1510)

NOTE:
1. DIMENSIONS ARE INCHES
MILLIMETERS
* THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)
Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.
TYPICAL APPLICATIONS

Reference Buffer

Differential Thermocouple Amplifier

+10ppm ERROR AT ±15mA
1µV p-p OUTPUT NOISE
2.5µV/°C DRIFT (DUE TO LM399)

VOUT
100mV/°C

RELATED PARTS

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<th>PART NUMBER</th>
<th>DESCRIPTION</th>
<th>COMMENTS</th>
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