**FEATURES**

- Standard 8-Pin Packages
- High Power Factor Over Wide Load Range with Line Current Averaging
- International Operation Without Switches
- Instantaneous Overvoltage Protection
- Minimal Line Current Dead Zone
- Typical 250μA Start-Up Supply Current
- Rejects Line Switching Noise
- Synchronization Capability
- Low Quiescent Current: 9mA
- Fast 1.5A Peak Current Gate Driver

**APPLICATIONS**

- Universal Power Factor Corrected Power Supplies
- Preregulators up to 1500W

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**DESCRIPTION**

The 8-pin LT®-1249 provides active power factor correction for universal offline power systems with very few external parts. By using fixed high frequency PWM current averaging without the need for slope compensation, the LT1249 achieves far lower line current distortion, with a smaller magnetic element than systems that use either peak current detection or zero current switching approach, in both continuous and discontinuous modes of operation.

The LT1249 uses a multiplier containing a square gain function from the voltage amplifier to reduce the AC gain at light output load and thus maintains low line current distortion and high system stability. The LT1249 also provides filtering capability to reject line switching noise which can cause instability when fed into the multiplier. Line current dead zone is minimized with low bias voltage at the current input to the multiplier.

The LT1249 provides many protection features including peak current limiting and overvoltage protection. The switching frequency is internally set at 100kHz.

While the LT1249 simplifies PFC design with minimal parts count, the LT1248 provides flexibilities in switching frequency, overvoltage and current limit.

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**BLOCK DIAGRAM**
# Absolute Maximum Ratings

Supply Voltage ....................................................... 27V  
GTDR Current Continuous ..................................... 0.5A  
GTDR Output Energy (Per Cycle) ............................. 5\mu J  
I_{AC} Input Current ............................................. 20mA  
V_{SENSE} Input Voltage ........................................... V_{MAX}  
M_{OUT} Input Current .......................................... \pm 5mA  
Operating Junction Temperature Range  
LT1249C ................................................ 0°C to 100°C  
LT1249I ........................................... –40°C to 125°C  
Thermal Resistance (Junction-to-Ambient)  
N8 Package ................................................ 100°C/W  
S8 Package ................................................. 120°C/W  
Storage Temperature Range ..................–65°C to 150°C  
Lead Temperature (Soldering, 10 sec)................. 300°C

# Package/Order Information

<table>
<thead>
<tr>
<th>ORDER PART NUMBER</th>
<th>PART NUMBER</th>
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<tbody>
<tr>
<td>LT1249CN8</td>
<td>LT1249CS8</td>
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<tr>
<td>LT1249IN8</td>
<td>LT1249IS8</td>
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<th>TOP VIEW</th>
<th>ORDER PART NUMBER</th>
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<tr>
<td>N8 PACKAGE 8-LEAD PDIP</td>
<td>LT1249CN8</td>
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<tr>
<td>S8 PACKAGE 8-LEAD PLASTIC SO</td>
<td>LT1249IS8</td>
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Consult factory for Military grade parts.

# Electrical Characteristics

The * denotes specifications which apply over the operating temperature range, otherwise specifications are at \( T_A = 25°C \). Maximum operating voltage (V_{MAX}) = 25V, V_{CC} = 18V, I_{AC} = 100\mu A, CAOUT = 3.5V, V_{AOUT} = 5V, no load on any outputs, unless otherwise noted.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
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<tr>
<td>Overall Supply Current (V_{CC} in Undervoltage Lockout) ( V_{CC} = \text{Lockout Voltage} - 0.2V )</td>
<td>( \bullet )</td>
<td>0.25</td>
<td>0.45</td>
<td>mA</td>
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<tr>
<td>Supply Current, On ( 11.5V \leq V_{CC} \leq V_{MAX}, CAOUT = 1V )</td>
<td>( \bullet )</td>
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<td>12</td>
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<td>V_{CC} Turn-On Threshold</td>
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<td>15.5</td>
<td>16.5</td>
<td>17.5</td>
<td>V</td>
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<tr>
<td>V_{CC} Turn-Off Threshold</td>
<td>( \bullet )</td>
<td>9.5</td>
<td>10.5</td>
<td>11.5</td>
<td>V</td>
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<td>Voltage Amplifier</td>
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<td></td>
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<td>V_{SENSE} Bias Current ( V_{SENSE} = 0V ) to 7V</td>
<td>( \bullet )</td>
<td>–25</td>
<td>–250</td>
<td>nA</td>
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<td>Voltage Amp Gain</td>
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<td>Voltage Amp Unity-Gain Bandwidth</td>
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<td>Voltage Amp Output High</td>
<td>( 0 \leq \text{Source Current} \leq 50\mu A )</td>
<td>( \bullet )</td>
<td>10</td>
<td>12</td>
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<td>Voltage Amp Output Low</td>
<td>( 0 \leq \text{Sink Current} \leq 5\mu A )</td>
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<td>0.1</td>
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<td>Voltage Amp Source Current</td>
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<td>130</td>
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<td>33</td>
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<td>Voltage Amp Sink Current Hysteresis</td>
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<td>( \pm 2 )</td>
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<td>Current Amp Transconductance ( \Delta CAOUT = \pm 40\mu A )</td>
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<td>320</td>
<td>550</td>
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<td>Current Amp Voltage Gain</td>
<td>( 2.5V \leq V_{CAOUT} \leq 7.5V )</td>
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<td>500</td>
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<td>220</td>
<td>\mu A</td>
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<td>Current Amp Output Low</td>
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**ELECTRICAL CHARACTERISTICS**

The ● denotes specifications which apply over the operating temperature range, otherwise specifications are at $T_A = 25^\circ C$. Maximum operating voltage ($V_{\text{MAX}}$) = 25V, $V_{\text{CC}} = 18V$, $I_{\text{AC}} = 100\mu A$, $CA_{\text{OUT}} = 3.5V$, $VA_{\text{OUT}} = 5V$, no load on any outputs, unless otherwise noted.

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<td>Reference</td>
<td>$T_A = 25^\circ C$, Measured at $V_{\text{SENSE}}$ Pin</td>
<td>7.39</td>
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<td>Reference Output Voltage Line Regulation</td>
<td>$V_{\text{LOCKOUT}} &lt; V_{\text{CC}} &lt; V_{\text{MAX}}$</td>
<td>●</td>
<td>–20</td>
<td>5</td>
<td>20 mV</td>
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| Multiplier                          | $I_{\text{AC}} = 100\mu A$, $VA_{\text{OUT}} = 5V$                         | 35    |       |       | $\mu A$ |
| Multiplier Output Current Offset    | $R_{\text{AC}} = 1M$ from $I_{\text{AC}}$ to GND                           | ●     | –0.05 | –0.5  | $\mu A$ |
| Multiplier Max Output Current ($I_{\text{IM(MAX)}}$) | $I_{\text{AC}} = 450\mu A$, $VA_{\text{OUT}} = 7V$ (Note 2)               | ●     | –375  | –250  | –150  | $\mu A$ |
| Multiplier Max Output Current Voltage ($I_{\text{IM(MAX)}} \cdot R_{\text{MOUT}}$) | $I_{\text{AC}} = 450\mu A$, $VA_{\text{OUT}} = 7V$ (Note 2)               | ●     | –1.25 | –1.1  | –0.96 | V     |
| Multiplier Gain Constant (Note 3)   |                                                                              | 0.035 |       |       | $V^{-2}$ |
| $I_{\text{AC}}$ Input Resistance   | $I_{\text{AC}}$ from 50$\mu A$ to 1mA                                      | 15    | 32    | 50    | k$\Omega$ |

| Oscillator                          |                                                                             | 75    | 100   | 125   | kHz  |
| Control Pin (CAOUT) Threshold       | Duty Cycle = 0                                                              | ●     | 1.3   | 1.8   | 2.3   | V    |
| Synchronization Frequency Range     | Synchronizing Pulse Low $\leq 0.35V$ on CAOUT                               | ●     | 127   | 160   | kHz  |

| Gate Driver                         |                                                                             | 12    | 15    | 17.5  | V    |
| Max GTDR Output Voltage             | 0mA Load, 18V $< V_{\text{CC}} < V_{\text{MAX}}$ (Note 4)                 | ●     |       |       | V    |
| GTDR Output High                    | $–200mA$ Load, 11.5V $\leq V_{\text{CC}} \leq 15V$                         | ●     | $V_{\text{CC}} – 3.0$ | V  |
| GTDR Output Low (Device Unpowered)  | $V_{\text{CC}} = 0V$, 50mA Load (Sinking)                                  | ●     | 0.9   | 1.5   | V    |
| GTDR Output Low (Device Active)     | $200mA$ Load (Sinking)                                                      | ●     | 0.5   | 1     | V    |
| Peak GTDR Current                   | $10nF$ from GTDR to GND                                                     | ●     | 1.5   |       | A    |
| GTDR Rise and Fall Time             | $1nF$ from GTDR to GND                                                     |       | 25    |       | ns   |
| GTDR Max Duty Cycle                 |                                                                             | 90    | 96    |       | %    |

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: Current amplifier is in linear mode with 0V input common mode.

Note 3: Multiplier Gain Constant: $K = \frac{I_{\text{IM}}}{I_{\text{AC}}(VA_{\text{OUT}} – 1.5)^2}$

Note 4: Maximum GTDR output voltage is internally clamped for higher $V_{\text{CC}}$ voltages.

**TYPICAL PERFORMANCE CHARACTERISTICS**
TYPICAL PERFORMANCE CHARACTERISTICS

Reference Voltage vs Temperature

Multiplier Current

Supply Current vs Supply Voltage

GTDR Source Current

GTDR Sink Current

GTDR Rise and Fall Time

Start-Up Supply Current vs Supply Voltage

Switching Frequency
**PIN FUNCTIONS**

**GND (Pin 1):** Ground.

**CAOUT (Pin 2):** This is the output of the current amplifier that senses and forces the line current to follow the reference signal that comes from the multiplier by commanding the pulse width modulator. When CAOUT is low, the modulator has zero duty cycle.

**MOUT (Pin 3):** The multiplier current goes out of this pin through the 4k resistor RMOUT. The voltage developed across RMOUT is the reference voltage of the current loop and it is limited to 1.1V. The noninverting input of the current amplifier is also tied to RMOUT. In operation, MOUT is normally at negative potential and only AC signals appear at the noninverting input of the current amplifier.

**IAC (Pin 4):** This is the AC line voltage sensing input to the multiplier. It is a current input that is biased at 2V to minimize the crossover dead zone caused by low line voltage. A 32k resistor is in series with the current input, so that a small external capacitor can be used to filter out the switching noise from the high impedance lines.

**VAOUT (Pin 5):** This is the output of the voltage error amplifier. The output is clamped at 12V. When the output goes below 1.5V, the multiplier output current is zero.
PIN FUNCTIONS

**VSENSE (Pin 6):** This is the inverting input to the voltage amplifier.

**VCC (Pin 7):** This is the supply of the chip. The LT1249 has a very fast gate driver required to fast charge high power MOSFET gate capacitance. High current spikes occur during charging. For good supply bypass, a $0.1\mu$F ceramic capacitor in parallel with a low ESR electrolytic capacitor, $56\mu$F or higher is required in close proximity to IC GND.

**GTDR (Pin 8):** The MOSFET gate driver is a 1.5A fast totem pole output. It is clamped at 15V. Capacitive loads like MOSFET gates may cause overshoot. A gate series resistor of at least $5\Omega$ will prevent the overshoot.

APPLICATIONS INFORMATION

**Error Amplifier**

The error amplifier has a 100dB DC gain and 1.5MHz unity-gain frequency. It is internally clamped at 12V. The noninverting input is tied to the 7.5V reference.

**Current Amplifier**

The multiplier output current $I_M$ flows out of the $M_{OUT}$ pin through the 4k resistor $R_{MOUT}$ and develops the reference signal to the current loop that is controlled by the current amplifier. Current gain is the ratio of $R_{MOUT}$ to line current sense resistor. The current amplifier is a transconductance amplifier. Typical $g_m$ is $320\mu$mho and gain is 60dB with no load. The inverting input is internally tied to GND. The noninverting input is tied to the multiplier output. The output is internally clamped at 8V. Output resistance is about 4M; DC loading should be avoided because it will lower the gain and introduce offset voltage at the inputs which becomes a false reference signal to the current loop and can distort line current. Note that in the current averaging operation, high gain at twice the line frequency is necessary to minimize line current distortion. Because $CA_{OUT}$ may need to swing 5V over one line cycle at high line condition, 11mV will be present at the inputs of the current amplifier if gain is rolled off to 450 at 120Hz (1nF in series with $10k$ at $CA_{OUT}$). At light load, when $(I_M)(R_{MOUT})$ can be less than 100mV, lower gain will distort the current loop reference signal and line current. If signal gain at the 100kHz switching frequency is too high, the system behaves more like a current mode system and can cause subharmonic oscillation. Therefore, the current amplifier should be compensated to have a gain of less than 15 at 100kHz and more than 300 at 120Hz.

**Multiplier**

The multiplier is a current multiplier with high noise immunity in a high power switching environment. The current gain is:

$$I_M = (I_{AC})(I_{EA^2})/(200\mu A)^2, \text{ and}$$

$$I_{EA} = (V_{AOUT} - 1.5V)/25k$$

With a square function, because of the lower gain at light power load, system stability is maintained and line current distortion caused by the AC ripple fed back to the error amplifier is minimized. Note that switching ripple on the high impedance lines could get into the multiplier from the $I_{AC}$ pin and cause instability. The LT1249 provides an internal 25k resistor in series with the low impedance multiplier current input so that only a capacitor from the $I_{AC}$ pin to GND is needed to filter out the noise. Maximum multiplier output current is limited to $250\mu A$. Figure 1 shows the multiplier transfer curves.

![Figure 1. Multiplier Current $I_M$ vs $I_{AC}$ and $V_{AOUT}$](image-url)
**APPLICATIONS INFORMATION**

**Line Current Limiting**
Maximum voltage across $R_{MOUT}$ is internally limited to 1.1V. Therefore, line current limit is 1.1V divided by the sense resistor $R_S$. With a 0.2Ω sense resistor $R_S$ line current limit is 5.5A. As a general rule, $R_S$ is chosen according

$$R_S = \frac{(I_{M\text{MAX}})(R_{MOUT})(V_{\text{LINE\text{MIN}}})}{K(1.414)P_{OUT\text{MAX}}},$$

where $P_{OUT\text{MAX}}$ is the maximum power output and $K$ is usually between 1.1 and 1.3 depending on efficiency and resistor tolerance. When the output is overloaded and line current reaches limit, output voltage $V_{OUT}$ will drop to keep line current constant. System stability is still maintained by the current loop which is controlled by the current amplifier. Further load current increase results in further $V_{OUT}$ drop and clipping of the line current, which degrades power factor.

**Synchronization**
The LT1249 can be externally synchronized in a frequency range of 127kHz to 160kHz. Figure 2 shows the synchronizing circuit. Synchronizing occurs when CAOUT pin is pulled below 0.5V with an external transistor and a Schottky diode. The Schottky diode and the 10k pull-up resistor are necessary for the required fast slewing back up to the normal operating voltage on CAOUT after the transistor is turned off. Positive slewing on CAOUT should be faster than the oscillator ramp rate of 0.5V/μs.

The width of the synchronizing pulse should be under 60ns. The synchronizing pulses introduce an offset voltage on the current amplifier inputs, according to:

$$\Delta V_{OS} = \left(\frac{(ts)(fs)(V_C - 0.5)}{R_2}\right)\frac{1}{g_m}$$

$ts = $ pulse width
$fs = $ pulse frequency
$I_C = CAOUT$ source current ($\approx 150\mu A$)
$V_C = CAOUT$ operating voltage (1.8V to 6.8V)
$R_2 = $ resistor for the midfrequency “zero” in the current loop
$g_m = $ current amplifier transconductance ($\approx 320\mu \text{mho}$)

With $ts = 30\text{ns}$, $fs = 130\text{kHz}$, $V_C = 3\text{V}$ and $R_2 = 10\text{k}$, offset voltage shift is $\approx 5\text{mV}$. Note that this offset voltage will add slight distortion to line current at light load.

**Overvoltage Protection**
In Figure 3, R1 and R2 set the regulator output DC level: $V_{OUT} = V_{REF}[(R_1 + R_2)/R_2]$. With $R_1 = 1\text{M}$ and $R_2 = 20\text{k}$, $V_{OUT}$ is 382V.

Because of the slow loop response necessary for power factor correction, output overshoot can occur with sudden load removal or reduction. To protect the power components and output load, the LT1249 voltage error amplifier senses the output voltage and quickly shuts off the current switch when overvoltage occurs. When overshoot occurs on $V_{OUT}$, the overcurrent from R1 will go through VAOUT because amplifier feedback keeps $V_{SENSE}$ locked at 7.5V. When this overcurrent reaches 44μA amplifier sinking limit, the amplifier loses feedback and its output snaps low to turn the multiplier off.

Overvoltage trip level: $\Delta V_{OUT} = (44\mu \text{A})(R_1)$
The Figure 3 circuit therefore has 382V on VOUT, and an overvoltage level = (VOUT + 44V), or 426V. With a 22μA hysteresis, VOUT then has to drop 22V to 404V before feedback recovers and the switch turns back on.

MOUT is a high impedance current output. In the current loop, offset line current is determined by multiplier offset current and input offset voltage of the current amplifier. A negative 4mV current amplifier VOS translates into 20mA line current and 5W input power for 250V line if 0.2Ω sense resistor is used. Under no load or when the load power is less than this offset input power, VOUT would slowly charge up to an overvoltage state because the overvoltage comparator can only reduce multiplier output current to zero. This does not guarantee zero output current if the current amplifier has offset. To regulate VOUT under this condition, the amplifier M1 (see Block Diagram), becomes active in the current loop when VAOUT goes down to 1V. The M1 can put out up to 15mA to the 4kΩ resistor at the inverting input to cancel the current amplifier negative VOS and keep VOUT error to within 2V.

Undervoltage Lockout

The LT1249 turns on when VCC is higher than 16V and remains on until VCC falls below 10V, whereupon the chip enters the lockout state. In the lockout state, the LT1249 only draws 250μA, the oscillator is off, the VREF and the GTDR pins remain low to keep the power MOSFET off.

Start-Up and Supply Voltage

The LT1249 draws only 250μA before the chip starts at 16V on VCC. To trickle start, a 90k resistor from the power line to VCC supplies the trickle current and C4 holds the VCC up while switching starts (see Figure 4). Then the auxiliary winding takes over and supplies the operating current. Note that D3 and the large value C3, in both Figures 4 and 5, are only necessary for systems that have sudden large load variation down to minimum load and/or very light load conditions. Under these conditions, the loop may exhibit a start/restart mode because switching remains off long enough for C4 to discharge below 10V. The C3 will hold VCC up until switching resumes. For less severe load variations, D3 is replaced with a short and C3 is omitted. The turns ratio between the primary winding and the auxiliary winding determines VCC according to: VOUT/(VCC – 2V) = NP/NS. For 382V VOUT and 18V VCC, NP/NS = 19.

In Figure 5 a new technique for supply voltage eliminates the need for an extra inductor winding. It uses capacitor charge transfer to generate a constant current source which feeds a Zener diode. Current to the Zener is equal to (VOUT – VZ)(C)(f), where VZ is Zener voltage and f is switching frequency. For VOUT = 382V, VZ = 18V, C = 1000pF and f = 100kHz, Zener current will be 36mA. This is enough to operate the LT1249, including the FET gate drive.

Output Capacitor

The peak-to-peak 120Hz output ripple is determined by:

\[ V_{P-P} = 2 \left( I_{LOAD DC} \right) (Z) \]

where \( I_{LOAD DC} \): DC load current

\( Z \): capacitor impedance at 120Hz

For 180μF at 300W load, \( I_{LOAD DC} = 300W/385V = 0.78A, \)
**APPLICATIONS INFORMATION**

\[ V_{P-P} = (2)(0.78A)(7.4\Omega) = 11.5V. \] If less ripple is desired, higher capacitance should be used.

The selection of the output capacitor should also be based on the operating ripple current through the capacitor.

The ripple current can be divided into three major components. The first is at 120Hz whose RMS value is related to the DC load current as follows:

\[ I_{1RMS} = (0.71)(I_{LOADDC}) \]

The second component contains the PF switching frequency ripple current and its harmonics. Analysis of this ripple is complicated because it is modulated with a 120Hz signal. However, computer numerical integration and Fourier analysis approximate the RMS value reasonably close to the bench measurements. The RMS value is about 0.82A at a typical condition of 120VAC, 200W load. This ripple is line voltage dependent, and the worst case is at low line.

\[ I_{2RMS} = 0.82A \text{ at 120VAC, 200W} \]

The third component is the switching ripple from the load, if the load is a switching regulator.

\[ I_{3RMS} = I_{LOADDC} \]

For United Chemicon KMH 400V capacitor series, ripple current multiplier for currents at 100kHz is 1.43. The equivalent 120Hz ripple current can then be found:

\[ I_{RMS} = \sqrt{(I_{1RMS})^2 + (I_{2RMS}/1.43)^2 + (I_{3RMS}/1.43)^2} \]

For a typical system that runs at an average load of 200W and 385V output:

\[ I_{LOADDC} = 0.52A \]
\[ I_{1RMS} = (0.71)(0.52A) = 0.37A \]
\[ I_{2RMS} = 0.82A \text{ at 120VAC} \]
\[ I_{3RMS} = I_{LOADDC} = 0.52A \]

\[ I_{RMS} = \sqrt{(0.37A)^2 + (0.82A/1.43)^2 + (0.52A/1.43)^2} = 0.77A \]

The 120Hz ripple current rating at 105°C ambient is 0.95A for the 180µF KMH 400V capacitor. The expected life of the output capacitor may be calculated from the thermal stress analysis:

\[ L = \left(\frac{L_{0}}{2}\right)^{\left(\frac{(105°C+\Delta T_{K})-(T_{\text{AMB}}+\Delta T_{O})}{10}\right)} \]

where

- \( L \) = expected life time
- \( L_{0} \) = hours of load life at rated ripple current and rated ambient temperature
- \( \Delta T_{K} \) = capacitor internal temperature rise at rated condition
- \( \Delta T_{K} = \frac{I^2R}{(KA)} \), where \( I \) is the rated current, \( R \) is capacitor ESR, and \( KA \) is a volume constant.
- \( T_{\text{AMB}} \) = operating ambient temperature
- \( \Delta T_{O} \) = capacitor internal temperature rise at operating condition

In our example, \( L_{0} = 2000 \) hours and \( \Delta T_{K} = 10°C \) at rated 0.95A. \( \Delta T_{O} \) can then be calculated from:

\[ \Delta T_{O} = \left(\frac{IRMS}{0.95A}\right)^{2}(\Delta T_{K}) = \left(\frac{0.77A}{0.95A}\right)^{2}(10°C) = 6.6°C \]

Assuming the operating ambient temperature is 60°C, the approximate life time is:

\[ L_{O} = \left(2000\right)^{\left(\frac{(105°C+10°C)-(60°C+6.6°C)}{10}\right)} = 57,000 \text{ Hrs.} \]

For longer life, capacitor with higher ripple current rating or parallel capacitors should be used.

**Protection Against Abnormal Current Surge Conditions**

The LT1249 has an upper limit on the allowed voltage across the current sense resistor. The voltage into the \( M_{\text{OUT}} \) pin connected to this resistor must not exceed −6V while the chip is running and −12V under any conditions. The LT1249 gate drive will malfunction if the \( M_{\text{OUT}} \) pin voltage exceeds −6V while \( V_{CC} \) is powered, destroying the power FET. The 12V absolute limit is imposed by ESD clamps on the \( M_{\text{OUT}} \) pin. Large currents will flow at
voltages above 8V and the 12V limit is only for surge conditions.

In normal operation, the voltage into M\text{OUT} does not exceed 1.1V, but under surge conditions, the voltage could temporarily go higher. To date, no field failures due to surges have been reported for normal LT1249 configurations, but if the possibility exists for extremely large current surges, please read the following discussion.

Offline switching power supplies can create large current surges because of the high value storage capacitor used. The surge can be the result of closing the line switch near the peak of the AC line voltage, or because of a large transient in the line itself. These surges are well known in the power supply business, and are normally controlled with a negative temperature coefficient thermistor in series with the rectifier bridge. When power is switched on, the thermistor is cold (high resistance) and surges are limited. Current flow in the thermistor causes it to heat and resistance drops to the point where overall efficiency loss in the resistor is acceptable.

This basic protection mechanism can be partially defeated if the power supply is switched off for a few seconds, then turned back on. The thermistor has not had time to cool significantly and if the subsequent turn-on catches the AC line near its peak, the resulting surge is much higher than normal. Even if this surge current generates a voltage greater than 6V (but less than 12V) across the sense resistor, the standard LT1249 application will not be affected because the chip is not yet powered. Problems are only created if the V\text{CC} pin is powered from some external housekeeping supply that remains powered when bridge power is switched off.

A huge line voltage surge, beyond the normal worst-case limits, can also create a large current surge. The peak of the line voltage must significantly exceed the storage capacitor voltage (typically 380V) for this to occur, so peak line voltage would probably have to exceed 450V. Such excessive surges might occur if a very large mains load was suddenly removed, with a resulting line “kickback”. If the surge results in voltage at the M\text{OUT} pin greater than 6V, it must also last more than 30\mu s (three switch cycles) to cause FET problems.

External Clamp

The external clamp shown in Figure 6 will protect the LT1249 M\text{OUT} pin against extremely large line current surges (see above). Protection is provided for all V\text{CC} power methods. The 100\Omega resistor and three diodes limit the peak negative voltage into M\text{OUT} to less than 3V. Current sense gain is attenuated by only 100\Omega/4000\Omega = 2.5%. Three diodes are used because the peak negative voltage into M\text{OUT} in normal operation could go as high as –1.1V and the diodes should not conduct more than a few microamperes under this condition.

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**Figure 6. Protecting M\text{OUT} from Extremely High Current Surges**
PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

N8 Package
8-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)

**THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD
FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE
**RELATED PARTS**

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>LT1103</td>
<td>Off-Line Switching Regulator</td>
<td>Universal Off-Line Inputs with Outputs to 100W</td>
</tr>
<tr>
<td>LT1248</td>
<td>Full Feature Average Current Mode Power Factor Controller</td>
<td>Provides All Features in 16-Lead Package</td>
</tr>
<tr>
<td>LT1508</td>
<td>Power Factor and PWM Controller</td>
<td>Simplified PFC Design</td>
</tr>
<tr>
<td>LT1509</td>
<td>Power Factor and PWM Controller</td>
<td>Complete Solution for Universal Off-Line Switching Power Supplies</td>
</tr>
</tbody>
</table>

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