LTC 1045
Programmable Micropower Hex Translator/Receiver/Driver

FEATURES
- Efficiently Translate Voltage Levels
- Internal Hysteresis for Noise Immunity
- Output Latches Included
- Three-State Outputs
- Programmable Power/Speed
- Power Can Be Completely Shut Off
- ±50V on Inputs with External 100k Limit Resistor
- 1.2μs Response at 100μA Supply Current

APPLICATIONS
- TTL/CMOS to ±5V Analog Switch Drive
- TTL to CMOS (3V to 15V VCC)
- ECL to CMOS (3V to 15V VCC)
- Ground Isolation Buffer
- Low Power RS232 Line Receiver

DESCRIPTION
The LTC® 1045 is a hex level translator manufactured using Linear Technology’s enhanced LTCMOS™ silicon gate process. It consists of six high speed comparators with output latches and three-state capability. Each comparator’s plus input is brought out separately. The minus inputs of comparators 1 to 4 are tied to VTRIP1 while 5 and 6 are tied to VTRIP2.

The ISET pin has several functions. When taken to V+ the outputs are latched and power is completely shut off. Power/speed can be programmed by connecting ISET to V− through an external resistor.

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**ABSOLUTE MAXIMUM RATINGS**

(Notes 1, 2)

- Total Supply Voltage \((V^+, \text{VOH} \text{ to } V^-, \text{VOL})\) .............. 18V
- Output High Voltage \((\text{VOH})\) .................................. \(\leq V^+\)
- Input Voltage .......................................... 18V to \((V^- – 0.3V)\)
- Output Short-Circuit Duration
  \((\text{VOH} – \text{VOL} \leq 10V)\) ................. Continuous
- ESD (MIL-STD-883, Method 3015) .................... 2000V
- Operating Temperature Range ................. –40°C to 85°C
- Storage Temperature Range ................. –55°C to 150°C
- Lead Temperature (Soldering, 10 sec) .......... 300°C

**PACKAGE/ORDER INFORMATION**

<table>
<thead>
<tr>
<th>ORDER PART NUMBER</th>
<th>LTC1045CN</th>
<th>LTC1045CSW</th>
</tr>
</thead>
<tbody>
<tr>
<td>TOP VIEW</td>
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<td></td>
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<tr>
<td>N PACKAGE</td>
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<tr>
<td>20-LEAD PDIP</td>
<td></td>
<td></td>
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<tr>
<td>TJ(<em>{MAX}) = 110°C, (q</em>{JA}) = 90°C/W (N)</td>
<td></td>
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<tr>
<td>SW PACKAGE</td>
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<tr>
<td>20-LEAD SO WIDE</td>
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<td></td>
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<tr>
<td>TJ(<em>{MAX}) = 110°C, (q</em>{JA}) = 90°C/W (SW)</td>
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<td>J PACKAGE</td>
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<tr>
<td>20-LEAD CERDIP</td>
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<td>TJ(<em>{MAX}) = 150°C, (q</em>{JA}) = 70°C/W (J)</td>
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<td>OBSOLETE PACKAGE</td>
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<tr>
<td>20-LEAD CERDIP</td>
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</table>

Consult LTC Marketing for parts specified with wider operating temperature ranges.

**ELECTRICAL CHARACTERISTICS**

The \(\bullet\) denotes the specifications which apply over the full operating temperature range, otherwise specifications are at \(T_A = 25°C\). \(V^+ = \text{VOH} = 5V, V^- = \text{VOL} = 0V\) unless otherwise specified. (Note 3).

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>I_B</td>
<td>Input Bias Current</td>
<td>(V^- \leq V_{IN} \leq V^+)</td>
<td>(\bullet)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(\bullet)</td>
<td>0.5</td>
</tr>
<tr>
<td>I_T</td>
<td>Trip Voltage Range (Pins 8, 9)</td>
<td>(V^- \leq V^+ \leq V^- + 2)</td>
<td>V</td>
</tr>
<tr>
<td>I_S</td>
<td>V^+ to V^- Supply Current</td>
<td>(\text{DISABLE} = V^+, R_{SET} = 10k)</td>
<td>(\bullet)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(\bullet)</td>
<td>3.5</td>
</tr>
<tr>
<td>I_OFF</td>
<td>V^+ to V^- Supply Current in Shutdown</td>
<td>(\text{DISABLE} = I_{SET} = V^+)</td>
<td>(\bullet)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(\bullet)</td>
<td>1</td>
</tr>
<tr>
<td>V_REF</td>
<td>Voltage on I_{SET} (Pin 12)</td>
<td>(R_{SET} = 10k)</td>
<td>(\bullet)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(\bullet)</td>
<td>0.9</td>
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<tr>
<td></td>
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<td>(\bullet)</td>
<td>1.25</td>
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<tr>
<td>V_OH</td>
<td>TTL Output High Voltage</td>
<td>(I_{OUT} = -360\mu A, V^+ = 4.5V)</td>
<td>(\bullet)</td>
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<td></td>
<td></td>
<td>(\bullet)</td>
<td>4.4</td>
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<tr>
<td>V_OL</td>
<td>TTL Output Low Voltage</td>
<td>(I_{OUT} = 1.6mA, V^- = 4.5V)</td>
<td>(\bullet)</td>
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<tr>
<td></td>
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<td>(\bullet)</td>
<td>0.4</td>
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<tr>
<td>I_SINK</td>
<td>Output Short-Circuit Sink Current</td>
<td>(V_{IN} = V_{TRIP} - 100mA, V_{OUT} = V^+)</td>
<td>(\bullet)</td>
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<tr>
<td></td>
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<td>(\bullet)</td>
<td>15</td>
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<tr>
<td>I_SOURCE</td>
<td>Output Short-Circuit Source Current</td>
<td>(V_{IN} = V_{TRIP} + 100mA, V_{OUT} = V^-)</td>
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<tr>
<td></td>
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<td>(\bullet)</td>
<td>8.0</td>
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<td>(\bullet)</td>
<td>3.2</td>
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<tr>
<td>I_QZ</td>
<td>Three-State Leakage Current</td>
<td>(\text{DISABLE} = V^+, \text{VOL} \leq V_{OUT} \leq V_{OH})</td>
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<tr>
<td>R_OH</td>
<td>Output Resistance to V_OH</td>
<td>(</td>
<td>I_{OUT}</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(\bullet)</td>
<td>475</td>
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<td>(\bullet)</td>
<td>600</td>
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<td>R_OL</td>
<td>Output Resistance to V_OH</td>
<td>(</td>
<td>I_{OUT}</td>
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<td></td>
<td></td>
<td>(\bullet)</td>
<td>180</td>
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<td>(\bullet)</td>
<td>250</td>
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<tr>
<td>I_SET</td>
<td>Voltage for Shutdown</td>
<td>(V^+ - 0.5)</td>
<td>(\bullet)</td>
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<tr>
<td>V_H</td>
<td>DISABLE Input Logic Levels</td>
<td>(V^+ = 4.5V, V^- = 0V)</td>
<td>(\bullet)</td>
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<td></td>
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<td>(\bullet)</td>
<td>0.8</td>
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<tr>
<td>V_L</td>
<td>Input Supply Differential ((V^+ – V^-)) (Note 3)</td>
<td>(V^+ = 5.5V, V^- = 0V)</td>
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<td></td>
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<td>15</td>
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<td>(\bullet)</td>
<td>3</td>
</tr>
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<td></td>
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<td>(\bullet)</td>
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</table>
AC ELECTRICAL CHARACTERISTICS

The ✷ denotes the specifications which apply over the full operating temperature range, otherwise specifications are at TA = 25°C. V+ = VOH = 5V, V- = VOL = 0V, unless otherwise specified.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
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<tr>
<td>tｄ</td>
<td>Response Time</td>
<td>Test Circuit Figure 1</td>
<td>✷ 250</td>
<td>350</td>
<td>ns</td>
<td></td>
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<tr>
<td>ISETUP</td>
<td>Time Before Rising Edge of ISET that Data Must Be Present</td>
<td>Test Circuit Figure 2</td>
<td>80</td>
<td>ns</td>
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<tr>
<td>IHOLD</td>
<td>Time After Rising Edge of ISET that Data Must Be Present</td>
<td>Test Circuit Figure 2</td>
<td>0</td>
<td>ns</td>
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<tr>
<td>tACC</td>
<td>Falling Edge of DISABLE to Logic Level (from Hi-Z State)</td>
<td>Test Circuit Figure 3</td>
<td>165</td>
<td>ns</td>
<td></td>
<td></td>
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<tr>
<td>Ih, IOH</td>
<td>Rising Edge of DISABLE to Hi-Z State</td>
<td>Test Circuit Figure 3</td>
<td>200</td>
<td>ns</td>
<td></td>
<td></td>
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</table>

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The maximum differential voltage between any two power pins (V+, V-, VOH and VOL) must not exceed 18V. The maximum recommended operating differential is 15V.

Note 3: During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple or ground noise; any of these conditions must not cause a supply differential to exceed the absolute maximum rating.

TYPICAL PERFORMANCE CHARACTERISTICS
**PIN FUNCTIONS**

**V_{OH} (Pin 1):** High Level to which the Output Switches.

**IN1 to IN7 (Pins 2 to 7):** Six Comparator Inputs; Voltage Range = \( V^- \) to \( V^- + 18V \).

**V_{TRIP2} (Pin 8):** Trip Point for Last Two Comparators (Inputs 5,6); Voltage Range = \( V^- \) to \( V^+ - 2V \).

**V_{TRIP1} (Pin 9):** Trip Point for First Four Comparators (Inputs 1 to 4); Voltage Range = \( V^- \) to \( V^+ - 2V \).

**V^- (Pin 10):** Comparator Negative Supply.

**V_{OL} (Pin 11):** Low Level to which the Output Switches.

**I_{SET} (Pin 12):** This has three functions: 1) \( R_{SET} \) from this pin to \( V^- \) sets bias current, 2) when forced to \( V^+ \) power is shut off completely and 3) when forced to \( V^+ \) outputs are latched.

**DISABLE (Pin 13):** When high, outputs are Hi-Z.

**OUT6 to OUT1 (Pins 14 to 19):** Six Driver Outputs.

**V^+ (Pin 20):** Comparator Positive Supply.

**TEST CIRCUITS**

![Figure 1. Response Time Test Circuit](image1)

**Figure 1. Response Time Test Circuit**

![Figure 2. Latch Test Circuit](image2)

**Figure 2. Latch Test Circuit**

![Figure 3. Three-State Output Test Circuit](image3)

**Figure 3. Three-State Output Test Circuit**

Conditions: \( V^+ = V_{OH} = 5V \), \( V^- = V_{OL} = 0V \)
The LTC1045 consists of six voltage translators and associated control circuitry (see Block Diagram). Each translator has a linear comparator input stage with the positive input brought out separately. The negative inputs of the first four comparators are tied in common to VTRIP1 and the negative inputs of the last two comparators are tied in common to VTRIP2. With these inputs the switching point of the comparators can be set anywhere within the common mode range of V– to V+ – 2V. To improve noise immunity each comparator has a small built-in hysteresis. Hysteresis varies with bias current from 7mV at low bias current to 20mV at high bias current (see typical curve of Hysteresis vs RSET).

### Setting the Bias Current

Unlike CMOS logic, any linear CMOS circuit must draw some quiescent current. The bias generator (Block Diagram) allows the quiescent current of the comparators to be varied. Bias current is programmed with an external resistor (see typical curve of I+ vs RSET). As the bias current is decreased, the LTC1045 slows down (see typical curve of Delay Time vs RSET).

### Shutting Power Off and Latching the Outputs

In addition to setting the bias current, the ISET pin shuts power completely off and latches the translator outputs. To do this, the ISET pin must be forced to V+ – 0.5V. As shown in Figure 4, a CMOS gate or a TTL gate with a resistor pull-up does this quite nicely. Even though power is turned off to the linear circuitry, the CMOS output logic is powered and maintains the output state. With no DC load on the output, power dissipation, for all practical purposes, is zero.

Latching the output is fast—typically 80ns from the rising edge of ISET. Going from the latched to flow-through state is much slower—typically 1.5μs from the falling edge of ISET. This time is set by the comparator’s power-up time. During the power-up time, the output can assume false states. To avoid problems, the output should not be considered valid until 2μs to 5μs after the falling edge of ISET.

### Putting the Outputs in Hi-Z State

A DISABLE input sets the six outputs to a high impedance state. This allows the LTC1045 to be interfaced to a data bus. When DISABLE = “1” the outputs are high impedance and when DISABLE = “0” they are active. With TTL supplies, V+ = 4.5V to 5.5V and V– = GND, the DISABLE input is TTL compatible.

### Power Supplies

There are four power supplies on the LTC1045: V+, V–, VOH and VOL. They can be connected almost arbitrarily, but there are a few restrictions. A minimum differential must exist between V+ and V– and VOH and VOL. The V+ to V– differential must be at least 4.5V and the VOH to VOL differential must be at least 3V. Another restriction is caused by the internal parasitic diode D1 (see Figure 5).
APPLICATIONS INFORMATION

Because of this diode, \( V_{OH} \) must not be greater than \( V^+ \). Lastly, the maximum voltage between any two power supply pins must not exceed 15V operating or 18V absolute maximum. For example, if \( V^+ = 5V \), \( V^- \) or \( V_{OL} \) should be no more negative than \(-10V\). Note that \( V_{OL} \) should not be more negative than \(-10V\) even if the \( V_{OH} \) to \( V_{OL} \) differential does not exceed the 15V maximum. In this case the \( V^+ \) to \( V_{OL} \) differential sets the limit.

Input Voltage

The LTC1045 has no upper clamp diodes as do conventional CMOS circuits. This allows the inputs to exceed the \( V^+ \) supply. The inputs will break down approximately 30V above the \( V^- \) supply. If the input current is limited with 100k\( \Omega \), the input voltage can be driven to at least \(-50V\) with no adverse effects for any combination of allowed power supply voltages. Output levels will be correct even under these conditions (i.e., if the input voltage is above the trip point, the output will be high and if it is below, the output will be low).

Output Drive

Output drive characteristics of the LTC1045 will vary with the power supply voltages that are chosen. Output impedance is affected by \( V^+ \), \( V_{OH} \) and \( V_{OL} \). \( V^- \) has no effect on output impedance. Guaranteed drive characteristics are specified in the table of electrical characteristics for \( V^+ = V_{OH} = 5V \) and \( V^- = V_{OL} = 0V \). Figures 6 and 7 show relative output impedance for other supply combinations. In general, output impedance is minimized if \( V^+ \) to \( V_{OH} \) is minimized and \( V_{OH} \) to \( V_{OL} \) is maximized.

Figure 6. Relative Output Sourcing Resistance (\( R_{OH} \)) vs \( V^+ – V_{OH} \)

Figure 7. Relative Output Sinking Resistance (\( R_{OL} \)) vs \( V_{OH} – V_{OL} \)
TYPICAL APPLICATIONS

ECL to CMOS/TTL Logic

TTL/CMOS (VCC = 5V) to High Voltage CMOS (VCC = 15V)

High Voltage CMOS (VCC = 15V) to TTL/CMOS (VCC = 5V)
TYPICAL APPLICATIONS

TTL/CMOS (V\textsubscript{CC} = 5V) to Low Voltage CMOS (V\textsubscript{CC} = 3V)

TTL/CMOS Logic Levels to ±5V Analog Switch Driver

TTL/CMOS (V\textsubscript{CC} = 5V) to 10V/–5V Clock Driver
TYPICAL APPLICATIONS

Logic Ground Isolation when Two Grounds are within LTC1045 Common Mode Range

SYSTEM A

\[ V_{CC_A} = 5V \]

\[ V_{TRIP} = 1.35V \]

\[ V_{GND} = \text{GND A} \]

SYSTEM B

\[ V_{CC_B} = 5V \]

\[ V_{GND} = \text{GND B} \]

SETS LOGIC THRESHOLD REFERRED TO GND A

\[ (\text{GND B} - V^- + V_{TRIP}) \leq \text{GND A} \leq (\text{GND B} + V_{CC_B} - 2V - V_{TRIP}) \]

TTL/CMOS LOGIC

THREE-STATE BUFFER

30-FT RG 174 COAX CABLE

50Ω

0.2V

Coax Cable Driver/Receiver

RCV OUT (5V/DIV)

RCV IN (1V/DIV)

XMT OUT (1V/DIV)

XMT IN (5V/DIV)

200ns/DIV
TYPICAL APPLICATIONS

±5V Analog Switch Driver

- TTL OR CMOS LOGIC INPUTS
- LTC1045
- CD4016
- SW A
- SW B
- SW C
- SW D
- 100k
- VOL
- 1.5V
- 5V
- -5V
- 20
Logic Systems DC Isolation

- SET $V_{TRIP}$ TO HALF WAY BETWEEN $V_{OH}$ AND $V_{OL}$ OF SYSTEM A
- **SHUNTS COMMON MODE SIGNAL
- † PROVIDES LEAKAGE PATH FOR TOTALLY ISOLATED SYSTEMS
TYPICAL APPLICATIONS

24V Relay Supply from 12V/15V Supply

RS232 Receiver

NOTE: INPUTS HAVE NO INTERNAL PULL-DOWN
LED Driver

V+ 5V TO 15V

1 V+IN
2 IN1 OUT1
3 IN2 OUT2
4 IN3 OUT3
5 IN4 OUT4
6 IN5 OUT5
7 IN6 OUT6
8 VTRIP2 DIS
9 VTRIP1 ISET
10 V–
11 V–
12 100k
13 2N2222
14 2N2905 (USE HEAT SINK)
15 V+ 5V
16 2N2222
17 2N2222
18 2N2222
19 2N2222
20 2N2222

REF LED

(ADJUSTS LED CURRENT)

(ADJUSTS LED CURRENT)

REGulates LED CURRENT

V+ 5V 1.5V

100Ω
**TYPICAL APPLICATIONS**

Multiwindow Comparator and Display

**Symbols:**
- **V**
- **IN**
- **OUT**
- **V**
- **VH**
- **VL**
- **R**
- **VREF**
- **VIN**
- **VTRIP**
- **ISET**
- **DIS**
- **5V**
- **V+**
- **V–**
- **V**

**Equations:**
- \( V_{IN} \leq V^+ - 2 \)
- \( R = \frac{100(V_{REF} - V_H)}{(V_H - V_L)} \)
- \( (V_H - V_L) \geq 0.5V \)

**Notes:**
- 

* For LED current control
See LTC1045 LED driver
ECL to CMOS from Single 5V Supply

1045 TA16
J Package
20-Lead CERDIP (Narrow .300 Inch, Hermetic)
(Reference LTC DWG # 05-08-1110)

NOTE: LEAD DIMENSIONS APPLY TO SOLDER DIP/PLATE OR TIN PLATE LEADS

PACKAGE DESCRIPTION

OBSOLETE PACKAGE
N Package
20-Lead PDIP (Narrow .300 Inch)
(Reference LTC DWG # 05-08-1510)

*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)
SW Package
20-Lead Plastic Small Outline (Wide .300 Inch)
(Reference LTC DWG # 05-08-1620)

NOTE 1

1. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS.
THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE
TYPICAL APPLICATION

Power MOSFET Driver Low Power Consumption Stepper Motor Driver

RELATED PARTS

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
<th>COMMENTS</th>
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<tbody>
<tr>
<td>LT1016</td>
<td>Ultrafast Precision Comparator</td>
<td>10ns Propagation Delay</td>
</tr>
<tr>
<td>LT1039</td>
<td>Triple RS232 Driver/Receiver with Shutdown</td>
<td>±12V Supply, No Supply Current in Shutdown</td>
</tr>
<tr>
<td>LTC1440/LTC1441/LTC1442</td>
<td>Ultralow Power, Single/Dual Comparator with Reference</td>
<td>2.8μA Supply Current</td>
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