The LTC®-1043 is a monolithic, charge-balanced, dual switched capacitor instrumentation building block. A pair of switches alternately connects an external capacitor to an input voltage and then connects the charged capacitor across an output port. The internal switches have a break-before-make action. An internal clock is provided and its frequency can be adjusted with an external capacitor. The LTC1043 can also be driven with an external CMOS clock.

The LTC1043, when used with low clock frequencies, provides ultra precision DC functions without requiring precise external components. Such functions are differential voltage to single-ended conversion, voltage inversion, voltage multiplication and division by 2, 3, 4, 5, etc. The LTC1043 can also be used for precise V–F and F–V circuits without trimming, and it is also a building block for switched capacitor filters, oscillators and modulators.

The LTC1043 is manufactured using Linear Technology’s enhanced LTCMOS™ silicon gate process.

LTC and LT are registered trademarks of Linear Technology Corporation.
LTCMOS is a trademark of Linear Technology Corporation.


**LTC1043**

**ABSOLUTE MAXIMUM RATINGS**

(Note 1)

Supply Voltage ........................................................ 18V

Input Voltage at Any Pin ........ –0.3V ≤ V_IN ≤ V+ + 0.3V

Operating Temperature Range

LTC1043C ................................... –40°C ≤ T_A ≤ 85°C

LTC1043M (OBSCLETE).............–55°C ≤ T_A ≤ 125°C

Storage Temperature Range ................. –65°C to 150°C

Lead Temperature (Soldering, 10 sec).............. 300°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

**ELECTRICAL CHARACTERISTICS**

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V+ = 10V, V− = 0V, LTC1043M operates from –55°C ≤ T_A ≤ 125°C; LTC1043C operates from –40°C ≤ T_A ≤ 85°C, unless otherwise noted.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>LTC1043M</th>
<th>LTC1043C</th>
</tr>
</thead>
<tbody>
<tr>
<td>I_S</td>
<td>Power Supply Current</td>
<td>Pin 16 Connected High or Low</td>
<td>● 0.25 0.4 0.7</td>
<td>● 0.25 0.4 0.7</td>
</tr>
<tr>
<td></td>
<td></td>
<td>COSC (Pin 16 to V−) = 100pF</td>
<td>● 0.4 0.65 1</td>
<td>● 0.4 0.65 1</td>
</tr>
<tr>
<td>I_I</td>
<td>OFF Leakage Current</td>
<td>Any Switch, Test Circuit 1 (Note 2)</td>
<td>● 6 100 6</td>
<td>● 6 100 6</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Any Switch, Test Circuit 2</td>
<td>● 240 400 700</td>
<td>● 240 400 700</td>
</tr>
<tr>
<td>R_ON</td>
<td>ON Resistance</td>
<td>Test Circuit 2, V_IN = 7V, I = ±0.5mA</td>
<td>● V+ = 10V, V− = 0V</td>
<td>●</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Test Circuit 2, V_IN = 3.1V, I = ±0.5mA</td>
<td>● V+ = 5V, V− = 0V</td>
<td>●</td>
</tr>
<tr>
<td>fOSC</td>
<td>Internal Oscillator Frequency</td>
<td>COSC (Pin 16 to V−) = 0pF</td>
<td>● 20 34 50</td>
<td>● 20 34 50</td>
</tr>
<tr>
<td></td>
<td></td>
<td>COSC (Pin 16 to V−) = 100pF</td>
<td>● 15 75 15</td>
<td>● 15 75 15</td>
</tr>
<tr>
<td>fOSC</td>
<td>Pin Source or Sink Current</td>
<td>Pin 16 at V+ or V−</td>
<td>● 40 70 100</td>
<td>● 40 70 100</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Break-Before-Make Time</td>
<td>25 25 ns</td>
<td>25 25 ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Clock to Switching Delay</td>
<td>75 75 ns</td>
<td>75 75 ns</td>
</tr>
<tr>
<td>fM</td>
<td>Max External CLK Frequency</td>
<td>COSC Pin Externally Driven</td>
<td>5 5 MHz</td>
<td>5 5 MHz</td>
</tr>
<tr>
<td>CMRR</td>
<td>Common Mode Rejection Ratio</td>
<td>V+ = 5V, V− = –5V, –5V &lt; V_CM &lt; 5V</td>
<td>DC to 400Hz</td>
<td>DC to 400Hz</td>
</tr>
</tbody>
</table>

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

**Note 2:** OFF leakage current is guaranteed but not tested at 25°C.
TYPICAL PERFORMANCE CHARACTERISTICS
(Test Circuits 2 through 4)

Power Supply Current vs Power Supply Voltage

Ron vs Vin

Ron (Peak) vs Power Supply Voltage and Temperature

Oscillator Frequency, fosc vs Cosc

Oscillator Frequency, fosc vs Supply Voltage

Normalized Oscillator Frequency, fosc vs Supply Voltage
### Typical Performance Characteristics

#### Oscillator Frequency, $f_{Osc}$ vs Ambient Temperature, $T_A$

- Plot showing $f_{Osc}$ vs $T_A$.
- Key points: $V^+ = 10V, V^- = 0V$ and $V^+ = 15V, V^- = 0V$.

#### C_{Osc} Pin ISINK, ISOURCE vs Supply Voltage

- Plot showing ISINK, ISOURCE vs $V_{SUPPLY}$.
- Key points: $T_A = 25°C$.

#### Break-Before-Make Time, $t_{NOV}$, vs Supply Voltage

- Plot showing $t_{NOV}$ vs $V_{SUPPLY}$.
- Key points: $T_A = 25°C$.

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### Block Diagram

- Diagram of the LTC1043 block diagram.
- The switches are timed as shown with pin 16 high.

---

THE CHARGE BALANCING CIRCUITRY SAMPLES THE VOLTAGE AT S3 WITH RESPECT TO S4 (PIN 16 HIGH) AND INJECTS A SMALL CHARGE AT THE C+ PIN (PIN 16 LOW). THIS BOOSTS THE CMRR WHEN THE LTC1043 IS USED AS AN INSTRUMENTATION AMPLIFIER FRONT END.

FOR MINIMUM CHARGE INJECTION IN OTHER TYPES OF APPLICATIONS, S3A AND S3B SHOULD BE GROUNDED.
Common Mode Rejection Ratio (CMRR)

The LTC1043, when used as a differential to single-ended converter rejects common mode signals and preserves differential voltages (Figure 1). Unlike other techniques, the LTC1043’s CMRR does not degrade with increasing common mode voltage frequency. During the sampling mode, the impedance of Pins 2, 3 (and 11, 12) should be reasonably balanced, otherwise, common mode signals will appear differentially. The value of the CMRR depends on the value of the sampling and holding capacitors \(C_S, C_H\) and on the sampling frequency. Since the common mode voltages are not sampled, the common mode signal frequency can well exceed the sampling frequency without experiencing aliasing phenomena. The CMRR of Figure 1 is measured by

\[
\text{CMRR} = 20 \log \left( \frac{V_{VOut}}{V_{VOut}} \right)
\]

\(\text{FOR OPTIMUM CMRR, THE } C_{\text{OSC}} \text{ SHOULD BE LARGER THAN } 0.0047 \mu F, \text{ AND THE SAMPLING CAPACITOR ACROSS PINS 11 AND 12 SHOULD BE PLACED OVER A SHIELD TIED TO PIN 10.}\)
shorting Pins 7 and 13 and by observing, with a precision DVM, the change of the voltage across \( C_H \) with respect to an input CM voltage variation. During the sampling and holding mode, charges are being transferred and minute voltage transients will appear across the holding capacitor. Although the \( R_{\text{ON}} \) on the switches is low enough to allow fast settling, as the sampling frequency increases, the rate of charge transfer increases and the average voltage measured with a DVM across it will increase proportionally; this causes the CMRR of the sampled data system, as seen by a “continuous” instrument (DVM), to decrease (Figure 2).

**Switch Charge Injection**

Figure 3 shows one out of the eight switches of the LTC1043, configured as a basic sample-and-hold circuit. When the switch opens, a “hold step” is observed and its magnitude depends on the value of the input voltage. Figure 4 shows charge injected into the hold capacitor. For instance, a 2\( pF \) charge injected into a 0.01\( \mu F \) capacitor causes a 200\( \mu V \) hold step. As shown in Figure 4, there is a predictable and repeatable charge injection cancellation when the input voltage is close to half the supply voltage of the LTC1043. This is a unique feature of this product, containing charge-balanced switches fabricated with a self-aligning gate CMOS process. Any switch of the LTC1043, when powered with symmetrical dual supplies, will sample-and-hold small signals around ground without any significant error.

**Shielding the Sampling Capacitor for Very High CMRR**

Internal or external parasitic capacitors from the \( C^+ \) pin(s) to ground affect the CMRR of the LTC1043 (Figure 1). The common mode error due to the internal junction capacitances of the \( C^+ \) Pin(s) 2 and 11 is cancelled through internal circuitry. The \( C^+ \) pin, therefore, should be used as the top plate of the sampling capacitor. The interpin capacitance between pin 2 and dummy Pin 1 (11 and 10) appears in parallel with the sampling capacitor so it does not degrade the CMRR. A shield placed underneath the sampling capacitor and connected to either Pin 1 or 3 helps to boost the CMRR in excess of 120dB (Figure 5).

Excessive external parasitic capacitance between the \( C^- \) pins and ground indirectly degrades CMRR; this becomes visible especially when the LTC1043 is used with clock frequencies above 2kHz. Because of this, if a shield is used, the parasitic capacitance between the shield and circuit ground should be minimized.

It is recommended that the outer plate of the sampling capacitor be connected to the \( C^- \) pin(s).

**Input Pins, SCR Sensitivity**

An internal 60\( \Omega \) resistor is connected in series with the input of the switches (Pins 5, 6, 7, 8, 13, 14, 15, 18) and it is included in the \( R_{\text{ON}} \) specification. When the input voltage exceeds the power supply by a diode drop, current will flow into the input pin(s). The LTC1043 will not latch until the input current reaches 2mA–3mA. The device will...
recovery from the latch mode when the input drops 3V to 4V below the voltage value which caused the latch. For instance, if an external resistor of 200Ω is connected in series with an input pin, the input can be taken 1.3V above the supply without latching the IC. The same applies for the C+ and C− pins.

**COSC Pin (16), Figure 6**

The Cosc pin can be used with an external capacitor, Cosc, connected from Pin 16 to Pin 17, to modify the internal oscillator frequency. If Pin 16 is floating, the internal 24pF capacitor, plus any external interpin capacitance, set the oscillator frequency around 190kHz with ±5V supply. The typical performance characteristics curves provide the necessary information to set the oscillator frequency for various power supply ranges. Pin 16 can also be driven with an external clock to override the internal oscillator. Although standard 7400 series CMOS gates do not guarantee CMOS levels with the current source and sink requirements of Pin 16, they will in reality drive the Cosc pin. CMOS gates conforming to standard B series output drive have the appropriate voltage levels and more than enough output current to simultaneously drive several LTC1043 COSC pins. The typical trip levels of the Schmitt trigger (Figure 6) are given below.

<table>
<thead>
<tr>
<th>SUPPLY</th>
<th>TRIP LEVELS</th>
</tr>
</thead>
<tbody>
<tr>
<td>V+ = 5V, V− = 0V</td>
<td>VH = 3.4VVL = 1.35V</td>
</tr>
<tr>
<td>V+ = 10V, V− = 0V</td>
<td>VH = 6.5VVL = 2.8V</td>
</tr>
<tr>
<td>V+ = 15V, V− = 0V</td>
<td>VH = 9.5VVL = 4.1V</td>
</tr>
</tbody>
</table>

![Figure 4. Individual Switch Charge Injection vs Input Voltage](image001.png)

![Figure 5. Printed Circuit Board Layout Showing Shielding the Sampling Capacitor](image002.png)

![Figure 6. Internal Oscillator](image003.png)
**Divide by 2**

- \( V_{OUT} = \frac{V_{IN}}{2} \pm 1 \text{ ppm} \)
- \( 0 \leq V_{IN} = V^+ \)
- \( 3 \leq V^+ \leq 18V \)

**Multiply by 2**

- \( V_{OUT} = 2V_{IN} \pm 5 \text{ ppm} \)
- \( 0 \leq V_{IN} = \frac{V^+}{2} \)
- \( 3 \leq V^+ \leq 18V \)

**Ultra Precision Voltage Inverter**

- \( V_{OUT} = -V_{IN} \pm 2 \text{ ppm} \)
- \( V^- < V_{IN} < V^+ \)
- \( V^+ = +5V, V^- = -5V \)

**Precision Multiply by 3**

- \( V_{OUT} = 3V_{IN} \pm 10 \text{ ppm} \)
- \( 0 < V_{IN} < V^+/3 \)
- \( 3V < V^+ < 18V \)

**Precision Multiply by 4**

- \( V_{OUT} = 4V_{IN} \pm 40 \text{ ppm} \)
- \( 0 \leq V_{IN} = V^+/4 \)
- \( 3V < V^+ < 18V \)

**Divide by 3**

- \( V_{OUT} = \frac{V_{IN}}{3} \pm 3 \text{ ppm} \)
- \( 0 \leq V_{IN} = V^+ \)
- \( 3V < V^+ < 18V \)
TYPICAL APPLICATIONS

Divide by 4

\[ V_{IN} \leq V_{OUT} = V_{IN}/4 \pm 5 \text{ppm} \]

0.005% V/F Converter

0.01% Analog Multiplier

OPERATE LTC1043 FROM ±5V
† POLYSTYRENE, MOUNT CLOSE
†† 1% FILM RESISTOR
ADJUST OUTPUT TRIM
50 X + Y = OUTPUT ± 0.01%

††† ± 0.01%

FOR START-UP
**Single 5V Supply, Ultra Precision Instrumentation Amplifier**

- **Input and Output Voltage Range**: Includes ground.
- **Input Referred Offset Errors**: Typically 3µV with 1µV of noise.
- **CMRR**: ~120dB

**Voltage Controlled Current Source with Ground Referenced Input and Output**

- **Operates from a Single 5V Supply**
- **Input Voltage**: 5V to 2V

**Precision Instrumentation Amplifier**

- **Offset**: 10µV
- **Drift**: 0.1µV/°C
- **Full Differential Input CMRR**: 150dB
- **Open Loop Gain**: >10^8
- **Gain**: \( \frac{R_2}{R_1} + 1 \)
- **Bias Current**: 1nA

- **Scheme Diagram**

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**Notes**

- LTC1043
- TYPICAL APPLICATIONS

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**Linear Technology**
LOCK-IN AMPLIFIER (= EXTREMELY NARROW-BAND AMPLIFIER)

50MHz Termal RMS/DC Converter

2% ACCURACY DC 50MHz
100:1 CREST FACTOR CAPABILITY
T1 TO T2 = YELLOW SPRINGS INST. CO.
THERMISTOR COMPOSITE
ENCLOSE T1 AND T2 IN STYROFOAM

T1 = TF5SX17ZZ, TOROTEL
Rf = VISHAY S-102
≈ 6.19k AT 37.5°C
MATCH 0.05% 6.19k = VISHAY S-102
OPERATE LTC1043 WITH ±5V SUPPLIES

LOCK-IN AMPLIFIER TECHNIQUE
USED TO EXTRACT VERY SMALL SIGNALS BURIED INTO NOISE

LTC1043 • A013

1/4 LTC1043

MATCH 0.05% 6.19k = VISHAY S-102
OPERATE LTC1043 WITH ±5V SUPPLIES

LOCK-IN AMPLIFIER TECHNIQUE
USED TO EXTRACT VERY SMALL SIGNALS BURIED INTO NOISE
**TYPICAL APPLICATIONS**

**Quad Single 5V Supply, Low Hold Step, Sample-and-Hold**

1. 5V
2. OUTPUT
3. 1/4 LTC1014
4. NC
5. VIN
6. OUTPUT
7. 1/4 LTC1014
8. NC
9. VIN
10. OUTPUT
11. 1/4 LTC1014
12. NC
13. VIN
14. OUTPUT
15. 1/4 LTC1014
16. NC
17. VIN
18. OUTPUT

For 1V \( \leq V_{IN} \leq 4V \), the hold step is \( \leq 300 \mu V \)

Acquisition time \( \approx 8 \times R_{ON} \) for 10-bit accuracy

**Single Supply Precision Linearized Platinum RTD Signal Conditioner**

1. 5V
2. 10k*
3. 1k
4. 2.74k*
5. 2.4k
6. 50k zero adjust
7. 5V
8. 250k* (linearity correction loop)
9. 2.5V
10. LT1009
11. 2.9V
12. 8.25k*
13. 10k*
14. 3
15. 2
16. 4
17. 1
18. 8

\( R_p = \text{ROSEMOunt 118MFRTD} \)

*1% Film Resistor

Trim sequence:
- Set sensor to 0°C value. Adjust zero for 0V out
- Set sensor to 100°C value. Adjust gain for 1,000V out
- Set sensor to 400°C value. Adjust linearity for 4,000V out
- Repeat as required
TYPICAL APPLICATIONS

High Frequency Clock Tunable Bandpass Filter

BANDPASS CENTER FREQUENCY \( f_0 = \frac{f_{CLK}}{3\pi \sqrt{\frac{R_2}{R_1}}} \)

\( Q \approx \frac{R_0}{R_1} \sqrt{\frac{R_2}{R_1}} \\
\)

\( f_{0\text{ MAX}} \leq 1000\text{Hz} \)

\( Q_{\text{MAX AT 10kHz}} f_0 < 10 \)

\( f_0 \times Q \leq 1\text{MHz} \)

\( f_{CLK} \text{ MAX} \leq 3\text{MHz}, Q < 2 \)

0.005% F/V Converter

\*75k = TRW # MTR-5/120ppm
**TYPICAL APPLICATIONS**

### Frequency-Controlled Gain Amplifier

- **Gain Control:**
  - 0kHz to 10kHz = Gain 0 to 1000

- **For Differential Input:**
  - Ground pin 8A and use pins 13A and 7A for inputs
  - Gain = \( f_{in} \times 0.01\mu F \); gain is negative as shown

- **For Single-Ended Input and Positive Gain:**
  - Ground pin 8A and use pin 7A for input

- **Use ±5V Supplies for LTC1043**

### Relative Humidity Sensor Signal Conditioner

- **Gain =**
- **GAIN IS NEGATIVE AS SHOWN**

- **Output:**
  - 0V to 1V = 0% to 100%

- **Sensor:**
  - Panametrics # RHS
  - \( \approx 500\mu F \) at RH = 76%
  - \( 1.7 \mu F/%RH \)

- **Use ±5V Supplies for LTC1043**
**TYPICAL APPLICATIONS**

Linear Variable Differential Transformer (LVDT), Signal Conditioner

![Precision Current Sensing in Supply Rails](image)

**Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.**
PACKAGE DESCRIPTION

18-Lead Side Brazed (Hermetic) (Reference LTC DWG # 05-08-1210)

N Package
18-Lead PDIP (Narrow .300 Inch) (Reference LTC DWG # 05-08-1510)

SW Package
18-Lead Plastic Small Outline (Wide .300 Inch) (Reference LTC DWG # 05-08-1620)