FEATURES
- Micropower
  1.5µW (1 Sample/Second)
- Power Supply Flexibility
  Single Supply 2.8V to 16V
  Split Supply ±2.8V to ±8V
- Guaranteed Max Offset 0.75mV
- Guaranteed Max Tracking Error Between Input Pairs ± 0.1%
- Input Common Mode Range to Both Supply Rails
- TTL/CMOS Compatible with ±5V or Single 5V Supply
- Input Errors are Stable with Time and Temperature

APPLICATIONS
- Battery-Powered Systems
- Remote Sensing
- Window Comparator
- BANG-BANG Controllers

DESCRIPTION
The LTC®-1040 is a monolithic CMOS dual comparator manufactured using Linear Technology’s enhanced LTCMOS™ silicon gate process. Extremely low operating power levels are achieved by internally switching the comparator ON for short periods of time. The CMOS output logic holds the output information continuously while not consuming any power.

In addition to switching power ON, a switched output is provided to drive external loads during the comparator’s active time. This allows not only low comparator power, but low total system power.

Sampling is controlled by an external strobe input or an internal oscillator. The oscillator frequency is set by an external RC network.

Each comparator has a unique input structure, giving two differential inputs. The output of the comparator will be high if the algebraic sum of the inputs is positive and low if the algebraic sum of the inputs is negative.

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Window Comparator with Symmetric Window Limits

A OUT = “1” WHEN VIN > VC + Δ

A + B = “1” WHEN VC – Δ ≤ VIN ≤ VC + Δ

B OUT = “1” WHEN VIN < VC – Δ

---

Typical LTC1040 Supply Current vs Sampling Frequency

Supply Current, IS (µA)

0.01 0.1 1 10 100 1,000 10,000

SAMPLING FREQUENCY, fS (Hz)

0.1 1 10 100 1,000 10,000

V S = ±5V

Rext = 10M

EXTERNALLY STROBED
**LTC1040**

### Absolute Maximum Ratings (Note 1)
- **Total Supply Voltage (V+ to V–)**: 18V
- **Input Voltage**: (V+ + 0.3V) to (V– – 0.3V)
- **Operating Temperature Range**
  - LTC1040C: –40°C ≤ TA ≤ 85°C
  - LTC1040M (OBSOLETE): –55°C to 125°C
- **Storage Temperature Range**: –55°C to 150°C
- **Lead Temperature (Soldering, 10 sec)**: 300°C
- **Output Short-Circuit Duration**: Continuous

### Package/Order Information

#### TOP VIEW

- N PACKAGE
  - 18-LEAD PDIP
  - TJMAX = 150°C, qJA = 80°C/W (N)

- J PACKAGE
  - 18-LEAD CERDIP
  - TJMAX = 150°C, qJA = 80°C/W

- SW PACKAGE
  - 18-LEAD PLASTIC SO WIDE
  - TJMAX = 110°C, qJA = 120°C/W (N)
  - TJMAX = 125°C, qJA = 85°C/W (SW)

#### ORDER PART NUMBER
- LTC1040CN
- LTC1040CSW
- LTC1040MJ
- LTC1040CJ

### OBSOLETE PACKAGE
Consider the N18 Package as an Alternate Source
Consult LTC Marketing for parts specified with wider operating temperature ranges.

### Electrical Characteristics

- **VOS (Offset Voltage)**: 
  - Split Supplies: ±2.8V to ±6V
  - Single Supply (V– = GND): 2.8V to 6V
  - Specifications: ±0.3 to ±0.75 mV

- **Tracking Error Between Input Pairs**: 
  - Split Supplies: ±2.8V to ±8V
  - Single Supply (V– = GND): 6V to 15V
  - Specifications: 0.05 to 0.1%

- **IBIAS (Input Bias Current)**: 
  - OSC = GND
  - Specifications: ≤0.3 nA

- **RIN (Average Input Resistance)**: 
  - fS = 1kHz (Note 4)
  - Specifications: 20 to 30 MΩ

- **CMR (Common Mode Range)**: 
  - Specifications: V– to V+

- **PSR (Power Supply Range)**: 
  - Specifications: ±2.8

- **IS(ON) (Power Supply ON Current)**: 
  - Specifications: 1.2 to 3 mA

- **IS(OFF) (Power Supply OFF Current)**: 
  - Specifications: 0.001 to 0.5 μA

- **tD (Response Time)**: 
  - Specifications: 60 to 100 μs

- **VOL (Logic “0” Output Voltage)**: 
  - Specifications: ≤0.25 V

- **VOH (Logic “1” Output Voltage)**: 
  - Specifications: ≥2.4 V

- **V + = 5V, V– = –5V, unless otherwise noted.**
**ELECTRICAL CHARACTERISTICS**

The ● denotes the specifications which apply over the full operating temperature range otherwise specifications are at \( T_A = 25^\circ C \). Test conditions: \( V^+ = 5V, V^- = -5V \), unless otherwise specified.

### Typical Performance Characteristics

**Peak Supply Current vs Supply Voltage**

**Normalized Sampling Frequency vs Supply Voltage and Temperature**

**Sampling Rate vs \( R_{EXT}, C_{EXT} \)**

**Response Time vs Supply Voltage**

**Input Resistance vs Sampling Frequency**

**Vp-P Output Voltage vs Load Current**

---

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

**Note 2:** Applies over input voltage range limit and includes gain uncertainty.

**Note 3:** Tracking error = \((V_{IN1} – V_{IN2})/ V_{IN1}\).

**Note 4:** \( R_{IN} \) is guaranteed by design and is not tested. \( R_{IN} = 1/(f_S \times 33pF) \).

**Note 5:** Average supply current = \( t_D \times I_{S(ON)} + (1 – t_D \times f_S) \times I_{S(OFF)} \).

**Note 6:** Response time is set by an internal oscillator and is independent of overdrive voltage.

**Note 7:** Inputs and outputs also capable of meeting EIA/JEDEC B series CMOS specifications.
**TYPICAL PERFORMANCE CHARACTERISTICS**

**Response Time vs Temperature**

<table>
<thead>
<tr>
<th>AMBIENT TEMPERATURE, $T_A$ ($°C$)</th>
<th>RESPONSE TIME, $t_D$ ($\mu$s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-50</td>
<td>40</td>
</tr>
<tr>
<td>-25</td>
<td>50</td>
</tr>
<tr>
<td>0</td>
<td>60</td>
</tr>
<tr>
<td>25</td>
<td>70</td>
</tr>
<tr>
<td>50</td>
<td>80</td>
</tr>
<tr>
<td>75</td>
<td>90</td>
</tr>
<tr>
<td>100</td>
<td>100</td>
</tr>
<tr>
<td>125</td>
<td>120</td>
</tr>
</tbody>
</table>

$V^+ = 5V$

**Quick Hookup Guide**

**Self-Oscillating**

- $V^+$
- $C_{EXT}$
- $R_{EXT}$

**External Strobe**

- $V^+$

**TEST CIRCUIT**

All inputs on opposite comparator at ground

**BLOCK DIAGRAM**

- $V_{IN1}$
- $V_{IN2}$
- $B1^+$
- $B1^-$
- $B2^+$
- $B2^-$
- $STROBE$
- $OSC$
- $AOUT$
- $ON/OFF$
- $A + B$
- $B_{OUT}$
- $VP-p$ circuit
- $V_{p-p}$
- $GND$
**APPLICATIONS INFORMATION**

The LTC1040 uses sampled data techniques to achieve its unique characteristics. Some of the experience acquired using classic linear comparators does not apply to this circuit, so a brief description of internal operation is essential to proper application.

The most obvious difference between the LTC1040 and other comparators is the dual differential input structure. Functionally, when the sum of inputs is positive, the comparator output is high and when the sum of the inputs is negative, the output is low. This unique input structure is achieved with CMOS switches and a precision capacitor array. Because of the switching nature of the inputs, the concept of input current and input impedance needs to be examined.

The equivalent input circuit is shown in Figure 1. Here, the input is being driven by a resistive source, \( R_S \), with a bypass capacitor, \( C_S \). The bypass capacitor may or may not be needed, depending on the size of the source resistance and the magnitude of the input voltage, \( V_{IN} \).

![Figure 1. Equivalent Input Circuit](image)

For \( R_S < 10k\Omega \)

Assuming \( C_S \) is zero, the input capacitor, \( C_{IN} \), charges to \( V_{IN} \) with a time constant of \( R_S \cdot C_{IN} \). When \( R_S \) is too large, \( C_{IN} \) does not have a chance to fully charge during the sampling interval (\( \approx 80\mu s \)) and errors will result. If \( R_S \) exceeds \( 10k\Omega \), a bypass capacitor is necessary to minimize errors.

For \( R_S > 10k\Omega \)

For \( R_S \) greater than \( 10k\Omega \), \( C_{IN} \) cannot fully charge and a bypass capacitor, \( C_S \), is needed. When switch S1 closes, charge is shared between \( C_S \) and \( C_{IN} \). The change in voltage on \( C_S \) because of this charge sharing is:

\[
\Delta V = V_{IN} \cdot \frac{C_{IN}}{C_{IN} + C_S}
\]

This represents an error and can be made arbitrarily small by increasing \( C_S \).

With the addition of \( C_S \), a second error term caused by the finite input resistance of the LTC1040 must be considered. Switches S1 and S2 alternately open and close, charging and discharging \( C_{IN} \) between \( V_{IN} \) and ground. The alternate charge and discharge of \( C_{IN} \) causes a current to flow into the positive input and out of the negative input. The magnitude of this current is:

\[
I_{IN} = q \cdot f_S = \frac{V_{IN} \cdot C_{IN} \cdot f_S}{C_{IN} + C_S}
\]

where \( f_S \) is the sampling frequency. Because the input current is directly proportional to input voltage, the LTC1040 can be said to have an average input resistance of:

\[
R_{IN} = \frac{V_{IN}}{I_{IN}} = \frac{1}{f_S \cdot C_{IN}} = \frac{1}{f_S \cdot 33\mu F}
\]

(see typical curve of Input Resistance vs Sampling Frequency). A voltage divider is set up between \( R_S \) and \( R_{IN} \) causing error.

The input voltage error caused by these two effects is:

\[
V_{ERROR} = V_{IN} \left( \frac{C_{IN}}{C_{IN} + C_S} + \frac{R_S}{R_S + R_{IN}} \right)
\]

Example: \( f_S = 10Hz \), \( R_S = 1M\Omega \), \( C_S = 1\mu F \), \( V_{IN} = 1V \)

\[
V_{ERROR} = 1V \left( \frac{33 \cdot 10^{-12}}{1 \cdot 10^{-6} + \frac{10^6}{10^6 + 3 \cdot 10^9}} \right)
\]

\[
= 33\mu V + 330\mu V = 363\mu V.
\]

Notice that most of the error is caused by \( R_{IN} \). If the sampling frequency is reduced to 1Hz, the voltage error is reduced to 66\mu V.
**Minimizing Comparison Errors**

The two differential input voltages, \( V_1 \) and \( V_2 \), are converted to charge by the input capacitors \( C_{IN1} \) and \( C_{IN2} \) (see Figure 2). The charge is summed at the virtual ground point; if the net charge is positive, the comparator output is high and if negative, it is low. There is an optimum way to connect these inputs, in a specific application, to minimize error.

Ignoring internal offset, the LTC1040 will be at its switching point when:

\[
V_1 \cdot C_{IN1} + V_2 \cdot C_{IN2} = 0.
\]

Optimum error will be achieved when the differential voltages, \( V_1 \) and \( V_2 \), are individually minimized. Figure 3 shows two ways to connect the LTC1040 to compare an input voltage, \( V_{IN} \), to a reference voltage, \( V_{REF} \). Using the above equation, each method will be at null when:

(a) \((V_{REF} - 0V) \cdot C_{IN1} - (0V - V_{IN}) \cdot C_{IN2} = 0 \)

or \( V_{IN} = V_{REF} \cdot (C_{IN1}/C_{IN2}) \)

(b) \((V_{REF} - V_{IN}) \cdot C_{IN1} - (0V - 0V) \cdot C_{IN2} = 0 \)

or \( V_{IN} = V_{REF} \).

Notice that in method (a) the null point depends on the ratio of \( C_{IN1}/C_{IN2} \), but method (b) is independent of this ratio. Also, because method (b) has zero differential input voltage, the errors due to finite input resistance are negligible. The LTC1040 has a high accuracy capacitor array and even the non-optimum connection will only result in \( \pm 0.1\% \) more error, worst-case compared to the optimum connection.

**Tracking Error**

Tracking error is caused by the ratio error between \( C_{IN1} \) and \( C_{IN2} \) and is expressed as a percentage. For example, consider Figure 3a with \( V_{REF} = 1V \). Then at null,

\[
V_{IN} = V_{REF} \cdot \frac{C_{IN1}}{C_{IN2}} = 1V \pm 1mV
\]

because \( C_{IN1} \) is guaranteed to equal \( C_{IN2} \) to within \( 0.1\% \).

**Common Mode Range**

The input switches of the LTC1040 are capable of switching to either the \( V^+ \) or \( V^- \) supply. This means that the input common mode range includes both supply rails. Many applications, not feasible with conventional comparators, are possible with the LTC1040. In the load current detector shown in Figure 4, a 0.1\( \Omega \) resistor is used to sense the current in the \( V^+ \) supply. This application requires the dual differential input and common mode capabilities of the LTC1040.

![Figure 2. Dual Differential Equivalent Input Circuit](image)

![Figure 3. Two Ways to Do It](image)

![Figure 4. Load Current Detector](image)
**APPLICATIONS INFORMATION**

**Offset Voltage Error**

The errors due to offset, common mode, power supply variation, gain and temperature are all included in the offset voltage specification. This makes it easy to compute the error when using the LTC1040.

Example: error computation for Figure 4. Assume: $2.8V \leq V_S \leq 6V$.

Then total worst-case error is:

$$I_L (\text{ERROR}) = \pm (100mV \times 0.001 + 0.5mV) \times \frac{1A}{100mV} \pm 6mA$$

$$\uparrow \quad \uparrow$$

Tracking Error $V_{OS}$

$$I_L (\text{ERROR}) \% = \frac{6mA}{1A} \times 100 = \pm 0.6\%.$$ 

Note: If source resistance exceeds 10k, bypass capacitors should be used and the associated errors must be included.

**Pulsed Power ($V_{P-P}$) Output**

It is often desirable to use comparators with resistive networks such as bridges. Because of the extremely low power consumption of the LTC1040, the power consumed by these resistive networks can far exceed that of the device itself.

At low sample rates the LTC1040 spends most of its time off. To take advantage of this, a pulsed power ($V_{P-P}$) output is provided. $V_{P-P}$ is switched to $V^+$ when the comparator is on and to a high impedance (open circuit) when the comparator is off. The ON time is nominally 80$\mu$s. Figure 5 shows the $V_{P-P}$ output circuit.

The $V_{P-P}$ output voltage is not precise (see $V_{P-P}$ Output Voltage versus Load Current curve). There are two ways $V_{P-P}$ can be used to power external networks without excessive errors: (1) ratiometric networks and (2) fast settling references.

In a ratiometric network, the inputs are all proportional to $V_{P-P}$ (see Figure 6). Consequently, for small changes, the absolute value of $V_{P-P}$ does not affect accuracy.

It is critical that the inputs to the LTC1040 completely settle within 4$\mu$s of the start of the comparison cycle and that they do not change during the 80$\mu$s ON time. When driving resistive networks with $V_{P-P}$, capacitive loading on the network should be minimized to meet the 4$\mu$s settling time requirement. It is not recommended that $V_{P-P}$ be used to drive networks with source impedances, as seen by the inputs, of greater than 10k$\Omega$.

In applications where an absolute reference is required, the $V_{P-P}$ output can be used to drive a fast settling reference. The LT1009 2.5V reference, ideal in this application, settles in approximately 2$\mu$s (see Figure 7). The current through R1 must be large enough to supply the LT1009 minimum bias current (=1mA) and the load current, $I_L$. 

Figure 6. Ratiometric Network Driven by $V_{P-P}$

Figure 7. Driving Reference with $V_{P-P}$ Output
Output Logic

In addition to the normal outputs (A_OUT and B_OUT), two additional outputs, A + B and ON/OFF, are provided (see Figure 8 and Table 1). All logic is powered from V+ and ground, thus input and output logic levels are independent of the V- supply. The LTC1040 is directly compatible with CMOS logic and is TTL compatible for 4.75V ≤ V+ ≤ 5.25V. No external pull-up resistors are required.

Using External Strobe

A positive pulse on the strobe input, with the OSC input tied to ground, will initiate a comparison cycle. The STROBE input is edge-sensitive and pulse widths of 50ns will typically trigger the device.

Because of the sampling nature of the LTC1040, some sensitivity exists between the offset voltage and the falling edge of the input strobe. When the falling edge of the strobe signal falls within the comparator’s active time (80µs after rising edge), offset changes of as much as 2mV can occur. To eliminate this problem, make sure the strobe pulse width is greater than the response time, tD.

Using Internal Strobe

An internal oscillator allows the LTC1040 to strobe itself. The frequency of oscillation, and hence sampling rate, is set by an external RC network (see typical curve of Sampling Rate vs R_EXT, C_EXT).

For self-oscillation, the STROBE pin must be tied to ground. The external RC network is connected as shown in Figure 9.

To assure oscillation, R_EXT must be between 100k and 10M. There is no limit to the size of C_EXT.

R_EXT is very important in determining the power consumption. The average voltage at the oscillator pin is approximately V+ / 2. The power consumed by R_EXT is then: P_EXT = (V+ / 2)^2 / R_EXT.

Example: R_EXT = 1M, V+ 5V, P_EXT = (2.5)^2 / 10^6 = 6.25 • 10^-6W.

This is about four times the power consumed by the LTC1040 at V+ = 5V and f_S = 1 sample/second. Where power is a premium R_EXT should be made as large as possible. Note that the power consumed by R_EXT is not a function of f_S or C_EXT.
Complete Heating/Cooling Automatic Thermostat

Window Comparator with Independent Window Limits and Fully Floating Differential Input

Hysteresis Comparator with Fully Floating Differential Input

HYSTERESIS = 5V • 82k* = 20mV

† THERMISTOR # 44007
YELLOW SPRINGS INSTRUMENT CO., INC.

HYSTERESIS = 5V • 82k = 20mV

† HYSTERESIS = 5V • 82k = 20mV

† TO CENTER HYSTERESIS ABOUT VTRIP, FORCE THIS INPUT TO HYSTERESIS/2 (10mV)
The LTC1040 as a Linear Amplifier

With a simple RC filter, the LTC1040 can be made to function as a linear amplifier. By filtering the logic output and feeding it back to the negative input, the loop forces the output duty cycle \([t_{ON}/(t_{ON} + t_{OFF})]\) so that \(V_{OUT}\) equals \(V_{IN}\) (Figure 10).

The RC time constant is set to keep the ripple on the output small. The maximum output ripple is: \(\Delta V = V^*/f_S RC\) and should be set to 0.5mV to 1mV for best results. Notice that the higher the sampling frequency, \(f_S\), the lower RC can be. This is important because the RC filter also sets the loop response. A convenient way to keep \(f_S\) as high as possible under all conditions is to connect a 100k resistor to pin 16 (OSC) with no capacitance to ground.

![Figure 10. The LTC1040 as a Linear Amplifier](image)

2-Wire 0°C to 100°C Temperature Transducer with 4mA to 20mA Output

![Circuit Diagram](image)
J Package
18-Lead CERDIP (Narrow .300 Inch, Hermetic)
(Reference LTC DWG # 05-08-1110)

N Package
18-Lead PDIP (Narrow .300 Inch)
(Reference LTC DWG # 05-08-1510)
**TYPICAL APPLICATIONS**

**Analog Multiplier/Divider**

\[ V_{OUT} = \left( \frac{V_B + V_1 - V_2}{V_B} \right) \times V_C \]

**ACCURACY = \pm 10mV NO TRIM**

*V_B MUST BE > V_A + (V_1 – V_2)*

**Single + 5V Voltage-to-Frequency Converter**

\[ f_{OUT} (AVERAGE) = f_{IN} \left( \frac{V_{IN}}{V_{REF} \times 5V} \right) \]

\[ f_{OUT} = \frac{f_{IN}}{0.1\% \text{ FS}} \]

**PACKAGE DESCRIPTION**

**SW Package**

18-Lead Plastic Small Outline (Wide .300 Inch)

(Reference LTC DWG # 05-08-1620)

*NOTE:*
1. DIMENSIONS IN INCHES (MM) (NOTE 4)
2. DRAWING NOT TO SCALE
3. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS.
THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS.
4. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)