# SELECTED ITEM DRAWING

| | | | | |
|---|---|---|---|---|
| | | | ANALOG DEVICES | |
| Unless otherwise specified DIMENSIONS ARE IN INCHES (MM) | TOLERANCES:<br>.XX +/- 0.010<br>.XXX +/- 0.005<br>.XXXX +/- 0.002<br>ANGLES +/- .5 DEG | Drawing practices per **ASME Y14.100** | **28 Gbps, 5-Bit, Digital Time Delay with Programmable Output Voltage** | |
| | | | SIZE **A** | DRAWING NUMBER **SID000091** |





One Analog Way, Wilmington, MA 01887-2356, U.S.A.
Tel: 781.935.5565 www.analog.com
Tel: 800.262.5643

## 1. SCOPE

1.1. Scope

This drawing establishes the requirements for the non-hermetic, 28 Gbps, 5-Bit Digital Time Delay with Programmable Output Voltage, to be screened with guidelines to MIL-PRF-38535, Class Level S, to the requirements specified in 4.1, 4.2, and 4.3 herein.

1.2. Analog Devices Part Number

| Generic Part Number | Screened Part Number |
|---|---|
| ADH856S | HMC8693LC5 |

## 2. APPLICABLE DOCUMENTS

2.1. Government Documents

Unless otherwise specified, the following drawings and standards, of the issue in effect on the date of the accepted purchase order, in the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, shall form a part of this drawing to the extent specified herein.

**DEPARTMENT OF DEFENSE TEST METHOD STANDARD**

| | |
|---|---|
| MIL-STD-883 | Microcircuits |
| MIL-STD-1580C | Destructive Physical Analysis for Electronic, Electromagnetic, and Electromechanical Parts |

**DEPARTMENT OF DEFENSE PERFORMANCE SPECIFICATIONS**

| | |
|---|---|
| MIL-PRF-38535 | Integrated Circuits (Microcircuits) Manufacturing, General Specification For |

2.2. Non-Government Documents

The following documents, of the issue in effect on the date of the purchase order, form a part of this drawing to the extent specified herein:

**Analog Devices Inc.**

ADI Standard Space Products Program – ASD-*lite*.

| | | |
|---|---|---|
| HMC856LC5 Data Sheet | Commercial Product Datasheet | Rev. D (Reference Only) |

## 3. REQUIREMENTS

3.1. General Requirements
The devices delivered shall comply to this specification.

3.2. Design Construction and Physical Dimensions
The design construction and physical dimensions shall be as defined in Figure 1 herein.

3.3. Traceability
Each delivered device shall be traceable to a production lot. Inspection lot records shall be maintained to provide traceability of its origin.

3.4. DPA
If specified on Purchase Order, DPA testing shall be done in accordance with MIL-STD-1580C, Sections 16.1.

3.5. Burn-In and Life Test Circuit
The burn-in and life test circuit and conditions shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test methods 1005 and 1015 per MIL-STD-883.

## 4. QUALITY ASSURANCE PROVISIONS

4.1. Wafer Lot Acceptance Testing
Not applicable.

4.2. Flight Screening Requirements
Flight screening requirements shall be per MIL-STD-883 TM 5004 for Class Level S microcircuits modified for non-hermetic packaged MMIC devices.

4.2.1. Electrical Test Requirements
Electrical test requirements are defined in Table I herein.

4.2.2. Electrical Performance Characteristics
Electrical performance characteristics are specified on Table II herein.

4.3. Quality Conformance Inspection (QCI)
Group B and Group D tests shall be performed per MIL-STD-883 TM 5005 for Class Level S microcircuits modified for non-hermetic packaged MMIC devices.

4.3.1. Post Steady State Life Electrical Test
Post steady state life electrical tests shall consist of the tests specified per Table II tested at room temperature only. Devices must meet delta parameter requirements in accordance with Table III herein.

## 5. MIL-PRF-38535 ASD-LITE EXCEPTIONS

The manufacturing flow described in the ADI STANDARD SPACE PRODUCTS PROGRAM is to be considered a part of this specification.

5.1. Wafer Fabrication

Foundry information is available upon request.

5.2. Flight Screening Flow

Wafer lot Acceptance: Not applicable for non-hermetic air cavity packages.
Non-destruct Bond Pull: Not applicable for non-hermetic air cavity packages.
Serialization: Not performed.
Post Burn-In Delta Test: Not performed.
Internal visual inspection: DPA performed in lieu of visual – commercial criteria is applicable.
Seal, Fine Leak: Not applicable for non-hermetic air cavity packages.
Seal, Gross Leak: Not applicable for non-hermetic air cavity packages.

5.3. Group B

Subgroup 2: Resistance to solvents is not applicable.
Subgroup 3: Steam aging shall not be required for pre-conditioning.
Subgroup 4: Not applicable for non-hermetic air cavity packages.
Subgroup 5: Qty/Acc = 10/0.
Subgroup 6: Qty/Acc = 6/0.

5.4. Group D

Subgroup 2: Not applicable for non-hermetic air cavity packages.
Subgroup 5: Not Applicable for non-hermetic air cavity packages.
Subgroup 6: Not applicable for non-hermetic air cavity packages.
Subgroup 7: Not applicable for non-hermetic air cavity packages.
Subgroup 8: Not applicable for non-hermetic air cavity packages.
Subgroup 9: Not applicable for non-hermetic air cavity packages.

## 6. PREPARATION FOR DELIVERY

The preparation for delivery, packaging, preservation, ESD protection and handling shall be in accordance with MIL-PRF-38535.

6.1. Part Marking

Devices shall be marked as specified on Figure 1 herein.

6.2. Inspection Data Requirements

The following data shall accompany each shipment.

a. A Certificate of Conformance (C of C) certifies that the lot(s) meets all requirements of this specification.
b. DPA Report (if applicable).
c. Summary of electrical test requirements defined in 4.2 herein.
d. Summary of QCI results defined in 4.3 herein.
e. Failure Analysis with photos (If applicable).
f. A cover sheet indicating the following purchasing information:
    1. Customer purchase order number.
    2. Analog Devices part number.
    3. Part lot identification codes.
    4. Date & quantity shipped.

## TABLE I: ELECTRICAL TEST REQUIREMENTS

| Test Requirement | Subgroups (in accordance with MIL-PRF-38535, Table III) |
|---|---|
| Interim Electrical Parameters | 1, 4 |
| Final Electrical Parameters | 1, 4 1/2/ |
| Group A Electrical Parameters | 1, 2, 3, 4, 5, 6 |
| Group B End-Point Electrical Parameters | 1, 4 2/ |
| Group D End-Point Electrical Parameters | 1, 4 |

TABLE I Notes:
1/ PDA applies to Table I subgroup 1 and Table III delta parameters.
2/ See Table III for delta parameters

## TABLE II: ELECTRICAL PERFORMANCE CHARACTERISTICS (-40 °C, +25 °C AND +85 °C)

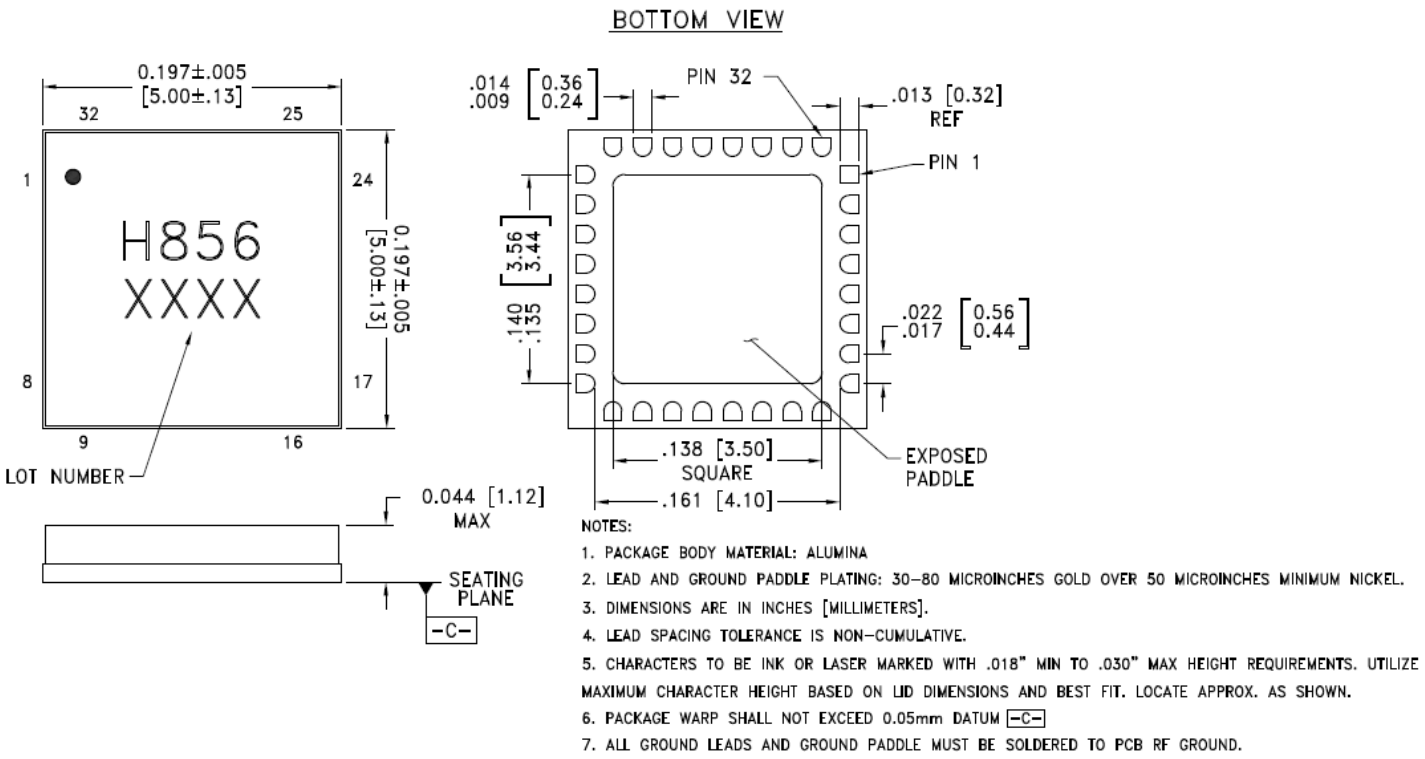
| Parameter | Test Conditions 1/4/ Unless otherwise specified | Group A Subgroups | Limits | | Units |
|---|---|---|---|---|---|
| | | | Min | Max | |
| VEE Power Supply Current | | 1 | -190 | -150 | mA |
| VR Pin Current | | 1 | 1 | 8 | mA |
| S21 2/ | Bit Control set at 0, 1, 3, 7, 15, & 31 | 4 | 7 | 12 | dB |
| Phase 2/3/ | Bit Control set at 1 | 4 | -17 | -7 | deg |
| | Bit Control set at 3 | 4 | -40 | -30 | |
| | Bit Control set at 7 | 4 | -85 | -70 | |
| | Bit Control set at 15 | 4 | -180 | -145 | |
| | Bit Control set at 31 | 4 | 0 | 50 | |

TABLE II Notes:
1/ Test limits apply at +25 °C only with VEE = -3.3 V and VR = 0 V
2/ Single-ended measurement with I+ = -10 dBm at 10 Gbps. Measurements shall be made at O+ and O-.
3/ Phase is a relative measurement from absolute phase with Bit Control = 0.
4/ -40 °C and +85 °C (Subgroups 2, 3, 5 and 6) are Read and Record only.

## TABLE III: BURN-IN/LIFE TEST DELTA LIMITS 1/2/3/

| Parameter | Test Conditions | Delta Limits | Units |
|---|---|---|---|
| VEE Power Supply Current | Per Table II | ± 10 | % |

TABLE III Notes:
1/ Delta test is performed at $T_A$ = +25 °C only.
2/ Table II limits will not be exceeded.
3/ Deltas calculated at post 240 hours / post 1000 hours.




| PIN # | FUNCTION | PIN # | FUNCTION | PIN # | FUNCTION | PIN # | FUNCTION |
|---|---|---|---|---|---|---|---|
| 1 | GND | 9 | B1+ | 17 | N/C | 25 | N/C |
| 2 | I+ | 10 | B1− | 18 | B4− | 26 | GND |
| 3 | I− | 11 | GND | 19 | B4+ | 27 | VEE |
| 4 | GND | 12 | B2+ | 20 | GND | 28 | VR |
| 5 | GND | 13 | B2− | 21 | GND | 29 | VB |
| 6 | BO+ | 14 | GND | 22 | O− | 30 | VEE |
| 7 | BO− | 15 | B3+ | 23 | O+ | 31 | GND |
| 8 | N/C | 16 | B3− | 24 | GND | 32 | N/C |

The HMC8693LC5 has a MSL rating of MSL3.

Figure 1 – Device Outline for the HMC8693LC5

## ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| HMC8693LC5 | –40 °C to +85 °C | 32-Lead Ceramic Leadless Chip Carrier | LCC (HE-32-1) |

## Revision History

| Revision History | | |
|---|---|---|
| **Rev** | **Description of Change** | **Date** |
| A | Initial release. | 04/16/2025 |
| | | |



ANALOG DEVICES

www.analog.com