SELECTED ITEM DRAWING

			ANALOG DEVICES	
Unless otherwise specified DIMENSIONS ARE IN INCHES (MM)	TOLERANCES: .XX +/- 0.010 .XXX +/- 0.005 .XXXX +/- 0.002 ANGLES +/- .5 DEG	Drawing practices per **ASME Y14.100**	**33 MHz to 4100 MHz, Wideband PLL + VCO**	
			SIZE **A**	DRAWING NUMBER **SID000090**

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1. SCOPE

1.1. Scope

This drawing establishes the requirements for the 33 MHz to 4100 MHz, SiGe BiCMOS, MMIC, PLL + VCO, assembled hermetically in the G32 package, to be screened in accordance with MIL-PRF-38535, Class Level S, to the requirements specified in 4.1, 4.2, and 4.3 herein.

1.2. Analog Devices Part Number

Generic Part Number	Screened Part Number
ADH835S	HMC8157G32

2. APPLICABLE DOCUMENTS

2.1. Government Documents

Unless otherwise specified, the following drawings and standards, of the issue in effect on the date of the accepted purchase order, in the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, shall form a part of this drawing to the extent specified herein.

DEPARTMENT OF DEFENSE TEST METHOD STANDARD

MIL-STD-883 Microcircuits

DEPARTMENT OF DEFENSE PERFORMANCE SPECIFICATIONS

MIL-PRF-38535 Integrated Circuits (Microcircuits) Manufacturing, General Specification For

2.2. Non-Government Documents

The following documents, of the issue in effect on the date of the purchase order, form a part of this drawing to the extent specified herein:

Analog Devices Inc.

ADI Standard Space Products Program – ASD-*Lite*.

HMC835LP6GE Data Sheet	Commercial Product Datasheet	v04.1113 (Reference Only)

3. REQUIREMENTS

3.1. General Requirements
The devices delivered shall comply to this specification.

3.2. Design Construction and Physical Dimensions
The design construction and physical dimensions shall be as defined in Figure 1 herein.

3.3. Traceability
Each delivered device shall be traceable to the wafer lot and wafer number. Inspection lot records shall be maintained to provide traceability to the specific wafer and wafer lot from which the chips originated as well as traceability to package and materials.

3.4. Burn-In and Life Test Circuit
The burn-in and life test circuit and conditions shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test methods 1005 and 1015 per MIL-STD-883.

4. QUALITY ASSURANCE PROVISIONS

4.1. Wafer Lot Acceptance Testing
The wafer lot acceptance testing shall consist of Class Level S inspections per MIL-STD-883 TM 5007.

4.2. Flight Screening Requirements
Flight screening requirements shall be per MIL-STD-883 TM 5004 for Class Level S microcircuits.

4.2.1. Electrical Test Requirements
Electrical test requirements are defined in Table I herein.

4.2.2. Electrical Performance Characteristics
Electrical performance characteristics are specified on Table II herein.

4.2.3. Burn-In Delta Requirements
Pre and Post Burn-In Electrical test and delta parameters shall consist of the tests specified in Table III herein.

4.3. Quality Conformance Inspection (QCI)
Group B and Group D tests shall be performed per MIL-STD-883 TM 5005 for Class Level S microcircuits.

4.3.1. Post Steady State Life Electrical Test
Post steady state life electrical tests shall consist of the tests specified per Table II tested at room temperature only. Devices must meet delta parameter requirements in accordance with Table III herein.

5. MIL-PRF-38535 ASD-LITE EXCEPTIONS

The manufacturing flow described in the ADI STANDARD SPACE PRODUCTS PROGRAM is to be considered a part of this specification.

5.1. Wafer Fabrication
Foundry information is available upon request.

5.2. Device Assembly
Device contains bi-metallic wire bonds (Gold bond wires on Aluminum Die pads).

5.3. Flight Screening Flow
Non-destruct Bond Pull: Not performed.
Reverse Bias Burn-In: Not applicable.

5.4. Group B
Subgroup 2: Resistance to solvents is not applicable.

5.5. Group D
Subgroup 5: Not applicable.

6. PREPARATION FOR DELIVERY

The preparation for delivery, packaging, preservation, ESD protection and handling shall be in accordance with MIL-PRF-38535.

6.1. Part Marking
Devices shall be marked as specified on Figure 1 herein.

6.2. Inspection Data Requirements
The following data shall accompany each shipment.

a. A Certificate of Conformance (C of C) certifies that the lot(s) meets all requirements of this specification.
b. Wafer Lot Acceptance data including photos from SEM Inspection defined in 4.1 herein.
c. Summary of electrical test requirements defined in 4.2 herein.
d. Summary of QCI results defined in 4.3 herein.
e. Failure Analysis with photos (If applicable).
f. A cover sheet indicating the following purchasing information:
    1. Customer purchase order number.
    2. Analog Devices part number.
    3. Part lot identification codes.
    4. Date & quantity shipped.

TABLE I: ELECTRICAL TEST REQUIREMENTS

Test Requirement	Subgroups (in accordance with MIL-PRF-38535, Table III)
Interim Electrical Parameters	1, 4,
Final Electrical Parameters	1, 4 1/2/
Group A Electrical Parameters	1, 2, 3, 4, 5, 6
Group B End-Point Electrical Parameters	1, 4 2/
Group D End-Point Electrical Parameters	1, 4

TABLE I Notes:
1/ PDA applies to Table I subgroup 1 and Table III delta parameters.
2/ See Table III for delta parameters.

TABLE II: ELECTRICAL PERFORMANCE CHARACTERISTICS (-40 °C, +25 °C AND +70 °C)

Parameter	Test Conditions 1/2/ Unless otherwise specified	Group A Subgroups	Limits		Units
			Min	Max	
3.3 V Power Consumption		1, 2, 3	30		mA
5 V Power Consumption		1, 2, 3	130		mA
Vtune		1	1.25	2.75	V
		2, 3	1	3	V
Pout @ 9 dB Gain	Frequency = 40 MHz	4	3.5	7.75	dBm
		5, 6	3	8.25	dBm
	Frequency = 2050 MHz	4	1	5	dBm
		5, 6	1	6	dBm
	Frequency = 3000 MHz	4	0.5	5.5	dBm
		5, 6	0.5	5.5	dBm
	Frequency = 4100 MHz	4	0.5	4.5	dBm
		5, 6	0	5	dBm
Pout @ 6 dB Gain	Frequency = 40 MHz	4	0.5	4.5	dBm
		5, 6	0	5	dBm
	Frequency = 2050 MHz	4	-1.5	2.5	dBm
		5, 6	-2	3	dBm
	Frequency = 3000 MHz	4	-2	2	dBm
		5, 6	-2.5	2.5	dBm
	Frequency = 4100 MHz	4	-2.5	1.5	dBm
		5, 6	-3	2	dBm
Pout @ 3 dB Gain	Frequency = 40 MHz	4	-2.5	1.5	dBm
		5, 6	-3	2	dBm
	Frequency = 2050 MHz	4	-4.5	-0.5	dBm
		5, 6	-5	0	dBm
	Frequency = 3000 MHz	4	-5	-1	dBm
		5, 6	-5.5	-0.5	dBm
	Frequency = 4100 MHz	4	-5.5	-1.5	dBm
		5, 6	-6	-1	dBm
Pout @ 0 dB Gain	Frequency = 40 MHz	4	-5.75	-1.5	dBm
		5, 6	-6.25	-1	dBm
	Frequency = 2050 MHz	4	-7.5	-3.5	dBm
		5, 6	-8	-3	dBm

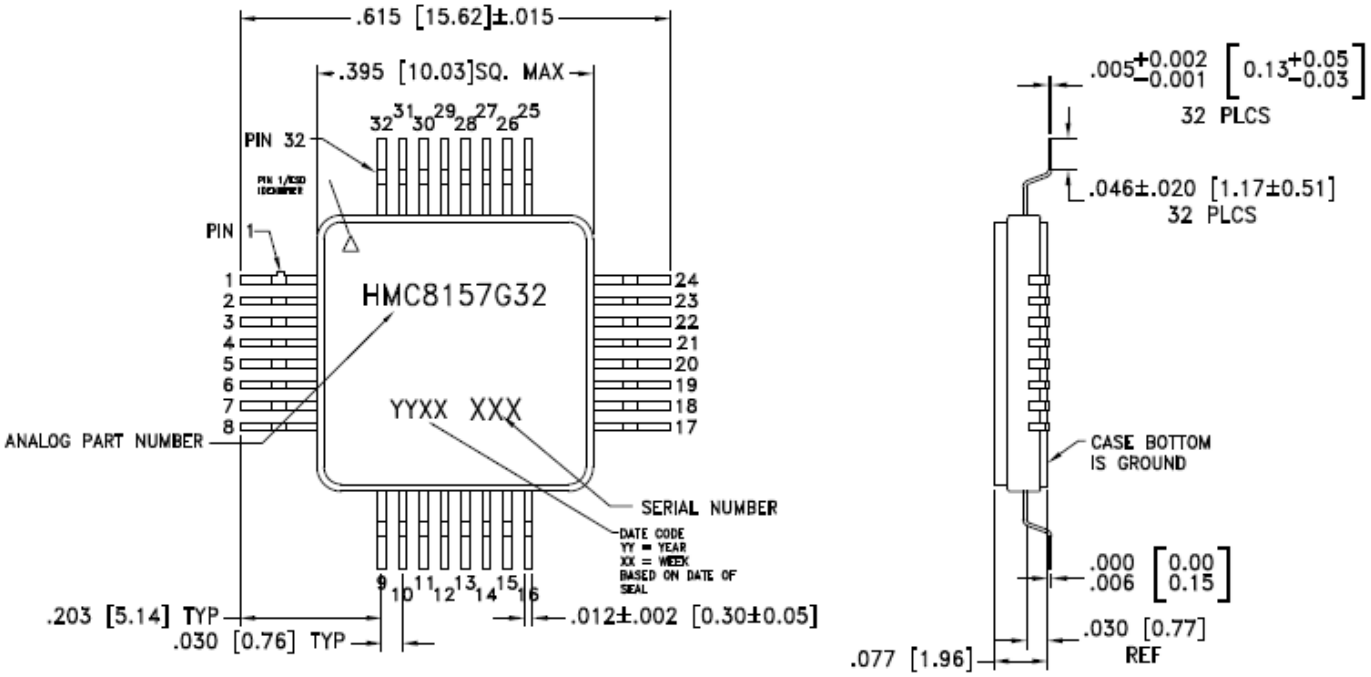
	Frequency = 3000 MHz	4	-8	-4	dBm
		5, 6	-8.5	-3.5	dBm
	Frequency = 4100 MHz	4	-8.5	-4.5	dBm
		5, 6	-9	-4	dBm
Phase Noise 3/4/	Frequency = 2050 MHz	5		-95	dBc/Hz
	Frequency = 4100 MHz	5		-85	dBc/Hz
Mute Function @ 9 dB Gain	Frequency = 2025 MHz, REG: 17h & BIT:04 = 0	5		-35	dB
		5, 6		-30	dB

TABLE II Notes:
1/ Limits apply with VPPCP = VDDLS = VCC1 = VCC2 = +5 V and RVDD = AVDD = DVDD = VCCPD = VCCHF = VCCPS = +3.3 V only.
2/ Limits apply with Ref = 10 MHz and Fcomp = 5 MHz.
3/ Measured with 250 kHz offset.
4/ Subgroup 6 is not performed.

TABLE III: BURN-IN/LIFE TEST DELTA LIMITS 1/2/3/

Parameter	Test Conditions	Delta Limits	Units
3.3 V Power Consumption	Per Table II	± 10	%
5 V Power Consumption		± 10	%
VTune		± 15	%
Pout @ 9 dB Gain	Frequency = 40 MHz	± 1	dB
	Frequency = 2050 MHz	± 1	dB
	Frequency = 3000 MHz	± 1	dB
	Frequency = 4100 MHz	± 1	dB
Pout @ 6 dB Gain	Frequency = 40 MHz	± 1	dB
	Frequency = 2050 MHz	± 1	dB
	Frequency = 3000 MHz	± 1	dB
	Frequency = 4100 MHz	± 1	dB
Pout @ 3 dB Gain	Frequency = 40 MHz	± 1	dB
	Frequency = 2050 MHz	± 1	dB
	Frequency = 3000 MHz	± 1	dB
	Frequency = 4100 MHz	± 1	dB
Pout @ 0 dB Gain	Frequency = 40 MHz	± 1	dB
	Frequency = 2050 MHz	± 1	dB
	Frequency = 3000 MHz	± 1	dB
	Frequency = 4100 MHz	± 1	dB

TABLE III Notes:
1/ Delta test is performed at T_A = +25 °C only.
2/ Table II limits will not be exceeded.
3/ Deltas calculated at pre/post 240 hours and post 240 hours / post 1000 hours.



NOTES:

1. PACKAGE MATERIAL: ALUMINA LOADED BOROSILICATE GLASS (#7052 CORNING).
2. LEADS, BASE, COVER MATERIAL: KOVAR™.
3. PLATING: ELECTROLYTIC GOLD 50 MICROINCHES MIN., OVER ELECTROLYTIC NICKEL 50 MICROINCHES MIN.
4. ALL DIMENSIONS ARE IN INCHES [MILLIMETERS].
5. TOLERANCES: ±.005 [0.13] UNLESS OTHERWISE SPECIFIED.
6. CHARACTERS TO BE LASER MARKED WITH .018"MIN to .030"MAX HEIGHT REQUIREMENTS. UTILIZE MAXIMUM CHARACTER HEIGHT BASED ON LID DIMENSIONS AND BEST FIT. LOCATE APPROX. AS SHOWN.
7. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.

PIN #	FUNCTION	PIN #	FUNCTION	PIN #	FUNCTION	PIN #	FUNCTION
1	VDDLS	9	AUX0_SDO	17	N/C	25	SDI
2	VDDCP	10	AUX1_SCK	18	CHIP_EN	26	SCK
3	BIAS	11	AUX2_SEN	19	LO1_N	27	LD_SDO
4	CP1	12	N/C	20	LO1_P	28	EXT_VCO_N
5	CP2	13	GND	21	VCC1	29	EXT_VCO_P
6	RVDD	14	LO2_P	22	VCC2	30	VCCHF
7	XREFP	15	LO2_N	23	VTUNE	31	VCCPS
8	DVDD	16	GND	24	SEN	32	VCCPD

Average Weight: 0.64 grams

Figure 1 – Device Outline for the HMC8157G32

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
HMC8157G32	−40 °C to +70 °C	32-Lead Glass/Metal Hermetic SMT	G32 (FR-32-1)

Revision History

Revision History		
Rev	**Description of Change**	**Date**
A	Initial Release	04/16/2025
B	Updated Figure 1	09/17/2025