SELECTED ITEM DRAWING

			ANALOG DEVICES	
Unless otherwise specified DIMENSIONS ARE IN INCHES (MM)	TOLERANCES: .XX +/- 0.010 .XXX +/- 0.005 .XXXX +/- 0.002 ANGLES +/- .5 DEG	Drawing practices per **ASME Y14.100**	**DC to 8 GHz, Low Noise 1:9 Fanout Buffer**	
			SIZE **A**	DRAWING NUMBER **SID000084**

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1. SCOPE

1.1. Scope

This drawing establishes the requirements for the non-hermetic, DC to 8 GHz, SiGe BiCMOS, Low Noise 1:9 Fanout Buffer, to be screened with guidelines to NASA/EEE-INST-002, Section M4, Table 2 and Table 3, Level 1 applications, to the requirements specified in 4.1, and 4.2 herein.

1.2. Analog Devices Part Number

Generic Part Number	Screened Part Number
ADH987S	HMC8626LP5E

2. APPLICABLE DOCUMENTS

2.1. Government Documents

Unless otherwise specified, the following drawings and standards, of the issue in effect on the date of the accepted purchase order, in the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, shall form a part of this drawing to the extent specified herein.

DEPARTMENT OF DEFENSE TEST METHOD STANDARD

MIL-STD-883	Microcircuits
MIL-STD-1580C	Destructive Physical Analysis for Electronic, Electromagnetic, and Electromechanical Parts

DEPARTMENT OF DEFENSE PERFORMANCE SPECIFICATIONS

MIL-PRF-38535	Integrated Circuits (Microcircuits) Manufacturing, General Specification For
PEM-INST-001	Instructions for Plastic Encapsulated Microcircuit (PEM) Selection, Screening, and Qualification
NASA/EEE-INST-002	Instructions for EEE Parts Selection, Screening, Qualification and Derating

2.2. Non-Government Documents

The following documents, of the issue in effect on the date of the purchase order, form a part of this drawing to the extent specified herein:

Analog Devices Inc.

HMC987LP5E Data Sheet	Commercial Product Datasheet	v03.1112 (Reference Only)

3. REQUIREMENTS

3.1. General Requirements
The devices delivered shall comply to this specification.

3.2. Design Construction and Physical Dimensions
The design construction and physical dimensions shall be as defined in Figure 1 herein.

3.3. Traceability
Each delivered device shall be traceable to a production lot. Inspection lot records shall be maintained to provide traceability of its origin.

3.4. DPA
If specified on Purchase Order, DPA testing shall be done in accordance with MIL-STD-1580C, Sections 16.1.

3.5. Solder Dipping
If specified on Purchase Order, Solder dipping of terminals is required. The terminal finish of the devices is 100% Matte Sn and shall be hot solder dipped with Sn63 in accordance with MIL-PRF-38535.

3.6. Burn-In and Life Test Circuit
The burn-in and life test circuit and conditions shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test methods 1005 and 1015 per MIL-STD-883.

4. QUALITY ASSURANCE PROVISIONS

4.1. Flight Screening Requirements
Flight screening requirements for PEM devices shall be per EEE-INST-002, Section M4, Table 2, Level 1 applications. Where applicable, electrical testing shall consist of tests specified in Table I herein.

4.1.1. Initial (Pre Burn-In) Electrical Test
Initial electrical test shall consist of the tests specified on Table I tested at room temperature only.

4.1.2. Post Burn-In Electrical Test
Post Burn-In electrical test shall consist of the tests specified on Table I, tested at room temperature only. Devices must meet PDA requirements of ≤ 5%.

4.1.3. Final Electrical Test (Temperature Extremes)
The final electrical test shall consist of tests specified in Table I, tested at -40 °C and +85 °C, which shall be Read and Record only.

4.2. Qualification Requirements for PEMS
Qualification requirements for PEMS devices shall be per EEE-INST-002, Section M4, Table 3, Level 1 applications. Where applicable, electrical testing shall consist of tests specified in Table I herein.

4.2.1. Post Steady State Life Electrical Test
Post steady state life electrical tests shall consist of the tests specified per Table I tested at +25 °C, -40 °C, and +85 °C. -40 °C, and +85 °C shall be Read and Record only.

5. EEE-INST-002 SECTION M4 EXCEPTIONS

5.1. Flight Screening Requirements
Serialization: Not performed.

5.2. Qualification Requirements for PEMS
Radiation Analysis: SEE has not been evaluated.
Subgroup 2: Unbiased HAST performed as Level 1 applications.

6. PREPARATION FOR DELIVERY

The preparation for delivery, packaging, preservation, ESD protection and handling shall be in accordance with MIL-PRF-38535.

6.1. Part Marking
Devices shall be marked as specified on Figure 1 herein.

6.2. Inspection Data Requirements
The following data shall accompany each shipment.

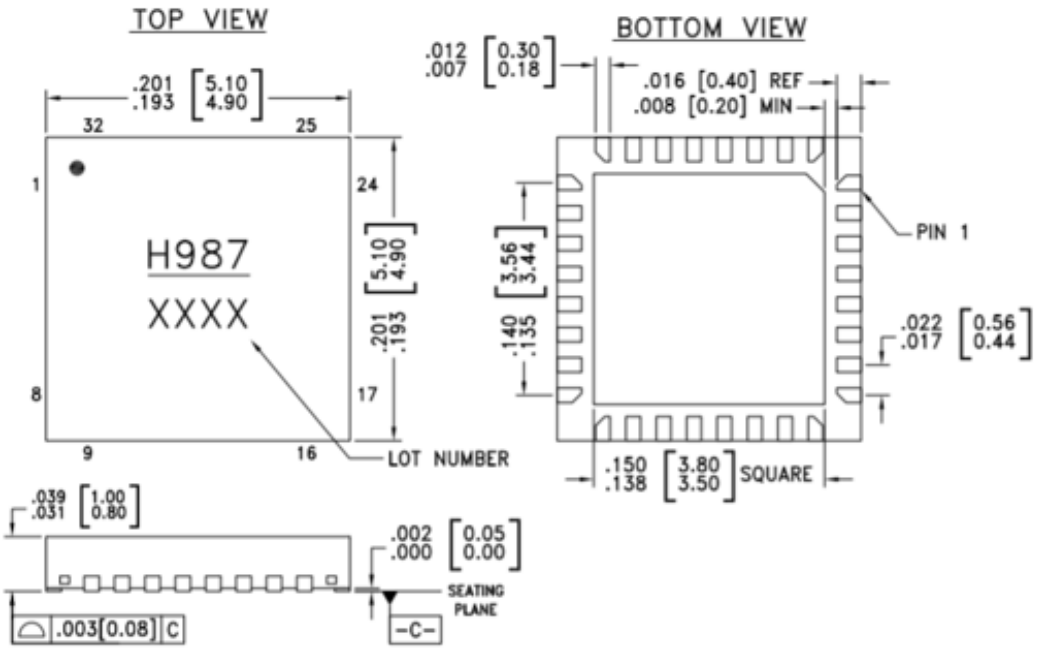
a. A Certificate of Conformance (C of C) certifies that the lot(s) meets all requirements of this specification.
b. DPA Report (if applicable)
c. Summary of electrical test requirements defined in 4.1 herein.
d. Summary of qualification requirements for PEMS results defined in 4.2 herein.
e. Failure Analysis with photos (If applicable)
f. A cover sheet indicating the following purchasing information:
    1. Customer purchase order number.
    2. Analog Devices part number.
    3. Part lot identification codes.
    4. Date & quantity shipped.

TABLE I: ELECTRICAL PERFORMANCE CHARACTERISTICS (-40 °C, +25 °C AND +85 °C)

Parameter	Test Conditions 1/2/ Unless otherwise specified	Group A Subgroups	Limits		Units
			Min	Max	
Stand-By Current	Chip Disabled	1		1.17	µA
Total Supply Current	RFIN = 700MHz RF Buffer EN	4	180	205	mA
	RFIN = 700MHz RF Buffer EN PMODE_SEL = 1	4	100	122	mA
	RFIN = 700MHz RF Buffer EN PMODE_SEL = 0	4	173	211	mA
OUT1N Buffer P_{OUT}	CLK_P = 500MHz CLK_P P_{IN} = -30dBm PMODE_SEL = 0 Reg02h = 255 Reg03h = 10 Reg04h = 7	4	-17.25	-14.25	dBm
OUT2P Buffer P_{OUT}		4	-17.25	-14.25	dBm
OUT3P Buffer P_{OUT}		4	-16.75	-13.75	dBm
OUT4P Buffer P_{OUT}		4	-16.75	-13.75	dBm
OUT5P Buffer P_{OUT}		4	-16.75	-13.75	dBm
OUT6P Buffer P_{OUT}		4	-17.25	-14.25	dBm
OUT7P Buffer P_{OUT}		4	-14.25	-11.11	dBm
OUT8P Buffer P_{OUT}		4	-14.0	-10.0	dBm
OUT1N Buffer P_{OUT}	CLK_P = 500MHz CLK_P PIN = +4dBm PMODE_SEL = 0 Reg02h = 255 Reg03h = 10 Reg04h = 7	4	-9.05	-7.05	dBm
OUT2P Buffer P_{OUT}		4	-9.05	-7.05	dBm
OUT3P Buffer P_{OUT}		4	-9.05	-7.05	dBm
OUT4P Buffer P_{OUT}		4	-9.05	-7.05	dBm
OUT5P Buffer P_{OUT}		4	-9.05	-7.05	dBm
OUT6P Buffer P_{OUT}		4	-9.05	-7.05	dBm
OUT7P Buffer P_{OUT}		4	-6.95	-4.95	dBm
OUT8P Buffer P_{OUT}		4	-6.95	-4.95	dBm
OUT1P Buffer P_{OUT}	CLK_P = 1000MHz CLK_P PIN = +4dBm PMODE_SEL = 0 Reg02h = 255 Reg03h = 10 Reg04h = 7	4	-9.55	-7.55	dBm
OUT2N Buffer P_{OUT}		4	-8.95	-6.95	dBm
OUT3N Buffer P_{OUT}		4	-9.95	-7.95	dBm
OUT4N Buffer P_{OUT}		4	-9.45	-7.45	dBm
OUT5N Buffer P_{OUT}		4	-10.15	-8.15	dBm
OUT6N Buffer P_{OUT}		4	-9.95	-7.95	dBm
OUT7N Buffer P_{OUT}		4	-18.75	-16.25	dBm
OUT8N Buffer P_{OUT}		4	-19.05	-16.55	dBm
RFOUTP P_{OUT}	CLK_P = 100MHz, CLK_P PIN = -30dBm, PMODE_SEL = 0, Reg02h =0, Reg03h = 10, Reg04h = 0	4	-15.5	-12.5	dBm
	CLK_P = 100MHz, CLK_P PIN = -30dBm, PMODE_SEL = 0, Reg02h = 0, Reg03h = 10, Reg04h = 1	4	-2.9	-0.9	dBm
	CLK_P = 100MHz, CLK_P P_{IN} = -30dBm, PMODE_SEL = 0, Reg02h = 0, Reg03h = 10, Reg04h = 2	4	-3.2	-1.2	dBm

	CLK_P = 100MHz, CLK_P P_{IN} = -30dBm, PMODE_SEL = 0, Reg02h = 0, Reg03h = 10, Reg04h = 3	4	-3.2	-1.2	dBm
	CLK_P = 100MHz, CLK_P P_{IN} = -30dBm, PMODE_SEL = 0, Reg02h = 0, Reg03h = 10, Reg04h = 4	4	-3.9	-1.9	dBm
	CLK_N = 100MHz, CLK_N P_{IN} = -30dBm, PMODE_SEL = 0, Reg02h =0, Reg03h = 10, Reg04h = 0	4	-15.5	-12.5	dBm
	CLK_P = 100MHz, CLK_P P_{IN} = +4dBm, PMODE_SEL = 0, Reg02h =0, Reg03h = 10, Reg04h = 0	4	-4.1	-2.1	dBm
	CLK_P = 100MHz, CLK_P P_{IN} = +4dBm, PMODE_SEL = 0, Reg02h = 0, Reg03h = 10, Reg04h = 1	4	-3.6	-1.6	dBm
	CLK_P = 100MHz, CLK_P P_{IN} = +4dBm, PMODE_SEL = 0, Reg02h = 0, Reg03h = 10, Reg04h = 2	4	-3.8	-1.8	dBm
	CLK_P = 100MHz, CLK_P P_{IN} = +4dBm, PMODE_SEL = 0, Reg02h = 0, Reg03h = 10, Reg04h = 3	4	-3.7	-1.7	dBm
	CLK_P = 100MHz, CLK_P P_{IN} = +4dBm, PMODE_SEL = 0, Reg02h = 0, Reg03h = 10, Reg04h = 4	4	-4.3	-2.3	dBm
	CLK_N = 100MHz, CLK_N P_{IN} = +4dBm, PMODE_SEL = 0, Reg02h = 0, Reg03h = 10, Reg04h = 0	4	-4.0	-2.0	dBm

TABLE I Notes:
1/ Test limits apply at +25 °C only with Regulated VDD (VCCHF = VCCA = VCCB = VCCRF) = 3.3 V.
2/ -40 °C and +85 °C (Subgroups 2, 3, 5, and 6) are Read and Record only.



NOTES:

1. PACKAGE BODY MATERIAL: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
2. LEAD AND GROUND PADDLE MATERIAL: COPPER ALLOY.
3. LEAD AND GROUND PADDLE PLATING: 100% MATTE TIN.
4. DIMENSIONS ARE IN INCHES [MILLIMETERS].
5. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
6. CHARACTERS TO BE HELVETICA MEDIUM, .025 HIGH, WHITE INK, OR LASER MARK LOCATED APPROX. AS SHOWN.
7. PAD BURR LENGTH SHALL BE 0.15mm MAX. PAD BURR HEIGHT SHALL BE 0.25mm MAX.
8. PACKAGE WARP SHALL NOT EXCEED 0.05mm
9. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.

PIN #	FUNCTION	PIN #	FUNCTION	PIN #	FUNCTION	PIN #	FUNCTION
1	VCCHF	9	VCCRF	17	OUTN6	25	VCCA
2	CLKP	10	SCLK	18	OUTP6	26	OUTN2
3	CLKN	11	SEN	19	OUTN5	27	OUTP2
4	SDI	12	OUTP8	20	OUTP5	28	OUTN1
5	SDO	13	OUTN8	21	OUTP4	29	OUTP1
6	PMODE-SEL	14	OUTP7	22	OUTN4	30	RFBUFEN
7	RFOUTP	15	OUTN7	23	OUTP3	31	CEN
8	RFOUTN	16	VCCB	24	OUTN3	32	N/C

The HMC8626LP5E has a MSL rating of MSL3.

Figure 1 – Device Outline for the HMC8626LP5E

ORDERING GUIDE

Model	Temperature Range	Package Description	Lead Finish	Package Option
HMC8626LP5E	–40 °C to +85 °C	32-Lead RoHS-Compliant Low Stress Injection Molded Plastic	100% Matte Sn	LFCSP (CP-32-35)

Revision History

Revision History		
Rev	**Description of Change**	**Date**
A	Initial release.	03/03/2025
B	Revise Section 2.2, 3.5, 4.1.2, and Figure 1, Add Section 5.1, and Remove Table II.	04/16/2025

ANALOG DEVICES

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