SELECTED ITEM DRAWING

			ANALOG DEVICES	
Unless otherwise specified DIMENSIONS ARE IN INCHES (MM)	TOLERANCES: .XX +/- 0.010 .XXX +/- 0.005 .XXXX +/- 0.002 ANGLES +/- .5 DEG	Drawing practices per **ASME Y14.100**	**12.5 GHz to 13.9 GHz, VCO with Divide-By-4 Frequency Output**	
			SIZE **A**	DRAWING NUMBER **SID000078**

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1. SCOPE

1.1. Scope

This drawing establishes the requirements for the 12.5 GHz to 13.9 GHz, GaAs, InGaP, HBT, MMIC, VCO with Divide-By-4 Frequency Output, assembled hermetically in the LSH7 package, to be screened in accordance with MIL-PRF-38535, Class Level S, to the requirements specified in 4.1, 4.2, and 4.3 herein.

1.2. Analog Devices Part Number

Generic Part Number	Screened Part Number
ADH584S	HMC8173LSH7

2. APPLICABLE DOCUMENTS

2.1. Government Documents

Unless otherwise specified, the following drawings and standards, of the issue in effect on the date of the accepted purchase order, in the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, shall form a part of this drawing to the extent specified herein.

DEPARTMENT OF DEFENSE TEST METHOD STANDARD

MIL-STD-883 Microcircuits

DEPARTMENT OF DEFENSE PERFORMANCE SPECIFICATIONS

MIL-PRF-38535 Integrated Circuits (Microcircuits) Manufacturing, General Specification For

2.2. Non-Government Documents

The following documents, of the issue in effect on the date of the purchase order, form a part of this drawing to the extent specified herein:

Analog Devices Inc.

ADI Standard Space Products Program – ASD-*Lite*.

HMC584LP5 / 584LP5E Data Sheet Commercial Product Datasheet v03.1210 (Reference Only)

3. REQUIREMENTS

3.1. General Requirements
The devices delivered shall comply to this specification.

3.2. Design Construction and Physical Dimensions
The design construction and physical dimensions shall be as defined in Figure 1 herein.

3.3. Traceability
Each delivered device shall be traceable to the wafer lot and wafer number. Inspection lot records shall be maintained to provide traceability to the specific wafer and wafer lot from which the chips originated as well as traceability to package and materials.

3.4. Burn-In and Life Test Circuit
The burn-in and life test circuit and conditions shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test methods 1005 and 1015 per MIL-STD-883.

4. QUALITY ASSURANCE PROVISIONS

4.1. Wafer Lot Acceptance Testing
The wafer lot acceptance testing shall consist of Class Level S inspections per MIL-STD-883 TM 5007.

4.2. Flight Screening Requirements
Flight screening requirements shall be per MIL-STD-883 TM 5004 for Class level S microcircuits.

4.2.1. Electrical Test Requirements
Electrical test requirements are defined in Table I herein.

4.2.2. Electrical Performance Characteristics
Electrical performance characteristics are specified on Table II herein.

4.2.3. Burn-In Delta Requirements
Pre and Post Burn-In Electrical test and delta parameters shall consist of the tests specified in Table III herein.

4.3. Quality Conformance Inspection (QCI)
Group B and Group D tests shall be performed per MIL-STD-883 TM 5005 for Class level S microcircuits.

4.3.1. Post Steady State Lie Electrical Test
Post steady state life electrical tests shall consist of the tests specified per Table II tested at room temperature only. Devices must meet delta parameter requirements in accordance with Table III herein.

5. MIL-PRF-38535 ASD-LITE EXCEPTIONS

The manufacturing flow described in the ADI STANDARD SPACE PRODUCTS PROGRAM is to be considered a part of this specification.

5.1. Wafer Fabrication

Foundry information is available upon request.

5.2. Flight Screening Flow

Non-Destruct Bond Pull: Not performed.
Reverse Bias Burn-In: Not applicable.

5.3. Group B

Subgroup 2: Resistance to solvents is not applicable.

5.4. Group D

Subgroup 5: Not applicable.
Subgroup 7: Not applicable.
Subgroup 8: Not applicable.
Subgroup 9: Not applicable.

6. PREPARATION FOR DELIVERY

The preparation for delivery, packaging, preservation, ESD protection and handling shall be in accordance with MIL-PRF-38535.

6.1. Part Marking

Devices shall be marked as specified on Figure 1 herein.

6.2. Inspection Data Requirements

The following data shall accompany each shipment.

a. A Certificate of Conformance (C of C) certifies that the lot(s) meets all requirements of this specification.
b. Wafer Lot Acceptance data including photos from SEM Inspection defined in 4.1 herein.
c. Summary of electrical test requirements defined in 4.2 herein.
d. Summary of QCI results defined in 4.3 herein.
e. Failure Analysis with photos (If applicable)
f. A cover sheet indicating the following purchasing information:
    1. Customer purchase order number.
    2. Analog Devices part number.
    3. Part lot identification codes.
    4. Date & quantity shipped.

TABLE I: ELECTRICAL TEST REQUIREMENTS

Test Requirement	Subgroups (in accordance with MIL-PRF-38535, Table III)
Interim Electrical Parameters	1, 4
Final Electrical Parameters	1, 4 1/2/
Group A Electrical Parameters	1, 2, 3, 4, 5, 6
Group B End-Point Electrical Parameters	1, 4 2/
Group D End-Point Electrical Parameters	1, 4

TABLE I Notes:
1/ PDA applies to Table I subgroup 1 and Table III delta parameters.
2/ See Table III for delta parameters

TABLE II: ELECTRICAL PERFORMANCE CHARACTERISTICS (-40 °C, +25 °C AND +65 °C)

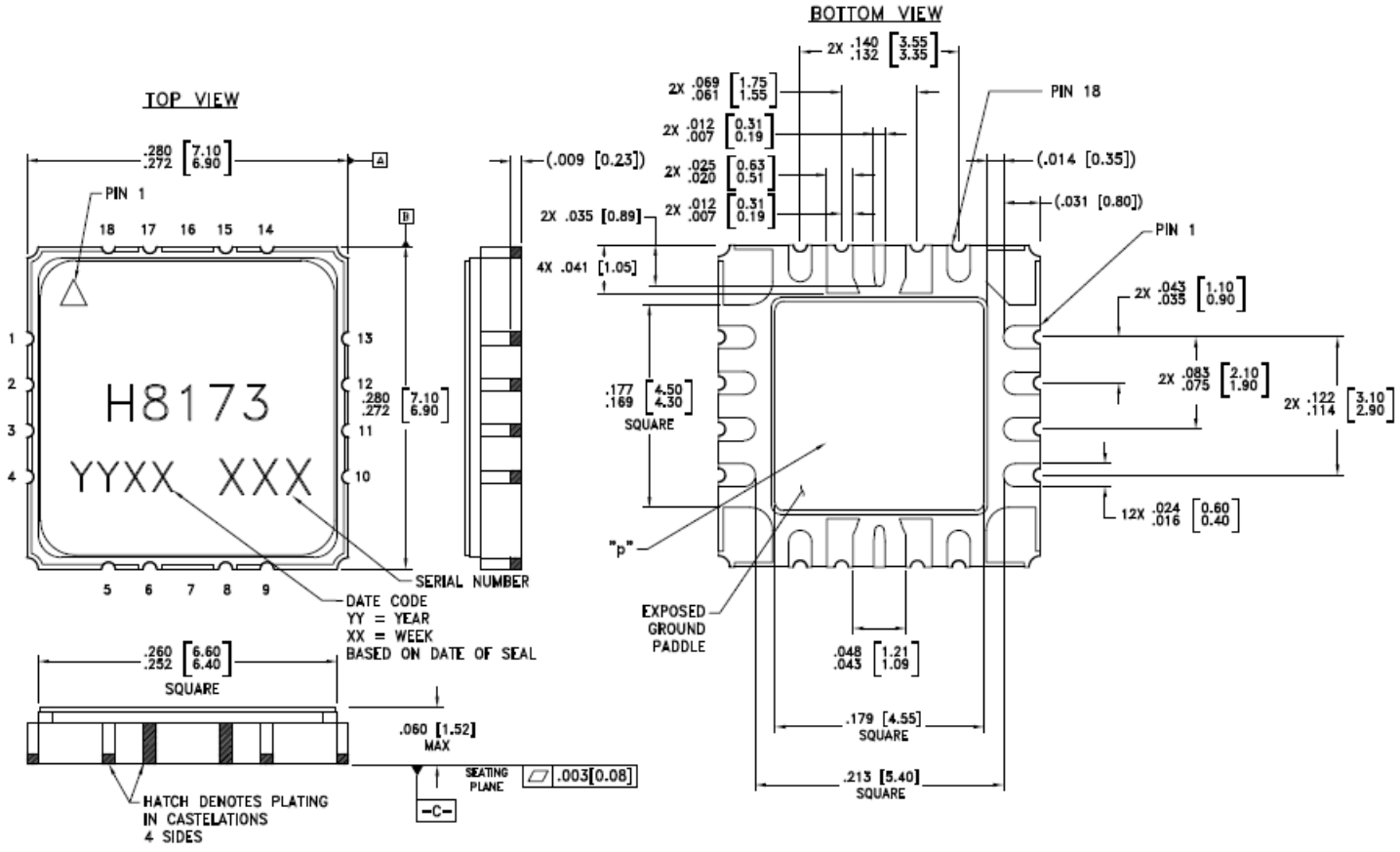
Parameter	Test Conditions 1/2/ Unless otherwise specified	Group A Subgroups	Limits			Units
			Min	Typ	Max	
Frequency Range Fo	Vtune = 2 V	4			12.5	GHz
	Vtune = 12 V	4	13.9			GHz
Frequency Range Fo/4	Vtune = 2 V	4			3.125	GHz
	Vtune = 12 V	4	3.475			GHz
Vtune		1	2		12	V
Turn Port Leakage Current	Vtune = 12 V	1			10	µA
Output Power RFOUT	Vtune = 2 V and Vtune = 12 V	4	7		14	dBm
Output Power RFOUT/4 3/	Vtune = 2 V and Vtune = 12 V	4	-9		-3	dBm
Supply Current	Vtune = 2 V and Vtune = 12 V	1			350	mA
SSB Phase Noise @ 100 kHz Offset 4/	Vtune = 2 V	4		-106		dBc/Hz
	Vtune = 2 V	5		-105	-100	dBc/Hz
	Vtune = 12V	4		-110		dBc/Hz
	Vtune = 12 V	5		-109	-100	dBc/Hz

TABLE II Notes:
1/ Test limits apply at +25 °C with Vcc (Dig) = Vcc (RF) = +5 V unless otherwise noted.
2/ -40 °C and +65 °C (subgroups 2, 3, 5, and 6) shall be Read and Record only unless otherwise noted.
3/ DC block required.
4/ Subgroup 6 is not performed. Subgroup 4 is for reference purposes only.

TABLE III: BURN-IN/LIFE TEST DELTA LIMITS 1/2/3/

Parameter	Test Conditions	Delta Limits	Units
Output Power RFOUT	Per Table II	± 1.2	dB
Output Power RFOUT/4		± 1.2	dB
Supply Current		± 10	%

TABLE III Notes:
1/ Delta test is performed at T_A = +25 °C only.
2/ Table II limits will not be exceeded.
3/ Deltas calculated at pre/post 240 hours and post 240 hour / post1000 hours.



NOTES:

1. PACKAGE BODY MATERIAL: ALUMINA, WHITE
2. FINISH: ELECTROLESS Au PLATING 40–100 uIN THK. OVER ELECTROLESS NICKEL PLATING 100 TO 250 uIN THK. PLATING THICKNESS MEASURED ON POINT "P".
3. DIMENSIONS ARE IN INCHES [MILLIMETERS].
4. LEAD SPACING TOLERANCE IS NON-CUMULATIVE, DIMENSIONS LOCATED ABOUT [-A-] AND [-B-] WITHIN .005".
5. CHARACTERS TO BE LASER MARKED WITH .018" MIN TO .030" MAX HEIGHT REQUIREMENTS. UTILIZE MAXIMUM CHARACTER HEIGHT BASED ON LID DIMENSIONS AND BEST FIT. LOCATE APPROX. AS SHOWN.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

PIN #	FUNCTION	PIN #	FUNCTION	PIN #	FUNCTION
1	GND	7	RFOUT/4	13	GND
2	GND	8	GND	14	GND
3	Vtune	9	Vcc (Dig)	15	GND
4	GND	10	GND	16	RFOUT
5	GND	11	GND	17	GND
6	GND	12	GND	18	Vcc (RF)

Figure 1 – Device Outline for the HMC8173LSH7

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
HMC8173LSH7	–40 °C to +65 °C	18-Lead Ceramic Hermetic Leadless Chip Carrier	LSH7 (EH-18-2)

Revision History

Revision History		
Rev	**Description of Change**	**Date**
A	Initial release.	01/28/2025

ANALOG DEVICES

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