


SELECTED ITEM DRAWING

				
Unless otherwise specified DIMENSIONS ARE IN INCHES (MM)	TOLERANCES: .XX +/- 0.010 .XXX +/- 0.005 .XXXX +/- 0.002 ANGLES +/- .5 DEG	Drawing practices per ASME Y14.100	10 MHz to 1300 MHz, Digital Phase – Frequency Detector	
			SIZE A	DRAWING NUMBER SID000076

SID000076

Rev. B

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1. SCOPE

1.1. Scope

This drawing establishes the requirements for the 10 MHz to 1300 MHz, HBT, Digital Phase – Frequency Detector, assembled hermetically in the G16 package, to be screened in accordance with MIL-PRF-38535, Class Level S, to the requirements specified in 4.1, 4.2, and 4.3 herein.

1.2. Analog Devices Part Number

Generic Part Number

ADH439S

Screened Part Number

HMC4219G16

2. APPLICABLE DOCUMENTS

2.1. Government Documents

Unless otherwise specified, the following drawings and standards, of the issue in effect on the date of the accepted purchase order, in the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, shall form a part of this drawing to the extent specified herein.

DEPARTMENT OF DEFENSE TEST METHOD STANDARD

MIL-STD-883

Microcircuits

DEPARTMENT OF DEFENSE PERFORMANCE SPECIFICATIONS

MIL-PRF-38535

Integrated Circuits (Microcircuits) Manufacturing, General Specification For

2.2. Non-Government Documents

The following documents, of the issue in effect on the date of the purchase order, form a part of this drawing to the extent specified herein:

Analog Devices Inc.

[ADI Standard Space Products Program](#) – ASD-*Lite*.

HMC439QS16G / 439QS16GE Data Sheet

Commercial Product Datasheet

v02.0705 (Reference Only)

3. REQUIREMENTS

3.1. General Requirements

The devices delivered shall comply to this specification.

3.2. Design Construction and Physical Dimensions

The design construction and physical dimensions shall be as defined in Figure 1 herein.

3.3. Traceability

Each delivered device shall be traceable to the wafer lot and wafer number. Inspection lot records shall be maintained to provide traceability to the specific wafer and wafer lot from which the chips originated as well as traceability to package and materials.

3.4. Burn-In and Life Test Circuit

The burn-in and life test circuit and conditions shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test methods 1005 and 1015 per MIL-STD-883.

4. QUALITY ASSURANCE PROVISIONS

4.1. Wafer Lot Acceptance Testing

The wafer lot acceptance testing shall consist of Class Level S inspections per MIL-STD-883 TM 5007.

4.2. Flight Screening Requirements

Flight screening requirements shall be per MIL-STD-883 TM 5004 for Class level S microcircuits.

4.2.1. Electrical Test Requirements

Electrical test requirements are defined in Table I herein.

4.2.2. Electrical Performance Characteristics

Electrical performance characteristics are specified on Table II herein.

4.2.3. Burn-In Delta Requirements

Pre and Post Burn-In Electrical test and delta parameters shall consist of the tests specified in Table III herein.

4.3. Quality Conformance Inspection (QCI)

Group B and Group D tests shall be performed per MIL-STD-883 TM 5005 for Class level S microcircuits.

4.3.1. Post Steady State Life Electrical Test

Post steady state life electrical tests shall consist of the tests specified per Table II tested at room temperature only. Devices must meet delta parameter requirements in accordance with Table III herein.

5. MIL-PRF-38535 ASD-LITE EXCEPTIONS

The manufacturing flow described in the ADI STANDARD SPACE PRODUCTS PROGRAM is to be considered a part of this specification.

5.1. Wafer Fabrication

Foundry information is available upon request.

5.2. Flight Screening Flow

Non-Destruct Bond Pull: Not performed.

Reverse Bias Burn-In: Not applicable.

5.3. Group B

Subgroup 2: Resistance to solvents is not applicable.

5.4. Group D

Subgroup 5: Not applicable.

Subgroup 7: Not applicable.

Subgroup 8: Not applicable.

Subgroup 9: Not applicable.

6. PREPARATION FOR DELIVERY

The preparation for delivery, packaging, preservation, ESD protection and handling shall be in accordance with MIL-PRF-38535.

6.1. Part Marking

Devices shall be marked as specified on Figure 1 herein.

6.2. Inspection Data Requirements

The following data shall accompany each shipment.

- a. A Certificate of Conformance (C of C) certifies that the lot(s) meets all requirements of this specification.
- b. Wafer Lot Acceptance data including photos from SEM Inspection defined in 4.1 herein.
- c. Summary of electrical test requirements defined in 4.2 herein.
- d. Summary of QCI results defined in 4.3 herein.
- e. Failure Analysis with photos (If applicable).
- f. A cover sheet indicating the following purchasing information:
 1. Customer purchase order number.
 2. Analog Devices part number.
 3. Part lot identification codes.
 4. Date & quantity shipped.

TABLE I: ELECTRICAL TEST REQUIREMENTS

Test Requirement	Subgroups (in accordance with MIL-PRF-38535, Table III)
Interim Electrical Parameters	1, 4
Final Electrical Parameters	1, 4 <u>1/2/</u>
Group A Electrical Parameters	1, 2, 3, 4, 5, 6
Group B End-Point Electrical Parameters	1, 4 <u>2/</u>
Group D End-Point Electrical Parameters	1, 4

TABLE I Notes:

1/ PDA applies to Table I subgroup 1 and Table III delta parameters.

2/ See Table III for delta parameters.

TABLE II: ELECTRICAL PERFORMANCE CHARACTERISTICS (-40 °C, +25 °C AND +85 °C)

Parameter	Test Conditions <u>1/2/</u> Unless otherwise specified	Group A Subgroups	Limits		Units
			Min	Max	
NU Output Voltage	F _{REF} = 144 MHz, P _{REF} = +5 dBm F _{VCO} = 143 MHz, P _{VCO} = -5 dBm	4, 5, 6	1.9	2.2	V _{PK-PK}
	F _{REF} = 143 MHz, P _{REF} = +5 dBm F _{VCO} = 144 MHz, P _{VCO} = -5 dBm	4, 5, 6	4.9	5.1	Vdc
ND Output Voltage	F _{REF} = 144 MHz, P _{REF} = +5 dBm F _{VCO} = 143 MHz, P _{VCO} = -5 dBm	4, 5, 6	4.9	5.1	Vdc
	F _{REF} = 143 MHz, P _{REF} = +5 dBm F _{VCO} = 144 MHz, P _{VCO} = -5 dBm	4, 5, 6	1.9	2.2	V _{PK-PK}
Phase Noise	F _{IN} = 143 MHz, P _{IN} = +5 dBm & 100 kHz Offset	4, 5, 6		-145	dBc/Hz
Supply Current	No RF Signal at FIN	1, 2, 3	75	100	mA

TABLE II Notes:

1/ Test limits apply between -40 °C and +85 °C with Vcc = +5 V.

2/ 200 Ohm pull-up to Vcc.

TABLE III: BURN-IN/LIFE TEST DELTA LIMITS 1/2/3/

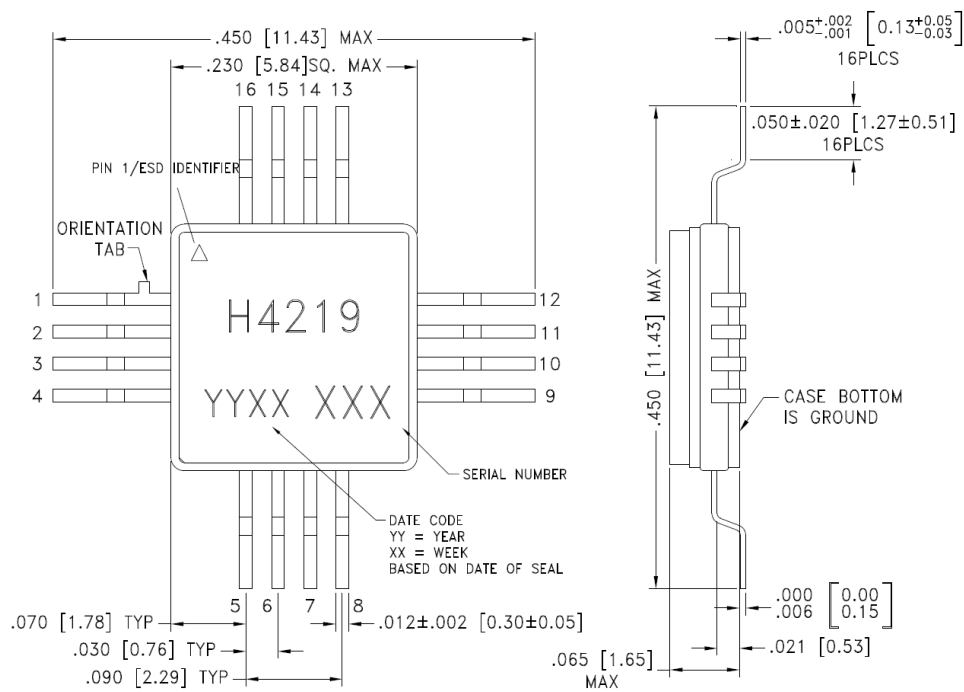
Parameter	Test Conditions	Delta Limits	Units
Supply Current	Per Table II	± 10	%

TABLE III Notes:

1/ Delta test is performed at T_A = +25 °C only.

2/ Table II limits will not be exceeded.

3/ Deltas calculated at pre/post 240 hours and post 240 hours / post 1000 hours.



NOTES:

1. PACKAGE MATERIAL: ALUMINA LOADED BOROSILICATE GLASS.
2. LEADS, BASE, COVER MATERIAL: KOVAR™ (#7052 CORNING).
3. PLATING: ELECTROLYTIC GOLD 50 MICROINCHES MIN., OVER ELECTROLYTIC NICKEL 50 MICROINCHES MIN.
4. ALL DIMENSIONS ARE IN INCHES [MILLIMETERS].
5. TOLERANCES: ± 0.005 [0.13] UNLESS OTHERWISE SPECIFIED.
6. CHARACTERS TO BE LASER MARKED WITH .018"MIN to .030"MAX HEIGHT REQUIREMENTS. UTILIZE MAXIMUM CHARACTER HEIGHT BASED ON LID DIMENSIONS AND BEST FIT. LOCATE APPROX. AS SHOWN.
7. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.

PIN #	FUNCTION	PIN #	FUNCTION
1	REF	9	GND
2	NREF	10	ND
3	VCO	11	D
4	GND	12	NU
5	NVCO	13	U
6	GND	14	GND
7	GND	15	VCC
8	Vcc3V	16	GND

Average Weight: 0.19 grams

Figure 1 – Device Outline for the HMC4219G16

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
HMC4219G16	−40 °C to +85 °C	16-Lead Glass/Metal Hermetic SMT	G16 (FR-16-2)

Revision History

Revision History		
Rev	Description of Change	Date
A	Initial release.	01/28/2025
B	Updated Section 4.3.1 and Figure 1	09/11/2025