		SELECTE	ED ITEM DRAWING
Unless otherwise specified DIMENSIONS ARE IN INCHES (MM)	TOLERANCES: .XX +/- 0.010 .XXX +/- 0.005 .XXXX +/- 0.002 ANGLES+/5 DEG	Drawing practices per ASME Y14.100	ANALOG DEVICES 18 GHz to 29 GHz Output, x2 Active Frequency Multiplier SIZE DRAWING NUMBER A SID000060

SID000060 Rev. A Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective companies.

1. SCOPE

1.1. <u>Scope</u>

This drawing establishes the requirements for the 18 GHz to 29 GHz Output, GaAs, PHEMT, MMIC, x2 Active Frequency Multiplier, to be screened in accordance with MIL-PRF-38534, Class K, to the requirements specified in 4.1, and 4.2 herein.

1.2. Analog Devices Part Number

Generic Part Number Screened Part Number

ADH576S HMC8332

2. APPLICABLE DOCUMENTS

2.1. Government Documents

Unless otherwise specified, the following drawings and standards, of the issue in effect on the date of the accepted purchase order, in the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, shall form a part of this drawing to the extent specified herein.

DEPARTMENT OF DEFENSE TEST METHOD STANDARD

MIL-STD-883 Microcircuits

DEPARTMENT OF DEFENSE PERFORMANCE SPECIFICATIONS

MIL-PRF-38534 Hybrid Microcircuits, General Specifications For

2.2. Non-Government Documents

The following documents, of the issue in effect on the date of the purchase order, form a part of this drawing to the extent specified herein:

Analog Devices Inc.

HMC576-Die Data Sheet Commercial Product Die Datasheet v00.0506 (Reference Only)

3. REQUIREMENTS

3.1. General Requirements

The devices delivered shall comply to this specification.

3.2. <u>Design Construction and Physical Dimensions</u>

The design construction and physical dimensions shall be as defined in Figure 1 herein.

3.3. <u>Traceability</u>

Each delivered device shall be traceable to the wafer number and the wafer lot number of each device. Inspection lot records shall be maintained to provide traceability to the specific wafer and wafer lot from which the chips originated.

3.4. Burn-In and Life Test Circuit

The burn-in and life test circuit and conditions shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test methods 1005 and 1015 per MIL-STD-883.

4. QUALITY ASSURANCE PROVISIONS

4.1. Wafer Acceptance Testing

The wafer lot acceptance testing shall consist of Class Level S inspections per MIL-STD-883 TM 5007. All deliverable Die shall have passed 100% element electrical test per 4.2.1. Element evaluation per 4.2.2 and passed 100% visual inspection, per MIL-STD-883 TM2010 Condition A, after wafer dicing.

4.2. Dice Qualification Requirements

Dice qualification requirements shall be in accordance with MIL-PRF-38534, Appendix C, Table C-II, per Class K.

4.2.1. Element Electrical Test (RF-On Wafer)

Electrical tests shall consist of the tests specified on Table I, tested at room temperature only.

4.2.2. Element Evaluation (Lot Acceptance Testing)

Sample Die shall be randomly selected from the wafer that has successfully passed RF-On wafer testing per 4.2.1 and shall be mounted to suitable fixturing for screening.

4.2.2.1. Initial Electrical Test (Pre Burn-In)

Pre Burn-In electrical tests shall consist of the tests specified on Table II, tested at room temperature only.

4.2.2.2. Interim Electrical Test (Post Burn-In)

Post Burn-In electrical tests shall consist of the tests specified on Table II, tested at room temperature only and shall meet performance requirements in accordance with Table II and Table III.

4.2.2.3. Final Electrical Test (Post Life Test)

Final electrical tests shall consist of the tests specified in Table II, tested at -40 °C and +85 °C, which shall be Read and Record only, and shall meet performance requirements in accordance with Table II and Table III.

5. MIL-PRF-38534 EXCEPTIONS

5.1. Wafer Fabrication

Foundry information is available upon request.

5.2. Microcircuit Dice Evaluation Requirements (TABLE C-II)

- Pre-screen test post assembly required to Die qualification to remove all assembly related rejects.
- Subgroup 4: mechanical shock or constant acceleration not performed.
- Subgroup 4: Interim and post burn-in electrical tests will include tests screened at +25 °C only.

6. PREPARATION FOR DELIVERY

The preparation for delivery, packaging, preservation, ESD protection and handling shall be in accordance with MIL-PRF-38534.

6.1. <u>Die Packaging Information</u>

The Die shall be delivered in accordance with Table IV herein.

6.2. <u>Inspection Data Requirements</u>

The following data shall accompany each shipment.

- a. A Certificate of Conformance (C of C) certifies that the lot(s) meets all requirements of this specification.
- b. Die Photograph
- c. Attribute data for all tests.
- d. Wafer Lot Acceptance data including photos from SEM inspection in 4.1.
- e. Summary of RF-On wafer test data per 4.2.1.
- f. Element Evaluation test results per 4.2.2.
 - a. Variables data for electrical end-point measurements.
- g. Failure Analysis with photos (If applicable)
- h. A cover sheet indicating the following purchasing information:
 - 1. Customer purchase order number.
 - 2. Analog Devices part number.
 - 3. Part lot identification codes.
 - 4. Date & quantity shipped.

TABLE I: DIE ELECTRICAL CHARACTERISTICS

Parameter	Conditions <u>1</u> /	Limits		l lucita
Parameter	Unless otherwise specified	Min	Max	Units
Output Power	$F_{IN} = 9 \text{ GHz}$, 12 GHz, and 14 GHz	11		dBm
Supply Current (Idd1)	No Cinnal of DEIN		68	mA
Supply Current (Idd2)	No Signal at RFIN		40	mA

TABLE I Note:

 $\underline{1}$ / Limits apply at +25 °C only with Vdd1 = Vdd2 = +5 V and Drive Level = + 3 dBm

TABLE II: ELECTRICAL CHARACTERISTICS FOR QUALIFICATION SAMPLES

Parameter	Conditions <u>1/2/3</u> /	Sub-Group	Limits		Units	
raidilletei	Unless otherwise specified	3ub-Group	Min	Max	Oiilts	
Output Power	$F_{IN} = 9$ GHz, 12 GHz, and 14 GHz	4	11		dBm	
Supply Current (ldd1 + ldd2)	No Signal at RFIN	1		108	mA	

TABLE II Notes:

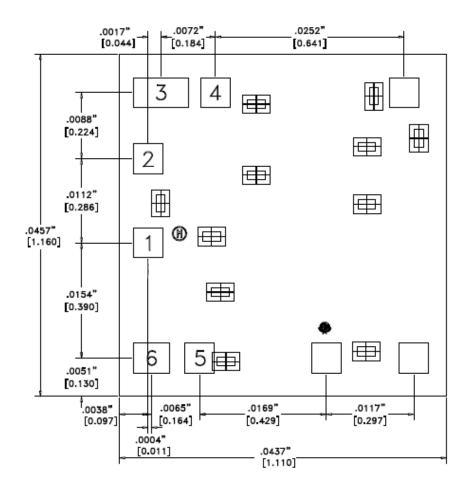
1/ Limits apply at +25 °C with Vdd1 = Vdd2 = +5 V and Drive Level = +3 dBm. 3/ -40 °C and +85 °C (Subgroup 2, 3, 5 and 6) shall be Read and Record only. 3/ See MIL-PRF-38534 Table C-Xa for subgroup parameter definitions.

TABLE III: BURN-IN/LIFE TEST DELTA LIMITS 1/2/3/

Parameter	Test Conditions	Delta Limits	Units
Output Power	Per Table II	± 1	dB
Supply Current (Idd1 +Idd2)	Per rable II	± 10	%

TABLE III Notes:

1/ Delta test is performed at T_A = +25 °C only.
2/ Table II limits will not be exceeded.
3/ Delta calculated pre/post 240 hours and post 240 hours / post 1000 hours.



NOTES:

- ALL DIMENSIONS ARE IN INCHES [MM]
- 2. DIE THICKNESS IS .004"
- 3. BOND PAD METALIZATION: GOLD
- 4. BACKSIDE METALIZATION: GOLD
- 5. BACKSIDE METAL IS GROUND
- 6. OVERALL DIE SIZE ±.002"

PAD	DESCRIPTION	PAD SIZE
1	Vdd1	.0039[.100] X .0039[.100]
2	Vdd2	.0039[.100] X .0039[.100]
3	RFOUT	.0074[.188] X .0039[.100]
4, 5	GND	.0039[.100] X .0039[.100]
6	RFIN	.0048[.121] X .0039[.100]

Figure 1 – Device Outline for the HMC8332

TABLE IV: DIE PACKAGING INFORMATION Standard Package Alternate GP-2 (Gel Pack) 1/

1/ For alternate packaging information, contact Analog Devices Inc.

TABLE IV Note:

ORDERING GUIDE

Model	Temperature Range	
HMC8332	−40 °C to +85 °C	

Revision History

Revision History			
Rev	Description of Change	Date	
Α	Initial release.	01/15/2025	

