SELECTED ITEM DRAWING

			ANALOG DEVICES	
Unless otherwise specified DIMENSIONS ARE IN INCHES (MM)	TOLERANCES: .XX +/- 0.010 .XXX +/- 0.005 .XXXX +/- 0.002 ANGLES +/- .5 DEG	Drawing practices per **ASME Y14.100**	**10 GHz, Latched Comparator With RSCML Output Stage**	
			SIZE **A**	DRAWING NUMBER **SID000056**

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1. SCOPE

1.1. Scope

This drawing establishes the requirements for the non-hermetic, 10 GHz, SiGe, MMIC, Latched Comparator with RSCML Output Stage, to be screened with guidelines to MIL-PRF-38535, Class Level S, to the requirements specified in 4.1, 4.2, and 4.3 herein.

1.2. Analog Devices Part Number

Generic Part Number	Screened Part Number
ADH675S	HMC6416LC3

2. APPLICABLE DOCUMENTS

2.1. Government Documents

Unless otherwise specified, the following drawings and standards, of the issue in effect on the date of the accepted purchase order, in the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, shall form a part of this drawing to the extent specified herein.

DEPARTMENT OF DEFENSE TEST METHOD STANDARD

MIL-STD-883	Microcircuits
MIL-STD-1580C	Destructive Physical Analysis for Electronic, Electromagnetic, and Electromechanical Parts

DEPARTMENT OF DEFENSE PERFORMANCE SPECIFICATIONS

MIL-PRF-38535	Integrated Circuits (Microcircuits) Manufacturing, General Specification For

2.2. Non-Government Documents

The following documents, of the issue in effect on the date of the purchase order, form a part of this drawing to the extent specified herein:

Analog Devices Inc.

ADI Standard Space Products Program – ASD-*lite*.

HMC675LC3C Data Sheet	Commercial Product Datasheet	v10.0514 (Reference Only)

3. REQUIREMENTS

3.1. General Requirements
The devices delivered shall comply to this specification.

3.2. Design Construction and Physical Dimensions
The design construction and physical dimensions shall be as defined in Figure 1 herein.

3.3. Traceability
Each delivered device shall be traceable to a production lot. Inspection lot records shall be maintained to provide traceability of its origin.

3.4. DPA
If specified on Purchase Order, DPA testing shall be done in accordance with MIL-STD-1580C, Sections 16.1.

3.5. Burn-In and Life Test Circuit
The burn-in and life test circuit and conditions shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test methods 1005 and 1015 per MIL-STD-883.

4. QUALITY ASSURANCE PROVISIONS

4.1. Wafer Lot Acceptance Testing
Not applicable.

4.2. Flight Screening Requirements
Flight screening requirements shall be per MIL-STD-883 TM 5004 for Class level S microcircuits modified for non-hermetic packaged MMIC devices.

4.2.1. Electrical Test Requirements
Electrical test requirements are defined in Table I herein.

4.2.2. Electrical Performance Characteristics
Electrical performance characteristics are specified on Table II herein.

4.2.3. Burn-In Delta Requirements
Pre and Post Burn-In Electrical test and delta parameters shall consist of the tests specified in Table III herein.

4.3. Quality Conformance Inspection (QCI)
Group B and Group D tests shall be performed per MIL-STD-883 TM 5005 for Class level S microcircuits modified for non-hermetic packaged MMIC devices.

4.3.1. Post Steady State Life Electrical Test
Post steady state life electrical tests shall consist of the tests specified per Table II tested at room temperature only. Devices must meet delta parameter requirements in accordance with Table III herein.

5. MIL-PRF-38535 ASD-LITE EXCEPTIONS

The manufacturing flow described in the ADI STANDARD SPACE PRODUCTS PROGRAM is to be considered a part of this specification.

5.1. Wafer Fabrication

Foundry information is available upon request.

5.2. Flight Screening Flow

Wafer lot Acceptance: Not applicable for non-hermetic air cavity packages.
Non-destruct Bond Pull: Not applicable for non-hermetic air cavity packages.
Internal visual inspection: DPA performed in lieu of visual – commercial criteria is applicable.
Seal, Fine Leak: Not applicable for non-hermetic air cavity packages.
Seal, Gross Leak: Not applicable for non-hermetic air cavity packages.

5.3. Group B

Subgroup 2: Resistance to solvents is not applicable.
Subgroup 3: Steam aging shall not be required for pre-conditioning.
Subgroup 4: Not applicable for non-hermetic air cavity packages.

5.4. Group D

Subgroup 2: Not applicable for non-hermetic air cavity packages.
Subgroup 5: Not Applicable for non-hermetic air cavity packages.
Subgroup 6: Not applicable for non-hermetic air cavity packages.
Subgroup 7: Not applicable for non-hermetic air cavity packages.
Subgroup 8: Not applicable for non-hermetic air cavity packages.
Subgroup 9: Not applicable for non-hermetic air cavity packages.

6. PREPARATION FOR DELIVERY

The preparation for delivery, packaging, preservation, ESD protection and handling shall be in accordance with MIL-PRF-38535.

6.1. Part Marking

Devices shall be marked as specified on Figure 1 herein.

6.2. Inspection Data Requirements

The following data shall accompany each shipment.

a. A Certificate of Conformance (C of C) certifies that the lot(s) meets all requirements of this specification.
b. DPA Report (if applicable)
c. Summary of electrical test requirements defined in 4.2 herein.
d. Summary of QCI results defined in 4.3 herein.
e. Failure Analysis with photos (If applicable)
f. A cover sheet indicating the following purchasing information:
    1. Customer purchase order number.
    2. Analog Devices part number.
    3. Part lot identification codes.
    4. Date & quantity shipped.

TABLE I: ELECTRICAL TEST REQUIREMENTS

Test Requirement	Subgroups (in accordance with MIL-PRF-38535, Table III)
Interim Electrical Parameters	1, 4
Final Electrical Parameters	1, 4 1/2/
Group A Electrical Parameters	1, 2, 3, 4, 5, 6
Group B End-Point Electrical Parameters	1, 4 2/
Group D End-Point Electrical Parameters	1, 4

TABLE I Notes:
1/ PDA applies to Table I subgroup 1 and Table III delta parameters.
2/ See Table III for delta parameters

TABLE II: ELECTRICAL PERFORMACE CHARACTERISTICS (-40 °C, +25 °C AND +85 °C)

Parameter	Test Conditions 1/2/ Unless otherwise specified	Group A Subgroups	Limits		Units
			Min	Max	
Iee Supply Current		1	-30	-20	mA
Icco Supply Current		1	5	20	mA
Icci Supply Current		1	5	20	mA
VHYS	Measure Volt drop across Rhys (100 Ohm)	1	0.08	0.2	V
TM int. LE 5GHz Vpp1	Track mode LE internal bias. 5GHz, -6 dBm INP input. Output Ch1=Q, Ch2=Qbar. Measure Vpp.	4	300	500	mV
TM int. LE 5GHz Vpp2	Track mode LE internal bias. 5GHz, -6 dBm INP input. Output Ch1=Q, Ch2=Qbar. Measure Vpp.	4	300	500	mV
TM int. LE 5GHz Tr1	Track mode LE internal bias. 5GHz, -6 dBm INP input. Output Ch1=Q, Ch2=Qbar. Measure Trise.	4	20	40	ps
TM int. LE 5GHz Tr2	Track mode LE internal bias. 5GHz, -6 dBm INP input. Output Ch1=Q, Ch2=Qbar. Meausre Trise.	4	20	40	ps
TM int. LE 5GHz Tf1	Track mode LE internal bias. 5GHz, -6 dBm INP input. Output Ch1=Q, Ch2=Qbar. Measure Tfall.	4	20	40	ps
TM int. LE 5GHz Tf1	Track mode LE internal bias. 5GHz, -6 dBm INP input. Output Ch1=Q, Ch2=Qbar. Measure Tfall.	4	20	40	ps
Tmode A 5GHz Vpp1	Track mode LE Low DC, LE=1.6V, LEbar=2.4V. 5GHz, -6 dBm INP input. Output Ch1=Q, Ch2=Qbar. Measure Vpp.	4	300	500	mV
Tmode A 5GHz Vpp2	Track mode LE Low DC, LE=1.6V, LEbar=2.4V. 5 GHz, -6 dBm INP input. Output Ch1=Q, Ch2=Qbar. Measure Vpp.	4	300	500	mV
Tmode A 5GHz Tr1	Track mode LE Low DC, LE=1.6V, LEbar=2.4V. 5 GHz, -6 dBm INP input. Output Ch1=Q, Ch2=Qbar. Measure Trise.	4	20	40	ps
Tmode A 5GHz Tr2	Track mode LE Low DC, LE=1.6V, LEbar=2.4V. 5 GHz, -6 dBm INP input. Output Ch1=Q, Ch2=Qbar. Measure Trise.	4	20	40	ps
Tmode A 5GHz Tf1	Track mode LE Low DCLE=1.6V, LEbar=2.4V. 5 GHz, -6 dBm INP input. Output Ch1=Q, Ch2=Qbar. Measure Tfall.	4	20	40	ps
Tmode A 5GHz Tf2	Track mode LE Low DCLE=1.6V, LEbar=2.4V. 5 GHz, -6 dBm INP input. Output Ch1=Q, Ch2=Qbar. Measure Tfall.	4	20	40	ps
Tmode B 5GHz Vpp1	Track mode LE Low DCLE=1.6V, LEbar=2.4V. 5 GHz, -6 dBm INN input. Output Ch1=Q, Ch2=Qbar. Measure Vpp.	4	300	500	mV
Tmode B 5GHz Vpp2	Track mode LE Low DCLE=1.6V, LEbar=2.4V. 5 GHz, -6 dBm INN input. Output Ch1=Q, Ch2=Qbar. Measure Vpp.	4	300	500	mV

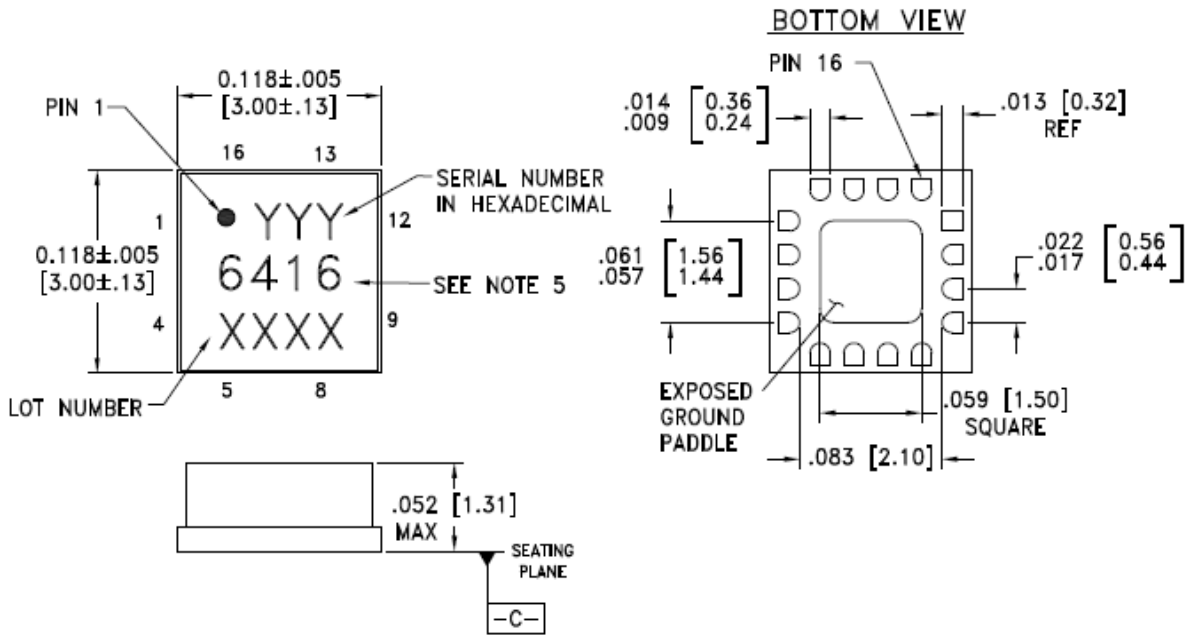
Tmode B 5GHz Tr1	Track mode LE Low DCLE=1.6V, LEbar=2.4V. 5 GHz, -6 dBm INN input. Output Ch1=Q, Ch2=Qbar. Measure Trise.	4	20	40	ps
Tmode B 5GHz Tr2	Track mode LE Low DCLE=1.6V, LEbar=2.4V. 5 GHz, -6 dBm INN input. Output Ch1=Q, Ch2=Qbar. Measure Trise.	4	20	40	ps
Tmode B 5GHz Tf1	Track mode LE Low DCLE=1.6V, LEbar=2.4V. 5 GHz, -6 dBm INN input. Output Ch1=Q, Ch2=Qbar. Measure Tfall.	4	20	40	ps
Tmode B 5GHz Tf2	Track mode LE Low DCLE=1.6V, LEbar=2.4V. 5 GHz, -6 dBm INN input. Output Ch1=Q, Ch2=Qbar. Measure Tfall.	4	20	40	ps
Hold Mode V CH1	Firstly set to Track Mode LE-LEbar=L. Set INP-INN=300mV DC. Secondly, set to Hold Mode LE-LEbar=H. App 5 GHz -6 dBm to INP. Measure output volts. Ch1=Q, Ch2=Qbar.	4	-0.01	0	V
Hold Mode V CH2	Firstly set to Track Mode LE-LEbar=L. Set INP-INN=300mV DC. Secondly, set to Hold Mode LE-LEbar=H. App 5 GHz -6dBm to INP. Measure output volts. Ch1=Q, Ch2=Qbar.	4	-0.43	-0.33	V
TM SL Offset Ch1	Set to Track Mode LE-LEbar=L. Set INP=-10mV, INN=0V DC. Measure output volts. Ch1=Q, Ch2=Qbar.	4	-0.43	-0.33	V
TM SL Offset Ch2	Set to Track Mode LE-LEbar=L. Set INP=-10mV, INN=0V DC. Measure output volts. Ch1=Q, Ch2=Qbar.	4	-0.01	0	V
TM SH Offset Ch1	Set to Track Mode LE-LEbar=L. Set INP=+10mV, INN=0V DC. Measure output volts. Ch1=Q, Ch2=Qbar.	4	-0.01	0	V
TM SH Offset Ch2	Set to Track Mode LE-LEbar=L. Set INP=+10mV, INN=0V DC. Measure output volts. Ch1=Q, Ch2=Qbar.	4	-0.43	-0.33	V

TABLE II Notes:
1/ Test limits apply at +25 °C only with Vcci = +3.3 V, Vcco = 0 V, Vee = -3 V
2/ -40 °C and +85 °C (Subgroups 2, 3, 5 and 6) are Read and Record only.

TABLE III: BURN-IN/LIFE TEST DELTA LIMITS 1/2/3/

Parameter	Test Conditions	Delta Limits	Units
Iee Supply Current	Per Table II	± 10	%
Icco Supply Current			
Icci Supply Current			

TABLE III Notes:
1/ Delta test is performed at T_A = +25 °C only.
2/ Table II limits will not be exceeded.
3/ Deltas calculated at pre/post 240 hours and post 240 hours / post 1000 hours.



NOTES:

1. PACKAGE BODY MATERIAL: ALUMINA
2. LEAD AND GROUND PADDLE PLATING: 30-80 MICROINCHES GOLD OVER 50 MICROINCHES MINIMUM NICKEL.
3. DIMENSIONS ARE IN INCHES [MILLIMETERS].
4. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
5. CHARACTERS TO BE INK OR LASER MARKED WITH .018" MIN TO .030" MAX HEIGHT REQUIREMENTS. UTILIZE MAXIMUM CHARACTER HEIGHT BASED ON LID DIMENSIONS AND BEST FIT. LOCATE APPROX. AS SHOWN.
6. PACKAGE WARP SHALL NOT EXCEED 0.05mm DATUM -C-
7. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.

PIN #	FUNCTION	PIN #	FUNCTION
1	VTP	9	VCCO
2	INP	10	$\overline{Q}$
3	INN	11	Q
4	VTN	12	VCCO
5	VCCI	13	VEE
6	$\overline{LE}$	14	HYS
7	LE	15	RTN
8	NC	16	VCCI

The HMC6416LC3 has a MSL rating of MSL3.

Figure 1 – Device Outline for the HMC6416LC3

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
HMC6416LC3	–40 °C to +85 °C	16-Lead Ceramic Leadless Chip Carrier	LCC (E-16-3)

Revision History

Revision History		
Rev	**Description of Change**	**Date**
A	Initial release.	12/03/2024
B	Update Section 1.2, Figure 1, and Ordering Guide	2/07/2025

ANALOG DEVICES

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