SELECTED ITEM DRAWING

			ANALOG DEVICES	
Unless otherwise specified DIMENSIONS ARE IN INCHES (MM)	TOLERANCES: .XX +/- 0.010 .XXX +/- 0.005 .XXXX +/- 0.002 ANGLES +/- .5 DEG	Drawing practices per **ASME Y14.100**	**8 GHz, 19-Bit Fractional-N PLL**	
			SIZE **A**	DRAWING NUMBER **SID000044**

One Analog Way, Wilmington, MA 01887-2356, U.S.A.
Tel: 781.935.5565 **www.analog.com**
Tel: 800.262.5643

1. SCOPE

1.1. Scope

This drawing establishes the requirements for the 8 GHz, SiGe BiCMOS, 8 GHz, 19-Bit Fractional-N PLL, assembled hermetically in the G24 package, to be screened in accordance with MIL-PRF-38535, Class Level S, to the requirements specified in 4.1, 4.2, and 4.3 herein.

1.2. Analog Devices Part Number

Generic Part Number	Screened Part Number
ADH704S	HMC7910G24

2. APPLICABLE DOCUMENTS

2.1. Government Documents

Unless otherwise specified, the following drawings and standards, of the issue in effect on the date of the accepted purchase order, in the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, shall form a part of this drawing to the extent specified herein.

DEPARTMENT OF DEFENSE TEST METHOD STANDARD

MIL-STD-883 Microcircuits

DEPARTMENT OF DEFENSE PERFORMANCE SPECIFICATIONS

MIL-PRF-38535 Integrated Circuits (Microcircuits) Manufacturing, General Specification For

2.2. Non-Government Documents

The following documents, of the issue in effect on the date of the purchase order, form a part of this drawing to the extent specified herein:

Analog Devices Inc.

ADI Standard Space Products Program – ASD-*Lite*.

HMC704LP4E Data Sheet	Commercial Product Datasheet	v04.0215 (Reference Only)

3. REQUIREMENTS

3.1. General Requirements
The devices delivered shall comply to this specification.

3.2. Design Construction and Physical Dimensions
The design construction and physical dimensions shall be as defined in Figure 1 herein.

3.3. Traceability
Each delivered device shall be traceable to the wafer lot and wafer number. Inspection lot records shall be maintained to provide traceability to the specific wafer and wafer lot from which the chips originated as well as traceability to package and materials.

3.4. Burn-In and Life Test Circuit
The burn-in and life test circuit and conditions shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test methods 1005 and 1015 per MIL-STD-883.

4. QUALITY ASSURANCE PROVISIONS

4.1. Wafer Lot Acceptance Testing
The wafer lot acceptance testing shall consist of Class Level S inspections per MIL-STD-883 TM 5007.

4.2. Flight Screening Requirements
Flight screening requirements shall be per MIL-STD-883 TM 5004 for Class level S microcircuits.

4.2.1. Electrical Test Requirements
Electrical test requirements are defined in Table I herein.

4.2.2. Electrical Performance Characteristics
Electrical performance characteristics are specified on Table II herein.

4.2.3. Burn-In Delta Requirements
Pre and Post Burn-In Electrical test and delta parameters shall consist of the tests specified in Table III herein.

4.3. Quality Conformance Inspection (QCI)
Group B and Group D tests shall be performed per MIL-STD-883 TM 5005 for Class level S microcircuits.

4.3.1. Post Steady State Life Electrical Test
Post steady state life electrical tests shall consist of the tests specified per Table II tested at room temperature only. Devices must meet delta parameter requirements in accordance with Table III herein.

5. MIL-PRF-38535 ASD-LITE EXCEPTIONS

The manufacturing flow described in the ADI STANDARD SPACE PRODUCTS PROGRAM is to be considered a part of this specification.

5.1. Wafer Fabrication
Foundry information is available upon request.

5.2. Device Assembly
Device contains bi-metallic wire bonds (Gold bond wires on Aluminum Die pads)

5.3. Flight Screening Flow
Reverse Bias Burn-In: Not applicable.

5.4. Group B
Subgroup 2: Resistance to solvents is not applicable.

5.5. Group D
Subgroup 5: Not applicable.

6. PREPARATION FOR DELIVERY

The preparation for delivery, packaging, preservation, ESD protection and handling shall be in accordance with MIL-PRF-38535.

6.1. Part Marking
Devices shall be marked as specified on Figure 1 herein.

6.2. Inspection Data Requirements
The following data shall accompany each shipment.

a. A Certificate of Conformance (C of C) certifies that the lot(s) meets all requirements of this specification.
b. Wafer Lot Acceptance data including photos from SEM Inspection defined in 4.1 herein.
c. Summary of electrical test requirements defined in 4.2 herein.
d. Summary of QCI results defined in 4.3 herein.
e. Failure Analysis with photos (If applicable)
f. A cover sheet indicating the following purchasing information:
    1. Customer purchase order number.
    2. Analog Devices part number.
    3. Part lot identification codes.
    4. Date & quantity shipped.

TABLE I: ELECTRICAL TEST REQUIREMENTS

Test Requirement	Subgroups (in accordance with MIL-PRF-38535, Table III)
Interim Electrical Parameters	1, 4,
Final Electrical Parameters	1, 4 1/2/
Group A Electrical Parameters	1, 2, 3, 4, 5, 6
Group B End-Point Electrical Parameters	1, 4 2/
Group D End-Point Electrical Parameters	1, 4

TABLE I Notes:
1/ PDA applies to Table I subgroup 1 and Table III delta parameters.
2/ See Table III for delta parameters

TABLE II: ELECTRICAL PERFORMACE CHARACTERISTICS (-40 °C, +25 °C AND +70 °C)

Parameter	Test Conditions 1/2/ Unless otherwise specified	Group A Subgroups	Limits		Units
			Min	Max	
Flicker Figure of Merit	Integer Mode 3/4/	4, 5, 6		-262	dBc/Hz
	Fractional Normal Mode 5/6/	4, 5, 6		-262	dBc/Hz
Floor Figure of Merit	Integer Mode 3/4/	4, 5, 6		-225	dBc/Hz
	Fractional Normal Mode 5/6/	5		-223	dBc/Hz
	Fractional Hik Mode 5/6/	5		-225	dBc/Hz
Derived SSB Phase Noise	10 kHz Offset, Integer Normal Mode 3/4/7/8/	4, 5, 6		-119.5	dBc/Hz
	50 kHz Offset, Integer Normal Mode 3/4/7/8/	4, 5, 6		-122	dBc/Hz
	100 kHz Offset, Integer Normal Mode 3/4/7/8/	4, 5, 6		-122.5	dBc/Hz
SSB Phase Noise	10 kHz Offset, Fractional Normal Mode 5/6/	5		-99.8	dBc/Hz
	10 kHz Offset, Fractional HiK Mode 5/6/	5		-100.9	dBc/Hz
	50 kHz Offset, Fractional Normal Mode 5/6/	5		-101.2	dBc/Hz
	50 kHz Offset, Fractional HiK Mode 5/6/	5		-102.8	dBc/Hz
	100 kHz Offset, Fractional Normal Mode 5/6/	5		-101.7	dBc/Hz
	100 kHz Offset, Fractional HiK Mode 5/6/	5		-103.5	dBc/Hz
Integer Boundary Spurs	Integer Normal Mode 3/4/	4, 5, 6		-60	dBc
Bias Reference Enable Current	3/4/	1, 2, 3	1.37	1.84	mA
Charge Pump Enable Current	3/4/	1, 2, 3	2.5	6	mA
Phase Detector Enable Current	3/4/	1, 2, 3	1.02	1.66	mA
Reference Path Buffer Enable Current	3/4/	1, 2, 3	6.1	9.12	mA
VCO Path RF Buffer Enable Current	3/4/	1, 2, 3	3.38	4.6	mA
VCO Divider Clock to Digital Enable Current	3/4/	1, 2, 3	0.93	3	mA
Pre-Scaler Clock Enable Current	3/4/	1, 2, 3	17.5	25.63	mA
VCO Buffer and Pre-scaler Bias Enable Current	3/4/	1, 2, 3	21.33	30.91	mA
Charge Pump Internal Opamp Enable Current	3/4/	1, 2, 3	0.57	0.75	mA
External VCO Input Div 2 Enable Current	3/4/	1, 2, 3	0.55	1.66	mA

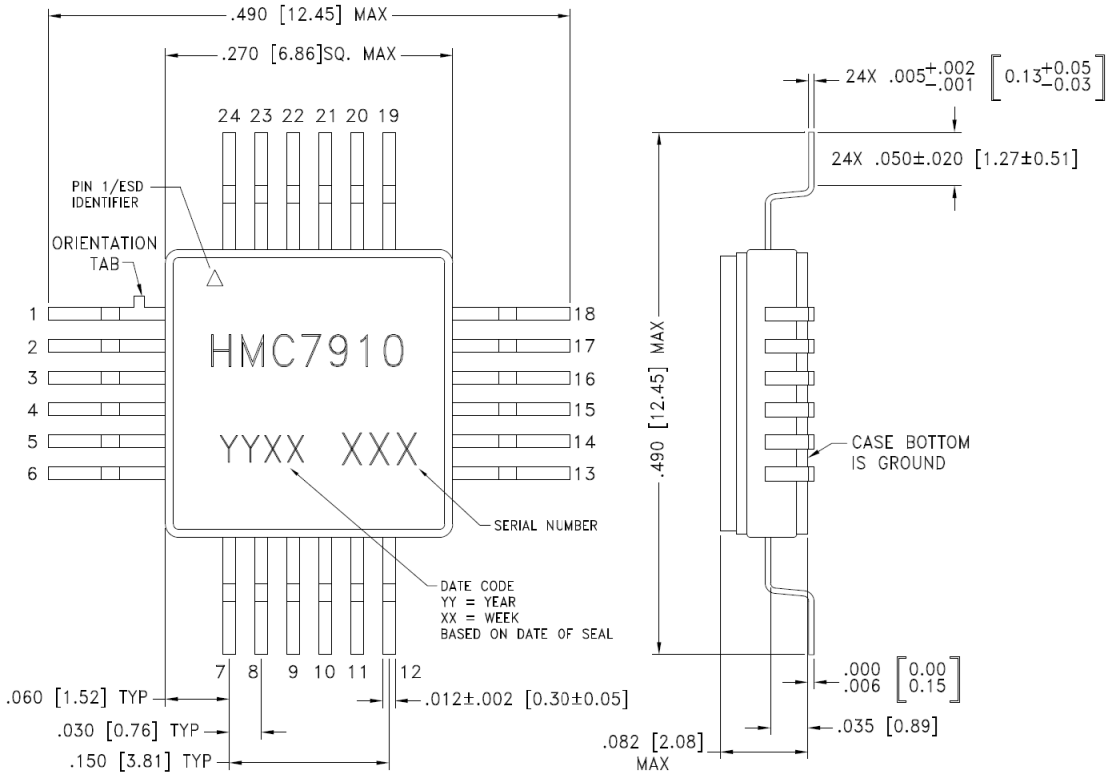
TABLE II Notes:
1/ VDDLS, VPPCP = +5 V nom; RVDD, AVDD, DVDD, VCCPS, VCCHF, VCCPD = +3.3 V nom; GND = 0 V
2/ VCOIN decoupled to the ground plane with a 100 pF ceramic bypass capacitor.
3/ Output Frequency = 1000 MHz, Reference Frequency = 100 MHz, Phase Detector Frequency (PFD_Freq) = 50 MHz
4/ Passive Loop Filter per Figure 2 herein
5/ Output Frequency = 7995 MHz, Reference Frequency = 50 MHz, Phase Detector Frequency (PFD_Freq) = 50 MHz.
6/ Active Loop Filter per Figure 3 herein
7/ Max limit is not guaranteed. Limit is based from the measured Flicker Figure of Merit (Flicker_FOM) and Floor Figure of Merit (Floor_FOM)
8/ Derived phase noise is calculated based from the following equations:

PN_{flick} = Flicker_FOM + 20log (f_{vco}) – 10log(f_{offset})
PN_{floor} =Floor_FOM + 10log(PFD_Freq) + 20log(f_{vco}/PFD_Freq)
PN = 10log((10^(PN_{flick}/10) + 10^(PN_{floor}/10)))

TABLE III: BURN-IN/LIFE TEST DELTA LIMITS 1/2/3/4/

Parameter	Test Conditions	Delta Limits	Units
Bias Reference Enable Current	Per Table II	± 0.27	mA
Charge Pump Enable Current		± 0.63	mA
Phase Detector Enable Current		± 0.37	mA
Reference Path Buffer Enable Current		± 1.74	mA
VCO Path RF Buffer Enable Current		± 0.66	mA
VCO Divider Clock to Digital Enable Current		± 1.2	mA
Pre-Scaler Clock Enable Current		± 4.67	mA
VCO Buffer and Pre-scaler Bias Enable Current		± 5.5	mA
Charge Pump Internal Opamp Enable Current		± 0.14	mA
External VCO Input Div 2 Enable Current		± 0.63	mA

TABLE III Notes:
1/ Delta test is performed at T_A = +25 °C only.
2/ Table II limits will not be exceeded.
3/ Passive Loop Filter configuration per Figure 2.
4/ Deltas calculated at pre/post 240 hours and post 240 hours / post 1000 hours.



NOTES:

1. PACKAGE MATERIAL: ALUMINA LOADED BOROSILICATE GLASS (#7052 CORNING).
2. LEADS, BASE, COVER MATERIAL: KOVAR™.
3. PLATING: ELECTROLYTIC GOLD 50 MICROINCHES MIN., OVER ELECTROLYTIC NICKEL 75 MICROINCHES MIN.
4. ALL DIMENSIONS ARE IN INCHES [MILLIMETERS].
5. TOLERANCES: ±.005 [0.13] UNLESS OTHERWISE SPECIFIED.
6. CHARACTERS TO BE LASER MARKED WITH .018 MIN to .030 MAX HEIGHT REQUIREMENTS. UTILIZE MAXIMUM CHARACTER HEIGHT BASED ON LID DIMENSIONS AND BEST FIT. LOCATE APPROX. AS SHOWN.
7. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.

PIN #	FUNCTION	PIN #	FUNCTION	PIN #	FUNCTION
1	SDI	9	VCCPS	17	VDDLS
2	SCK	10	GND	18	RVDD
3	ASEN	11	VCCPD	19	XREFP
4	LD_SDO	12	BIAS	20	ASCK
5	VCOIN	13	GND	21	ASD
6	VCOIP	14	AVDD	22	DVDD
7	VCCHF	15	VPPCP	23	CEN
8	GND	16	CP	24	SEN

Figure 1 – Device Outline for the HMC7910G24

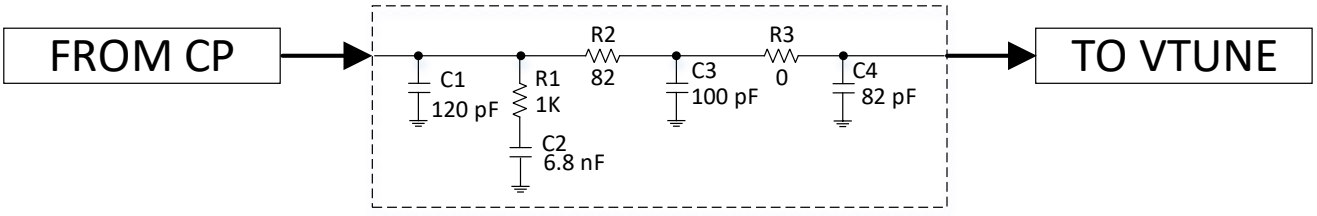


Figure 2 – Passive Loop Filter Configuration

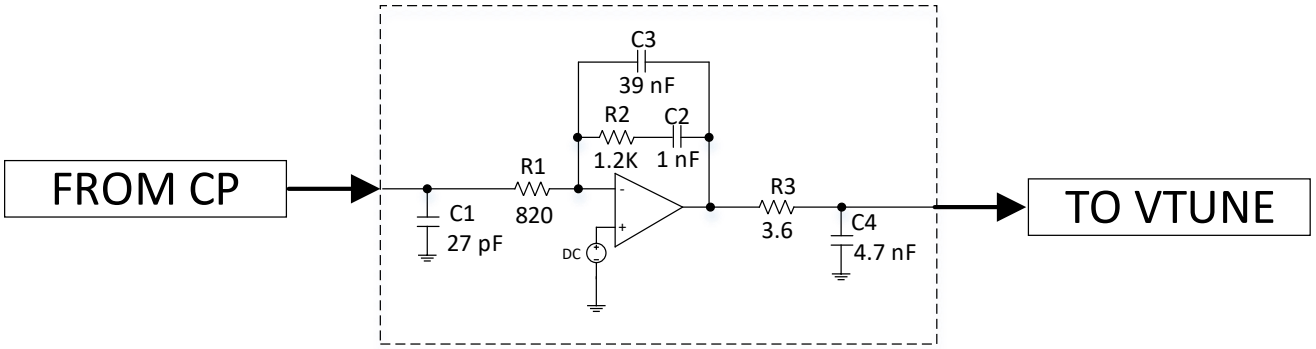


Figure 3 – Active Loop Filter Configuration

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
HMC7910G24	–40 °C to +70 °C	24-Lead Glass/Metal Hermetic SMT	G24 (FR-24-1)

Revision History

Revision History		
Rev	**Description of Change**	**Date**
A	Initial Release.	10/24/2024

Printed in the U.S.A. **10/2024**

ANALOG DEVICES

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