

SELECTED ITEM DRAWING

			
Unless otherwise specified DIMENSIONS ARE IN INCHES (MM)	TOLERANCES: .XX +/- 0.010 .XXX +/- 0.005 .XXXX +/- 0.002 ANGLES +/- .5 DEG	Drawing practices per ASME Y14.100	DC to 15 GHz, Power Amplifier
			<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%; text-align: center;"> SIZE A </td> <td style="width: 50%; text-align: center;"> DRAWING NUMBER SID000023 </td> </tr> </table>
SIZE A	DRAWING NUMBER SID000023		

SID000023 **Rev. B**
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1. SCOPE

1.1. Scope

This drawing establishes the requirements for the DC to 15 GHz, GaAs, PHEMT, MMIC, Power Amplifier, to be screened in accordance with MIL-PRF-38534, Class K, to the requirements specified in 4.1, and 4.2 herein.

1.2. Analog Devices Part Number

Generic Part Number

ADH659S

Screened Part Number

HMC8418

2. APPLICABLE DOCUMENTS

2.1. Government Documents

Unless otherwise specified, the following drawings and standards, of the issue in effect on the date of the accepted purchase order, in the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, shall form a part of this drawing to the extent specified herein.

DEPARTMENT OF DEFENSE TEST METHOD STANDARD

MIL-STD-883

Microcircuits

DEPARTMENT OF DEFENSE PERFORMANCE SPECIFICATIONS

MIL-PRF-38534

Hybrid Microcircuits, General Specifications For

2.2. Non-Government Documents

The following documents, of the issue in effect on the date of the purchase order, form a part of this drawing to the extent specified herein:

Analog Devices Inc.

HMC659 Data Sheet

Commercial Product Die Datasheet

v02.0217 (Reference Only)

3. REQUIREMENTS

3.1. General Requirements

The devices delivered shall comply to this specification.

3.2. Design Construction and Physical Dimensions

The design construction and physical dimensions shall be as defined in Figure 1 herein.

3.3. Traceability

Each delivered device shall be traceable to the wafer number and the wafer lot number of each device. Inspection lot records shall be maintained to provide traceability to the specific wafer and wafer lot from which the chips originated.

3.4. Burn-In and Life Test Circuit

The burn-in and life test circuit and conditions shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test methods 1005 and 1015 per MIL-STD-883.

4. QUALITY ASSURANCE PROVISIONS

4.1. Wafer Acceptance Testing

The wafer lot acceptance testing shall consist of Class Level S inspections per MIL-STD-883 TM 5007. All deliverable Die shall have passed 100% element electrical test per 4.2.1. Element evaluation per 4.2.2 and passed 100% visual inspection, per MIL-STD-883 TM2010 Condition A, after wafer dicing.

4.2. Dice Qualification Requirements

Dice qualification requirements shall be in accordance with MIL-PRF-38534, Appendix C, Table C-II, per Class K.

4.2.1. Element Electrical Test (RF-On Wafer)

Electrical tests shall consist of the tests specified on Table I, tested at room temperature only.

4.2.2. Element Evaluation (Lot Acceptance Testing)

Sample Die shall be randomly selected from the wafer that has successfully passed RF-On wafer testing per 4.2.1 and shall be mounted to suitable fixturing for screening.

4.2.2.1. Initial Electrical Test (Pre Burn-In)

Pre Burn-In electrical tests shall consist of the tests specified on Table II, tested at room temperature only.

4.2.2.2. Interim Electrical Test (Post Burn-In)

Post Burn-In electrical tests shall consist of the tests specified on Table II, tested at room temperature only and shall meet performance requirements in accordance with Table II and Table III.

4.2.2.3. Final Electrical Test (Post Life Test)

Final electrical tests shall consist of the tests specified in Table II, tested at -40 °C and +85 °C and shall meet performance requirements in accordance with Table II and Table III.

5. MIL-PRF-38534 EXCEPTIONS

5.1. Wafer Fabrication

Foundry information is available upon request.

5.2. Microcircuit Dice Evaluation Requirements (TABLE C-II)

- Pre-screen test post assembly required to Die qualification to remove all assembly related rejects.
- Subgroup 4: mechanical shock or constant acceleration not performed.
- Subgroup 4: Interim and post burn-in electrical tests will include tests screened at +25 °C only.

6. PREPARATION FOR DELIVERY

The preparation for delivery, packaging, preservation, ESD protection and handling shall be in accordance with MIL-PRF-38534.

6.1. Die Packaging Information

The Die shall be delivered in accordance with Table III herein.

6.2. Inspection Data Requirements

The following data shall accompany each shipment.

- a. A Certificate of Conformance (C of C) certifies that the lot(s) meets all requirements of this specification.
- b. Die Photograph
- c. Attribute data for all tests.
- d. Wafer Lot Acceptance data including photos from SEM inspection in 4.1.
- e. Summary of RF-On wafer test data per 4.2.1.
- f. Element Evaluation test results per 4.2.2.
 - a. Variables data for electrical end-point measurements.
- g. Failure Analysis with photos (If applicable)
- h. A cover sheet indicating the following purchasing information:
 1. Customer purchase order number.
 2. Analog Devices part number.
 3. Part lot identification codes.
 4. Date & quantity shipped.

TABLE I: DIE ELECTRICAL CHARACTERISTICS

Parameter	Conditions <u>1/3/</u> Unless otherwise specified	Limits			Units
		Min	Typ	Max	
Gain	RFIN = 15 GHz	14.8			dB
Output Power for 1 dB Compression (OP1dB) <u>2/</u>	RFIN = 15 GHz	22.5			dBm
Supply Current (Idd)	No Signal at RFIN		300	350	mA

TABLE I Notes:

1/ Test limits apply at +25 °C only with Vdd = +8 V, Vgg2 = +3 V, and Idd = 300 mA.

2/ OP1dB testing is go-no-go confirming minimum requirements are met.

3/ Adjust Vgg1 between -2 V and +0 V to achieve Idd = 300 mA typical.

TABLE II: ELECTRICAL CHARACTERISTICS FOR QUALIFICATION SAMPLES

Parameter	Conditions <u>1/3/4/5/</u> Unless otherwise specified	Sub-Group	Limits			Units
			Min	Typ	Max	
Gain	RFIN = 15 GHz	4, 5, 6	17			dB
Output Power for 1 dB Compression (OP1dB) <u>2/</u>	RFIN = 15 GHz	7, 8A, 8B	22.5			dBm
Supply Current (Idd)	No Signal at RFIN	1, 2, 3		300	350	mA

TABLE II Notes:

1/ Test limits apply between -40 °C and +85 °C only with Vdd = +8 V, Vgg2 = +3 V, and Idd = 300 mA.

2/ OP1dB testing is go-no-go confirming minimum requirements are met.

3/ Adjust Vgg1 between -2 V to 0 V to achieve Idd = 300 mA typical at -40 °C, +25 °C, and +85 °C.

4/ Each device shall use the individual Vgg1 voltage established at pre burn-in throughout all electrical testing.

5/ See MIL-PRF-38534 Table C-Xa for subgroup parameter definitions.

TABLE III: BURN-IN/LIFE TEST DELTA LIMITS 1/2/3/4/

Parameter	Test Conditions	Delta Limits	Units
Gain	Per Table II	± 1	dB
Supply Current (Idd)		± 10	%

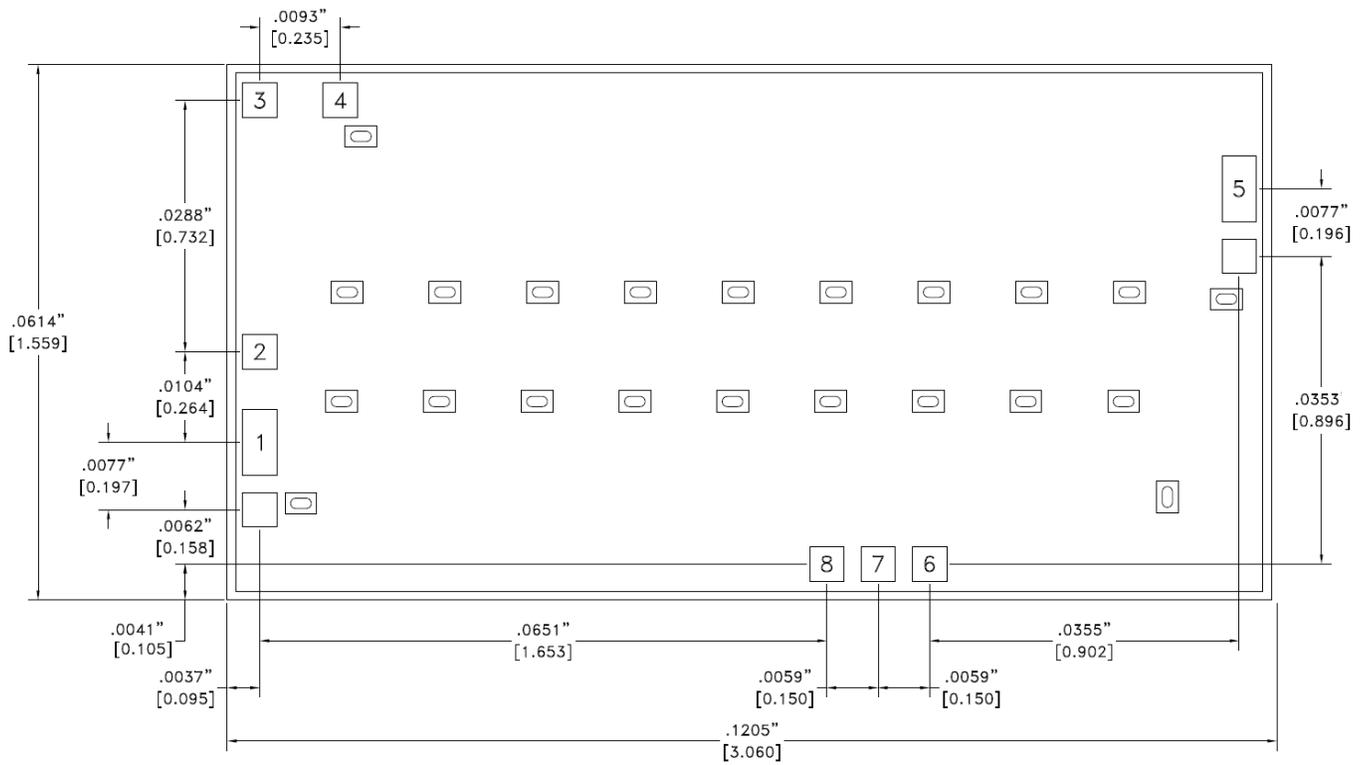
TABLE III Notes:

1/ Delta test is performed at TA = +25 °C only.

2/ Table II limits will not be exceeded.

3/ Delta calculated pre/post 240 hours and post 240 hours / post 1000 hours.

4/ Vgg1 voltage set to pre burn-in value for each device.



NOTES:

1. ALL DIMENSIONS ARE IN INCHES [MM]
2. DIE THICKNESS IS .004"
3. BOND PAD METALIZATION: GOLD
4. BACKSIDE METALIZATION: GOLD
5. BACKSIDE METAL IS GROUND
7. NO CONNECTION REQUIRED FOR UNLABELED BOND PADS
6. OVERALL DIE SIZE $\pm .002$ "

PAD	DESCRIPTION	PAD SIZE
1	RFIN	.0039[.100] X .0076[.193]
2	Vgg2	.0039[.100] X .0039[.100]
3	ACG1	.0039[.100] X .0039[.100]
4	ACG2	.0039[.100] X .0039[.100]
5	RFOUT	.0039[.100] X .0076[.193]
6	Vgg1	.0039[.100] X .0039[.100]
7	ACG3	.0039[.100] X .0039[.100]
8	ACG4	.0039[.100] X .0039[.100]

Figure 1 – Device Outline for the HMC8418

TABLE IV: DIE PACKAGING INFORMATION

Standard Package	Alternate
GP-1 (Gel Pack)	<u>1</u> /

TABLE III Note:

1/ For alternate packaging information, contact Analog Devices Inc.

ORDERING GUIDE

Model	Temperature Range
HMC8418	-40 °C to +85 °C

Revision History

Revision History		
Rev	Description of Change	Date
A	Initial release.	10/07/2024
B	Update Section 2.1 and Table II	01/02/2025