REVISION RECORD		
REV	DESCRIPTION	DATE
0	INITIAL RELEASE	06/12/96
A	• PAGE 2: ADDED PARAGRAPHS 3.2.1 AND 3.2.2. PARAGRAPH 3.3.b HAD "(SEE PARAGRAPH 3.2)". • PAGE 3: ADDED PARAGRAPHS 3.8.1 AND 3.8.2. • PAGE 4: PARAGRAPH 4.4.2, GROUP B INSPECTION WAS REDEFINED. • PAGE 5: PARAGRAPH 4.4.3, GROUP D INSPECTION WAS REDEFINED. PARAGRAPH 4.5, SOURCE INSPECTION, REDEFINED.	12/01/97
B	• PAGE 4, AMENDED PARAGRAPHS 4.1 AND 4.1.1 TAKING EXCEPTION TO ANALYSIS OF CATASTROPHIC FAILURES.	03/20/98
C	• PAGE 6, TO5 CASE OUTLINE, CHANGED θjc FROM 60°C/W TO 40°C/W, θja DOES NOT CHANGE. • PAGE 7, CERAMIC DIP CASE OUTLINE, CHANGED θja FROM 120°C/W TO 110°C/W, θjc CHANGED FROM 50°C/W TO 30°C/W.	07/14/99
D	• PAGE 3, PARAGRAPHS 3.2.1, 3.2.2, HAD FIGURES 1, 2, REMOVED. • PAGE 4, PARAGRAPH 3.7, CHANGED VERBIAGE FROM "SPECIFIED IN TABLE III" TO "AND AS SPECIFIED IN TABLE III HEREIN", LINE 2. PARAGRAPH 3.9, ADDED "HEREIN" AFTER TABLE II", LINE 2. • PAGE 5, PARAGRAPH 4.3, ADDED "HEREIN" AFTER "TABLE III", LINE 2. PARAGRAPH 4.4.1, ADDED "HEREIN" AFTER "TABLE III", LINE 2. 4.4.2.2, CHANGED VERBIAGE IN LINE 1 FROM "ALL FOOTNOTES OF TABLE IIA OF MIL-STD-883" TO "ALL FOOTNOTES PERTAINING TO TABLE IIA IN MIL-STD-883". • PAGE 6, PARAGRAPH 4.4.3.2, CHANGED VERBIAGE IN LINE 1 FROM "ALL FOOTNOTES OF TABLE IV OF MIL-STD-883" TO "ALL FOOTNOTES PERTAINING TO TABLE IV IN MIL-STD-883".	01/04/00
E	• PAGE 3, PARAGRAPH 3.2.3, 03 ADDED RH37W10 (FLATPAK GLASS SEAL, 10 LEAD). • PAGE 4, PARAGRAPH 3.8.3, ADDED OPTION 3. PARAGRAPH 3.10.1, ADDED FIGURE 3. PARAGRAPH 3.10.2, CHANGED TO FIGURE 4, 5 AND ADDED FIGURE 6. • PAGE 5, PARAGRAPH 3.11.3, CHANGED FIGURE TO 13. • PAGE 9, ADDED DEVICE OPTION 03. • PAGE 10, ADDED FIGURE 6. • PAGE 15, ADDED DEVICE OPTION 03, STATIC BURN-IN CIRCUIT. • PAGE 16, ADDED DEVICE OPTION 03, DYNAMIC BURN-IN CIRCUIT. • PAGE 18, CHANGED NOTES FROM ALPHABETICAL ORDER TO NUMBER'S PER LTC DATA SHEET.	07/06/00

REVISION RECORD AND DESCRIPTION CONTINUED ON NEXT PAGE.

CAUTION: ELECTROSTATIC DISCHARGE SENSITIVE PART

REVISION	PAGE NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
INDEX	REVISION	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**	**P**
REVISION	PAGE NO.	18	19	20	21	22												
INDEX	REVISION	**P**	**P**	**P**	**P**	**P**												

				LINEAR TECHNOLOGY CORPORATION MILPITAS, CALIFORNIA		
	ORIG			TITLE:		
	DSGN			**MICROCIRCUIT, LINEAR, RH37C, PRECISION OPERATIONAL AMPLIFIER**		
	ENGR					
	MFG					
	CM					
	QA			SIZE	CAGE CODE	DRAWING NUMBER	REV
	PROG				**64155**	**05-08-5030**	**P**
APPLICATION	FUNCT	SIGNOFFS	DATE	CONTRACT:		

FOR OFFICIAL USE ONLY

REVISION RECORD		
REV	DESCRIPTION	DATE
F	• PAGE 9, CHANGED THETA JA TO 0JA=170°C/W AND THETA JC 0JC=40°C/W FROM 0JA=225°C/W AND 0JC=18°C/W PER PACKAGE ENGINEER.	09/05/00
G	• PAGE 3, PARAGRAPHS 3.2.1, 3.2.2, 3.2.3, ADDED "OPTION" BEFORE EACH DEVICE SELECTION. • PAGE 4, PARAGRAPH 3.6, TABLE IA CHANGED TO TABLE II. PARAGRAPH 3.7, TABLE III CHANGED TO TABLE IV. PARAGRAPH 3.10.3, ADDED "DEVICE OPTIONS 1, 2, AND 3" TO LINE 1. PARAGRAPH 3.11.1 WAS CHANGED FROM "…dosage rate of approximately 20 Rads per second" TO "…dosage rate of less than or equal to 10 Rads per second". • PAGE 5, PARAGRAPHS 4.1 THROUGH 4.4.2 CHANGES WERE DONE TO CLARIFY GROUP SAMPLING. • PAGE 6, PARAGRAPHS 4.4.2.1 THROUGH 4.4.3 CHANGES WERE DONE TO CLARIFY GROUP SAMPLING. PARAGRAPHS 4.6.2 THROUGH 4.6.4 WERE RE-WRITTEN. THESE DATA PROVIDED, AND DATA AVAILABLE. • PAGE 7, PARAGRAPH 4.6.10 NOTE, ADDED FURTHER EXPLANATION OF MINIMUM DELIVERED DATA. • PAGES 8 THROUGH 18, ALL FIGURE TITLES CHANGED TO HAVE DEVICE OPTIONS AND PACKAGE TYPES AT TOP OF PAGE, AND HAVE ALL FIGURES AT BOTTOM OF PAGE. • PAGE 11, MOVED FIGURES TO BETTER FIT ON THE PAGE. • PAGE 14, CERDIP STATIC BURN-IN CHANGED TO REFLECT DIFFERENT BURN-IN VOLTAGES AND BURN-IN CIRCUIT. • PAGE 15, CERDIP DYNAMIC BURN-IN CHANGED TO COMPLETE NEW CIRCUIT. • PAGE 17, FLATPACK, DYNAMIC BURN-IN CHANGED TO COMPLETE NEW CIRCUIT. • PAGE 19, TABLES I, II HAVE CORRESPONDING NOTES ALL ON PAGE 20. • PAGE 21, FIGURE 14 AND FIGURE 15 NOW ON ONE PAGE.	09/20/02
H	• PAGE 10, CHANGED OUTLINE DRAWING PIN 1 NOTCH MOVED TO INSIDE LEAD LOCATION.	05/19/03
J	• PAGE 5, CHANGED INITIAL RATE OF RADS TO 240 RADS/SEC.	03/16/05
K	• PAGE 5, CHANGED IN BOTH PARAGRAPHS 4.2, 4.3 IN CONJUNCTION TO 3.3 CHANGED TO 3.4 AND PARAGRAPH 4.3 CHANGED 3.1.1 TO 3.1 AND 3.2.1 TO 3.1.1 • PAGE 4, PARAGRAPH 3.10.3 ADDED OPTION 3 IS ALLOY 42 FOR FLATPACK.	10/11/07
L	• PAGE 4, PARAGRAPH 3.10.3 CHANGED OPTION 2 TO ALLOY 42 PACKAGE REQUIREMENT. • PAGE 5, PARAGRAPH 3.11.1 CHANGED VERBIAGE.	04/29/08
M	• PAGE 5, PARAGRAPH 4.4.2 CHANGED VERBIAGE. • PAGE 10, FIGURE 3 NOTE 2 ADDED TO LEAD THICKNESS.	05/27/08
N	• PAGE 3, PARAGRAPH 3.2.3, OPTION 3, AMENDED DEVICE NOMENCLATURE FROM RH37CW10 TO RH37CW.	05/23/12
P	• **PAGE 4, PARAGRAPH 3.5, DEVICE HAS BEEN RETESTED AND FOUND TO HAVE AN ESD CLASSIFICATION OF 3A.**	

1.0 SCOPE:

1.1 This specification defines the performance and test requirements for a microcircuit processed to a space level manufacturing flow.

2.0 APPLICABLE DOCUMENTS:

2.1 Government Specifications and Standards: the following documents listed in the Department of Defense Index of Specifications and Standards, of the issue in effect on the date of solicitation, form a part of this specification to the extent specified herein.

SPECIFICATIONS:

MIL-PRF-38535	Integrated Circuits (Microcircuits) Manufacturing, General Specification for
MIL-STD-883	Test Method and Procedures for Microcircuits
MIL-STD-1835	Microcircuits Case Outlines

2.2 Order of Precedence: In the event of a conflict between the documents referenced herein and the contents of this specification, the order of precedence shall be this specification, MIL-PRF-38535 and other referenced specifications.

3.0 REQUIREMENTS:

3.1 General Description: This specification details the requirements for the RH37C, Precision Operational Amplifier, processed to space level manufacturing flow.

3.2 Part Number:

3.2.1 Option 1 – RH37CH (TO5 Metal Can, 8 Lead)

3.2.2 Option 2 – RH37CJ8 (Ceramic Dip, 8 Lead)

3.2.3 Option 3 – RH37CW (Flatpak Glass Sealed, 10 Lead)

3.3 Part Marking Includes:

a. LTC Logo

b. LTC Part Number (See Paragraph 3.2)

c. Date Code

d. Serial Number

e. ESD Identifier per MIL-PRF-38535, Appendix A

3.4 The Absolute Maximum Ratings:

Supply Voltage	±22V
Internal Power Dissipation	500mW
Input Voltage	Equal to Supply Voltage
Output Short-Circuit Duration	Indefinite
Differential Input Current 1/	±25mA
Operating Temperature Range	-55°C to +125°C
Junction Temperature Range	-55°C to +150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 sec)	+300°C

1/ The RH37's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.

3.5 Electrostatic discharge sensitivity, ESDS, shall be Class 3A.

3.6 Electrical Performance Characteristics: The electrical performance characteristics shall be as specified in Table I and **Table II**.

3.7 Electrical Test Requirements: Screening requirements shall be in accordance with 4.1 herein, MIL-STD-883, Method 5004, and as specified in **Table IV** herein.

3.8 Burn-In Requirement:

3.8.1 Option 1 (TO5): Static Burn-In, Figure 7; Dynamic Burn-In, Figure 8

3.8.2 Option 2 (Ceramic Dip): Static Burn-In, Figure 9; Dynamic Burn-In, Figure 10

3.8.3 Option 3 (Flatpack Glass Sealed) : Static Burn-In, Figure 11; Dynamic Burn-In, Figure 12

3.9 Delta Limit Requirement: Delta limit parameters are specified in **Table III** herein, are calculated after each burn-in, and the delta rejects are included in the PDA calculation.

3.10 Design, Construction, and Physical Dimensions: Detail design, construction, physical dimensions, and electrical requirements shall be specified herein.

3.10.1 Mechanical / Packaging Requirements: Case outlines and dimensions are in accordance with Figure 1, Figure 2, and Figure 3.

3.10.2 Terminal Connections: The terminal connections shall be as specified in Figure 4, Figure 5, and Figure 6.

3.10.3 Lead Material and Finish: The lead material and finish for Device Options 1, shall be Kovar and Options 2, 3 is Alloy 42. The lead finishes shall be hot solder dip (Finish letter A) in accordance with MIL-PRF-38535.

3.11 Radiation Hardness Assurance (RHA):

3.11.1 The manufacturer shall perform a lot sample test as an internal process monitor for total dose radiation tolerance. The sample test is performed with MIL-STD-883 TM1019 Condition A as a guideline.

3.11.2 For guaranteed radiation performance to MIL-STD-883, Method 1019, total dose irradiation, the manufacturer will provide certified RAD testing and report through an independent test laboratory when required as a customer purchase order line item.

3.11.3 Total dose bias circuit is specified in Figure 13.

3.12 Wafer Lot Acceptance: Wafer lot acceptance shall be in accordance with MIL-PRF-38535, Appendix A, except for the following: Topside glassivation thickness shall be a minimum of 4KÅ.

3.13 Wafer Lot Acceptance Report: SEM is performed per MIL-STD-883, Method 2018 and copies of SEM photographs shall be supplied with the Wafer Lot Acceptance Report as part of a Space Data Pack when specified as a customer purchase order line item.

4.0 VERIFICATION (QUALITY ASSURANCE PROVISIONS)

4.1 Quality Assurance Provisions: Quality Assurance provisions shall be in accordance with MIL-PRF-38535. Linear Technology is a QML certified company and all Rad Hard candidates are assembled on qualified Class S manufacturing lines.

4.2 Sampling and Inspection: Sampling and Inspection shall be in accordance with MIL-STD-883, Method 5005 with QML allowed and TRB approved deviations in conjunction with paragraphs 3.1.1, 3.2.1, and 3.4 of the test method.

4.3 Screening: Screening requirements shall be in accordance with MIL-STD-883, Method 5004 with QML allowed and TRB approved deviations in conjunction with paragraphs 3.1, 3.1.1, and 3.4 of the test method. Electrical testing shall be as specified in **Table IV** herein.

4.3.1 Analysis of catastrophic (open/short) failures from burn-in will be conducted only when a lot fails the burn-in or re-burn-in PDA requirements.

4.4 Quality Conformance Inspection: Quality conformance inspection shall be in accordance with 4.2 and 4.3 herein and as follows:

4.4.1 Group A Inspection: Group A inspection shall be performed in accordance with 4.1 herein, per MIL-STD-883, Method 5005, and specified in **Table IV** herein.

4.4.2 Group B Inspection: When purchased, a full Group B is performed on an inspection lot. As a minimum, Subgroups 1-4 plus 6 are performed on every assembly lot, and Subgroup B2 (Resistance to Solvents / Mark Permanency) and Subgroup B3 (Solderability) are performed prior to the first shipment from any inspection lot and Attributes provided when a Full Space Data Pack is ordered. Subgroup B5 (Operating Life) is performed on each wafer lot. This subgroup may or may not be from devices built in the same package style as the current inspection lot. Attributes and variables data for this subgroup will be provided upon request at no charge.

4.4.2.1 Group B, Subgroup 2c = 10%

Group B, Subgroup 3 = 10%

Group B, Subgroup 4 = 5%

Group B, Subgroup 5 = *5% (*per wafer or inspection lot whichever is the larger quantity)

Group B, Subgroup 6 = 15%

4.4.2.2 All footnotes pertaining to Table IIa in MIL-STD-883, Method 5005 apply. The quantity (accept number) of all other subgroups are per MIL-STD-883, Method 5005, Table IIa.

4.4.3 Group D Inspection: When purchased, a full Group D is performed on an inspection lot. As a minimum, periodic full Group D sampling is performed on each package family for each assembly location every 26 weeks. A generic Group D Summary is provided when a full Space Data Pack is ordered.

4.4.3.1 Group D, Subgroups 3, 4 and 5 = 15% each (Sample Size Series).

4.4.3.2 All footnotes pertaining to Table IV in MIL-STD-883, Method 5005 apply. The quantity (accept number) or sample number and accept number of all other subgroups are per MIL-STD-883, Method 5005, Table IV.

4.5 Source Inspection:

4.5.1 The manufacturer will coordinate Source Inspection at wafer lot acceptance and pre-seal internal visual.

4.5.2 The procuring activity has the right to perform source inspection at the supplier's facility prior to shipment for each lot of deliverables when specified as a customer purchase order line item. This may include wafer lot acceptance and final data review.

4.6 Deliverable Data: Deliverable data that will ship with devices when a Space Data Pack is ordered:

4.6.1 Lot Serial Number Sheets identifying all devices accepted through final inspection by serial number.

4.6.2 100% attributes (completed lot specific traveler; includes Group A Summary)

4.6.3 Burn-In Variables Data and Deltas (if applicable)

4.6.4 Group B2, B3, and B5 Attributes (Variables data, if performed on lot shipping)

4.6.5 Generic Group D data (4.4.3 herein)

4.6.6 SEM photographs (3.13 herein)

4.6.7 Wafer Lot Acceptance Report (3.13 herein)

4.6.8 X-Ray Negatives and Radiographic Report

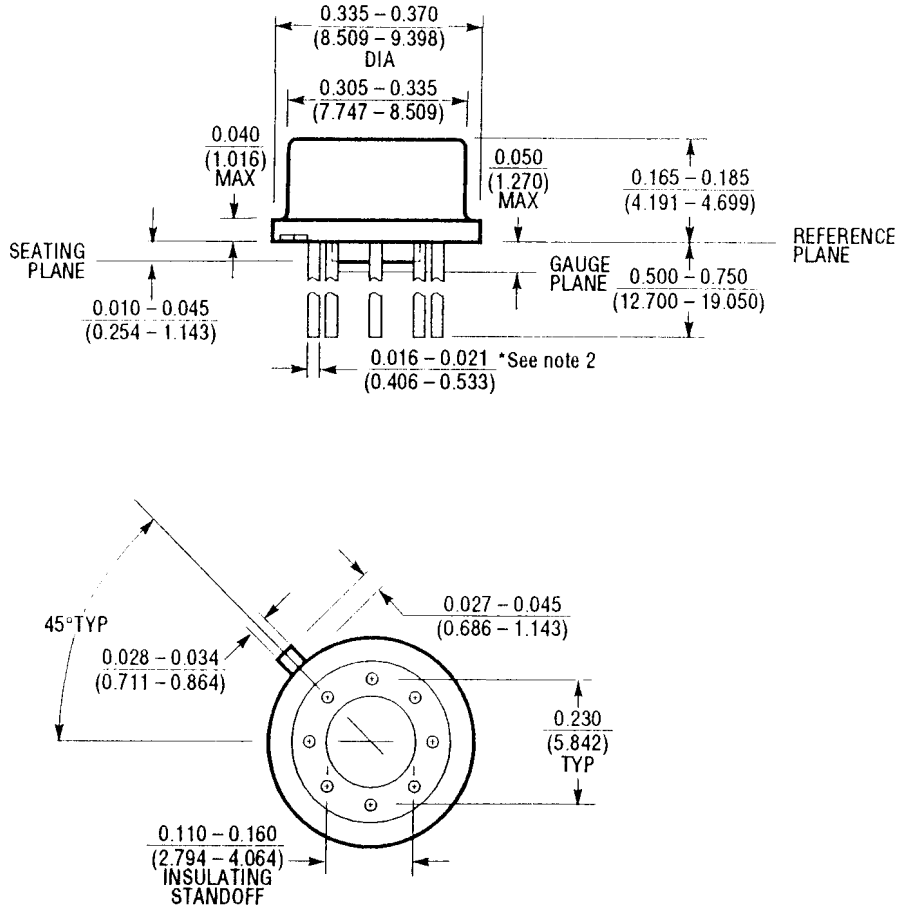
4.6.9 A copy of outside test laboratory radiation report if ordered

4.6.10 Certificate of Conformance certifying that the devices meet all the requirements of this specification and have successfully completed the mandatory tests and inspections herein.

Note: Items 4.6.1 and 4.6.10 will be delivered as a minimum, with each shipment. This is noted on the Purchase Order Review Form as “No Charge Data”.

5.0 Packaging Requirements: Packaging shall be in accordance with Appendix A of MIL-PRF-38535. All devices shall be packaged in conductive material or packaged in anti-static material with an external conductive field shielding barrier.

DEVICE OPTION # 1
(H) TO5 / 8 LEADS CASE OUTLINE



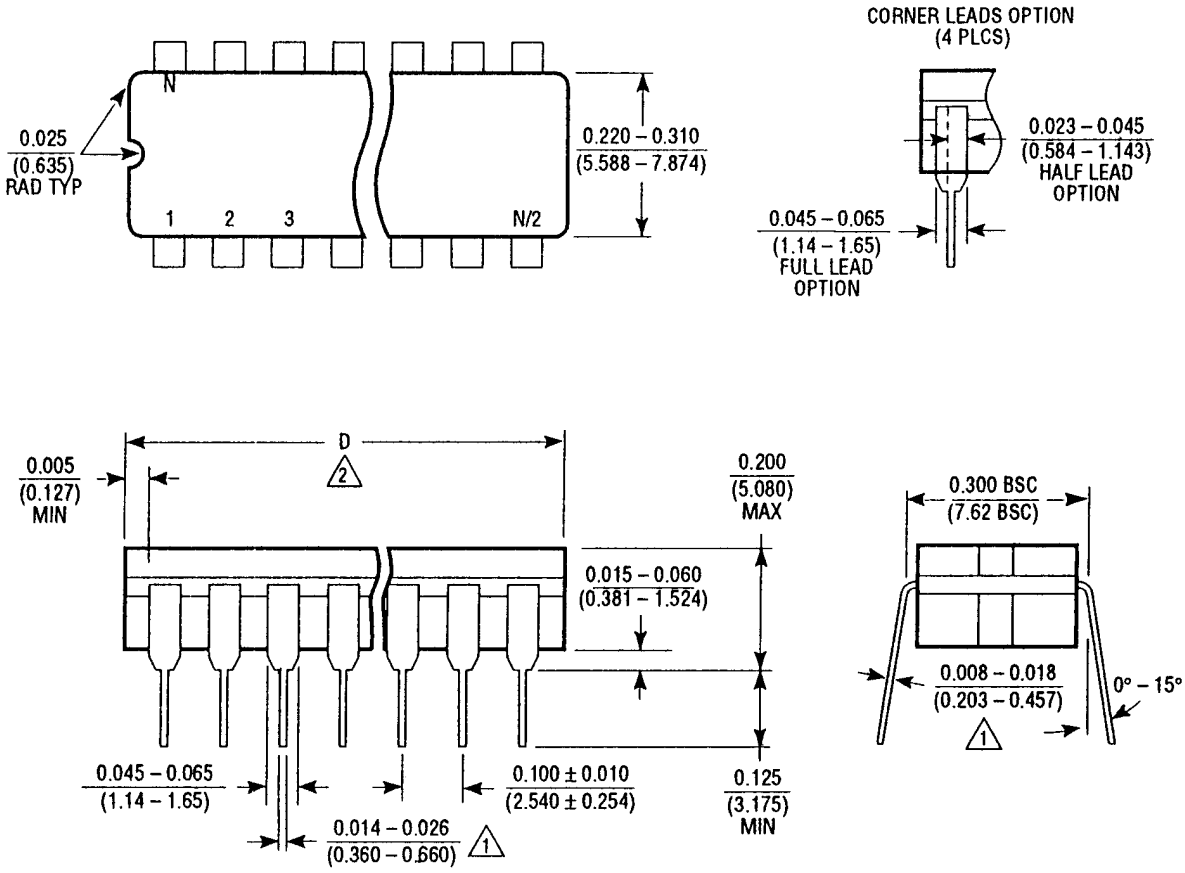
NOTE: 1. LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND SEATING PLANE.
2. FOR SOLDER DIP LEAD FINISH, LEAD DIAMETER IS 0.016 – 0.024 (0.406 – 0.610)

θja = +150°C/W
θjc = +40°C/W

FIGURE 1

DEVICE OPTION # 2

(J8) CERAMIC DIP / 8 LEADS CASE OUTLINE

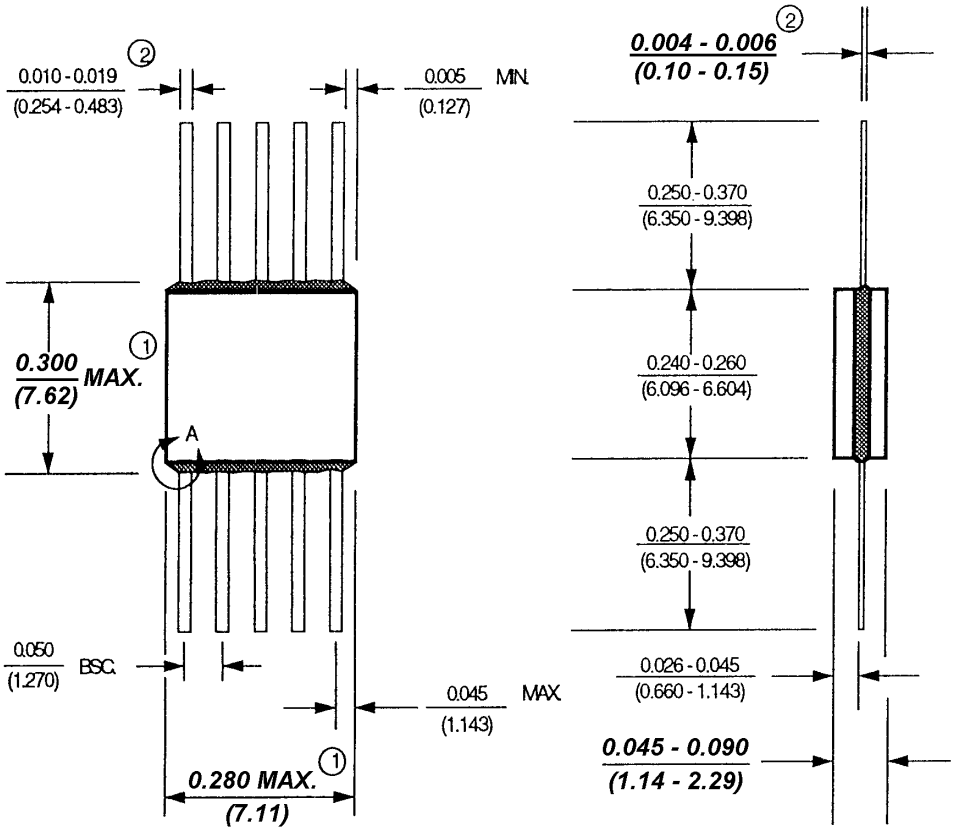


NOTE: 1. LEAD DIMENSIONS APPLY TO SOLDER DIP OR TIN PLATE LEADS.
2. 8 LEAD D MAX = .0405 (10.287)

θ_{ja} = +110°C/W
θ_{jc} = +30°C/W

FIGURE 2

DEVICE OPTION # 3
(W10) GLASS SEALED FLATPACK / 10 LEADS CASE OUTLINE



NOTE: 1. THIS DIMENSION ALLOWS FOR OFF-CENTER LID, MENISCUS AND GLASS OVER RUN.

NOTE: 2. INCREASE DIMENSION BY 0.003 INCH WHEN LEAD FINISH IS APPLIED (SOLDER DIPPED).

θ_{ja} = +170°C/W
θ_{jc} = +40°C/W

FIGURE 3

TERMINAL CONNECTIONS

DEVICE OPTION #1

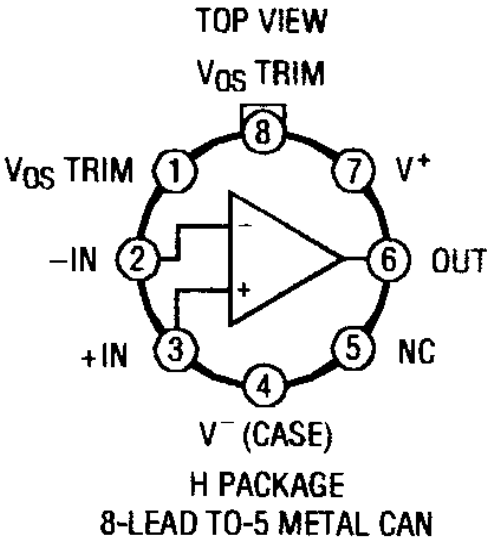


FIGURE 4

DEVICE OPTION #2

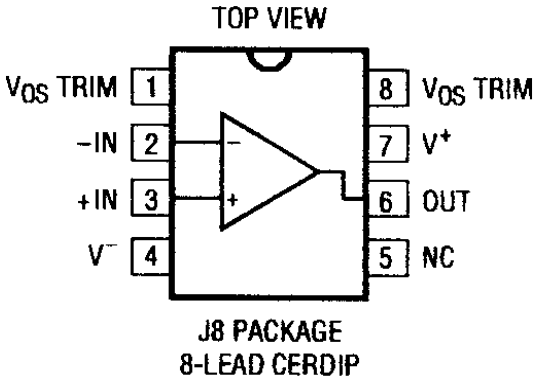


FIGURE 5

DEVICE OPTION #3

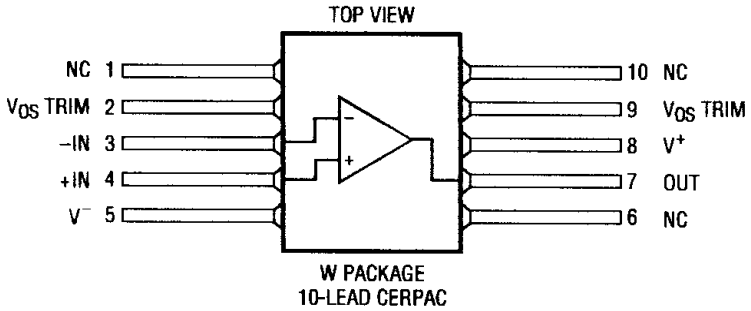
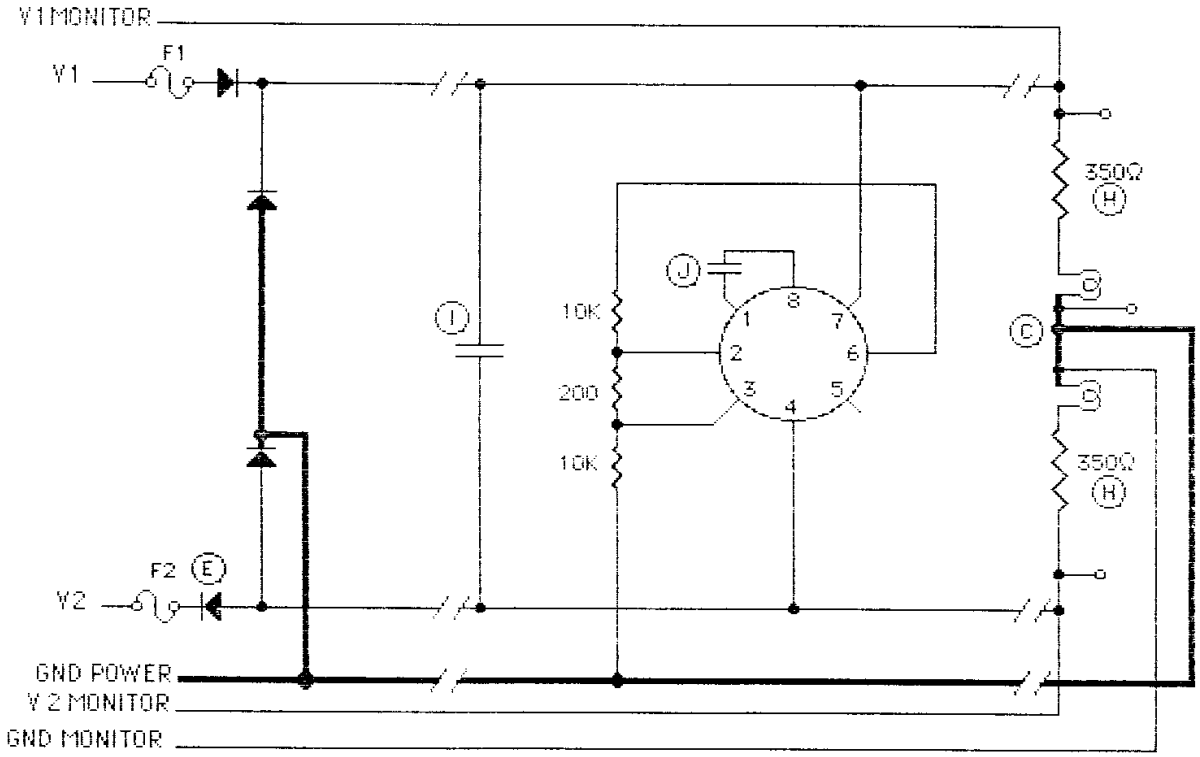


FIGURE 6

STATIC BURN-IN CIRCUIT
OPTION 1, TO5 METAL CAN / 8 LEADS



NOTES:

1. Unless otherwise specified, component tolerances shall be per military specification.
2. Tj maximum = Varies with device being burned in.
3. Ta = 150 °C.
4. Burn-in voltages; V1 = +20V to +22V
   V2 = -20V to -22V

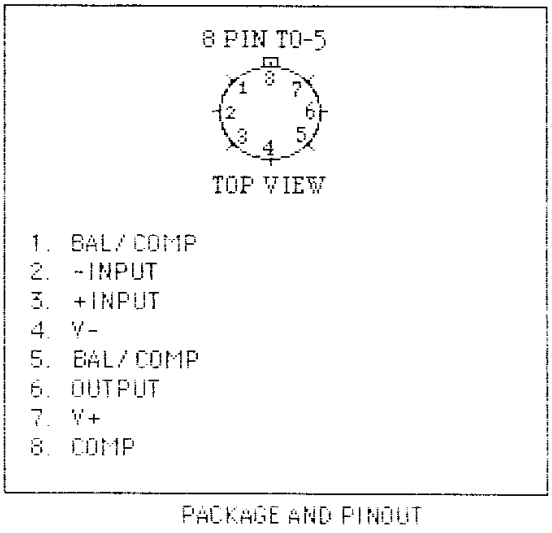
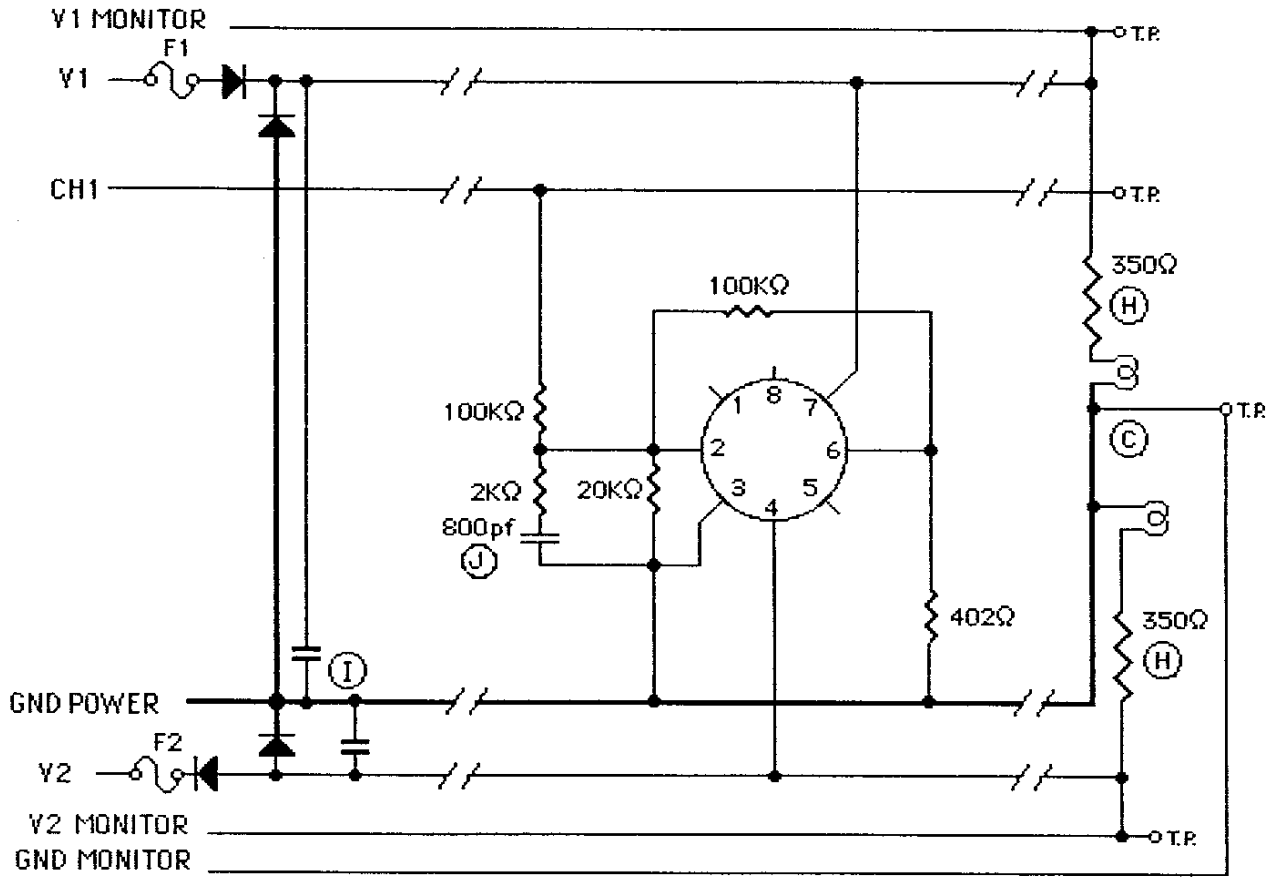
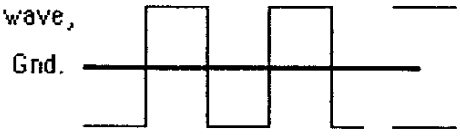


FIGURE 7

DYNAMIC BURN-IN CIRCUIT
OPTION 1, TO5 METAL CAN / 8 LEADS



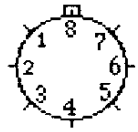
NOTES:
1. Unless otherwise specified, component tolerances shall be per military specification.
2. Tj max= 168°C at 150°C ambient.
3. Burn-in Voltages: V1 = + 18V to + 20V
   V2= - 18V to - 20V
4. CH. 1 = Square wave,



Frequency, 4.5hz(222ms) to 5.5hz(182ms)

1. Offset Trim
2. -IN
3. +IN
4. V-
5. N/C
6. Output
7. V+
8. Offset Trim

8 PIN TO-5

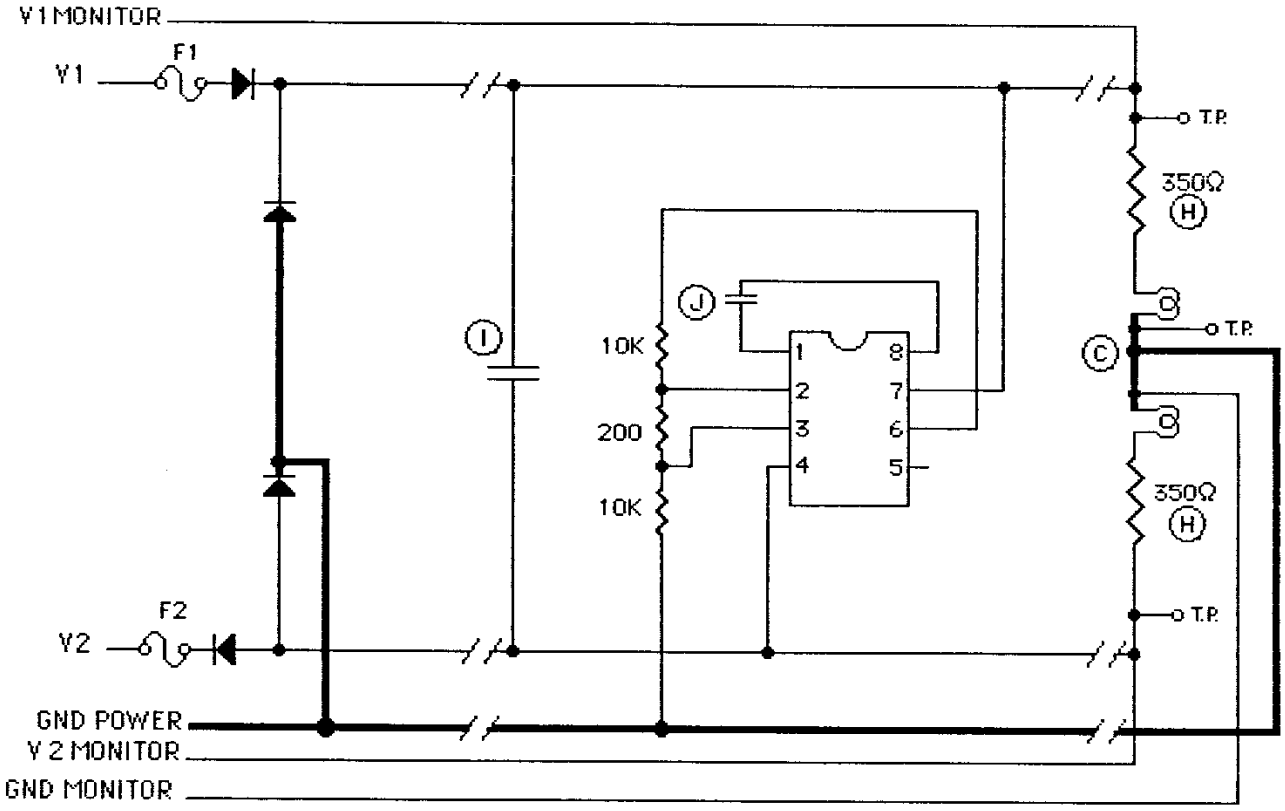


TOP VIEW

PACKAGE

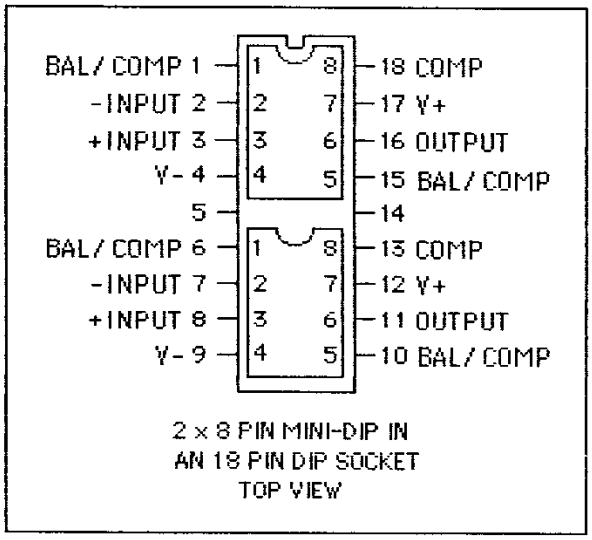
FIGURE 8

STATIC BURN-IN CIRCUIT
OPTION #2, CERDIP / 8 LEADS



NOTES:

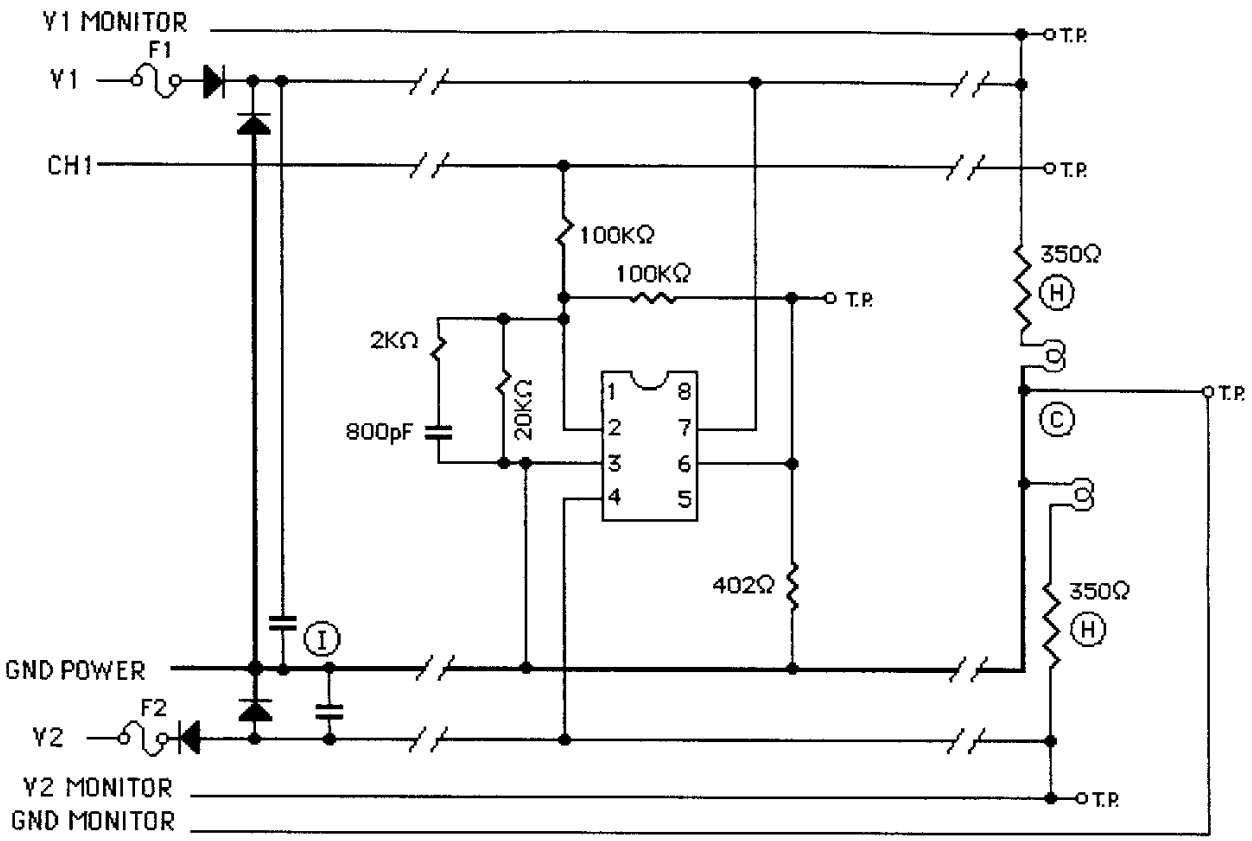
1. Unless otherwise specified, component tolerances shall be per military specification.
2. Tj maximum = Varies with device being burned in.
3. Ta = 150 °C.
4. Burn-in voltages; V1 = +20V to +22V
   V2 = -20V to -22V



PACKAGE AND PINOUT

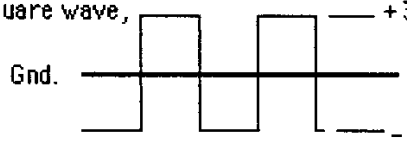
FIGURE 9

DYNAMIC BURN-IN CIRCUIT
OPTION 2, CERDIP / 8 LEADS

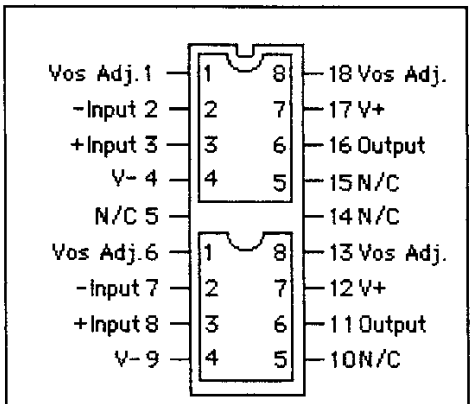


NOTES:

1. Unless otherwise specified, component tolerances shall be per military specification.
2. Tj max = 163° C
3. Ta = 125° C
4. Burn-in Voltages: Y1 = +18V to +19.8V
   Y2 = -18V to -19.8V
5. CH. 1 = Square wave, +3.0V to +3.3V



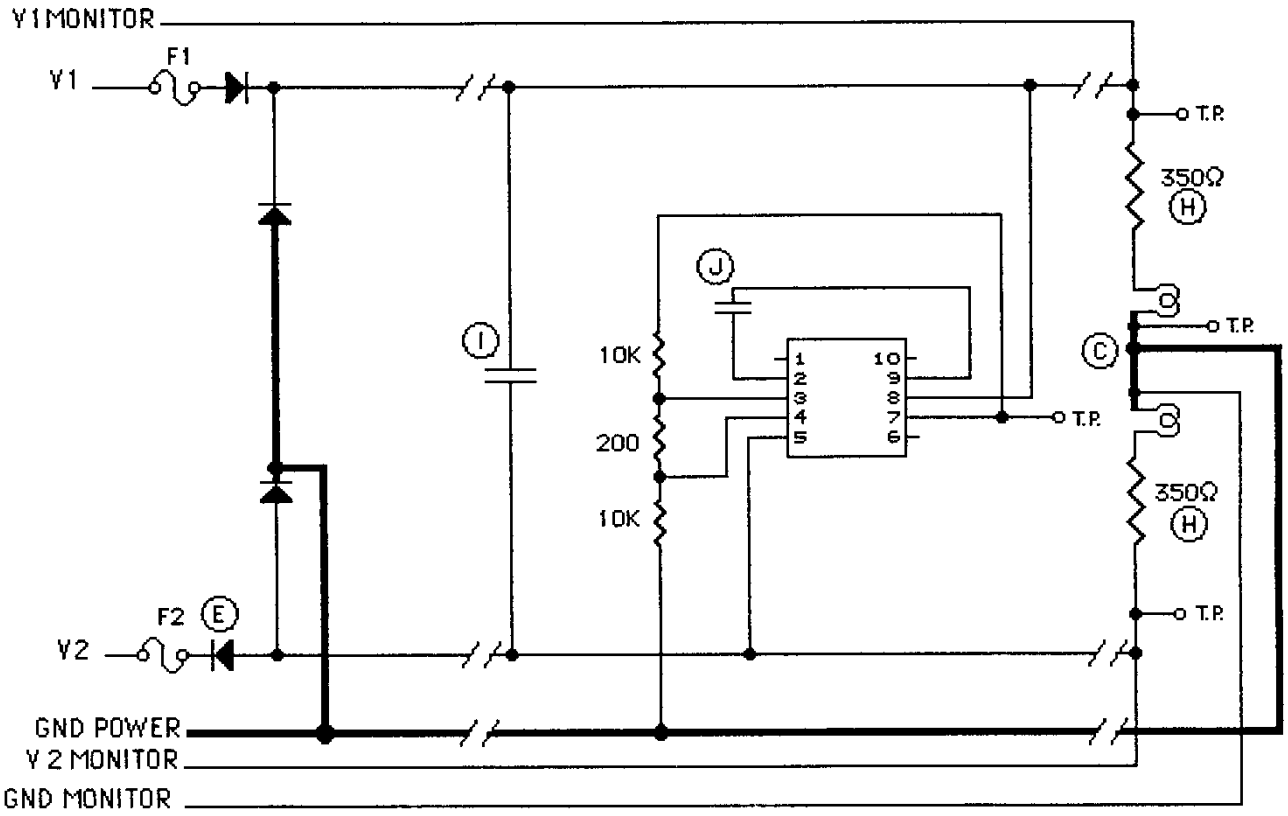
Frequency, 4.5hz(222ms) to 5.5hz(182ms)



PACKAGE

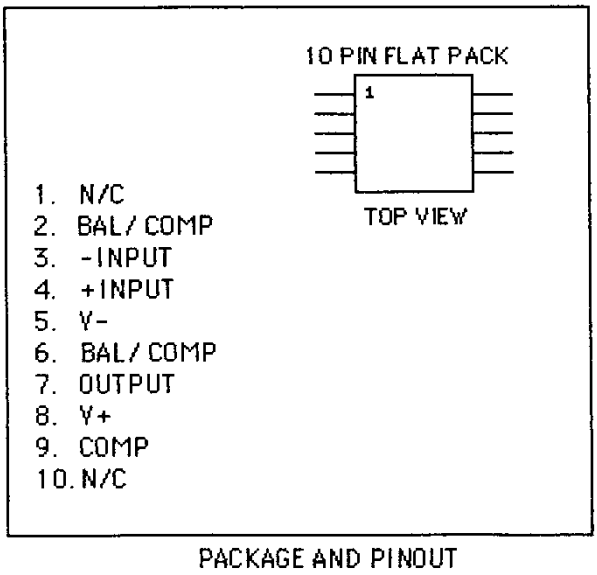
FIGURE 10

STATIC BURN-IN CIRCUIT
OPTION 3, GLASS SEALED FLATPACK / 10 LEAD



NOTES:

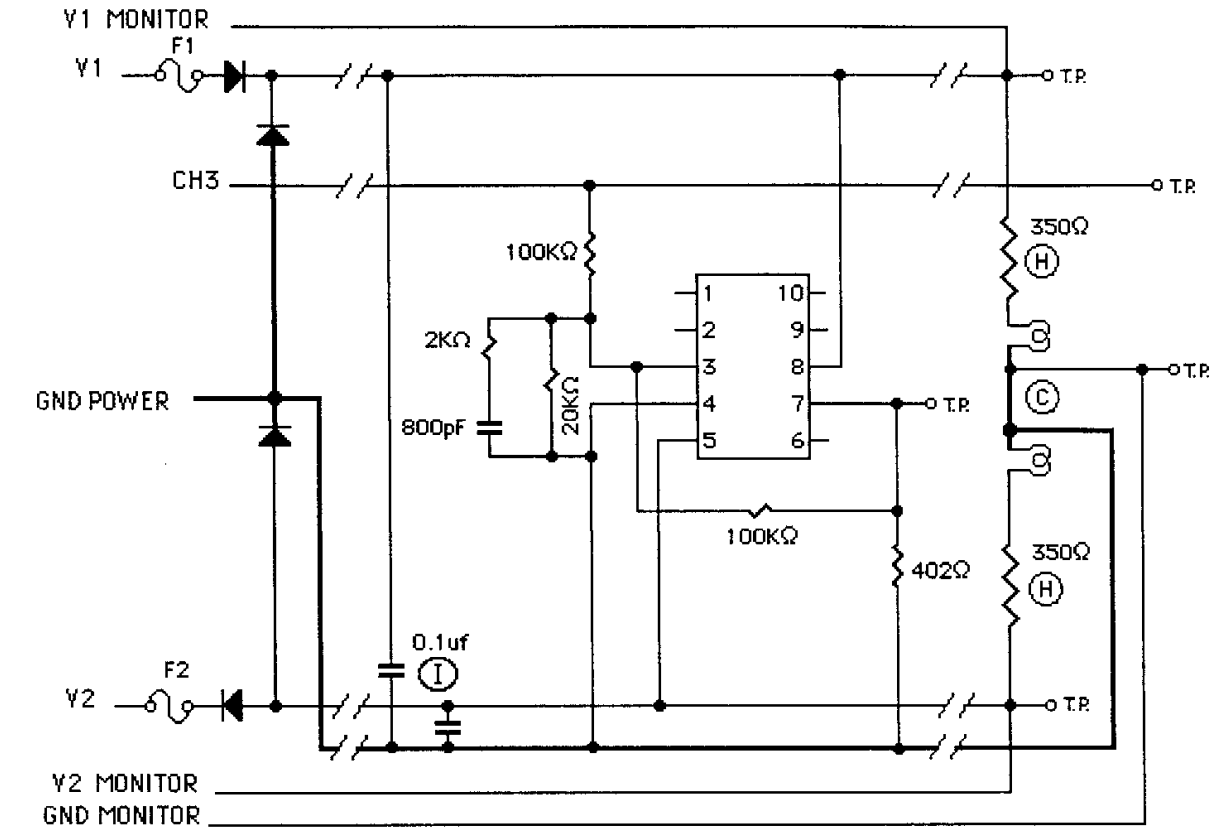
1. Unless otherwise specified, component tolerances shall be per military specification.
2. Tj maximum = Varies with device being burned in.
3. Ta = 150 °C.
4. Burn-in voltages; V1 = +20V to +22V
   V2 = -20V to -22V



PACKAGE AND PINOUT

FIGURE 11

DYNAMIC BURN-IN CIRCUIT
OPTION 3, GLASS SEALED FLATPACK / 10 LEAD



NOTES:

1. Unless otherwise specified, component tolerances shall be per military specification.
2. Tj max = 163° C
3. Ta = 125° C
4. Burn-in Voltages: V1 = +18V to +19.8V
   V2 = -18V to -19.8V
5. CH. 1 = Square wave, +3.0V to +3.3V / Gnd. / -3.0V to -3.3V
   Frequency, 4.5hz(222ms) to 5.5hz(182ms)

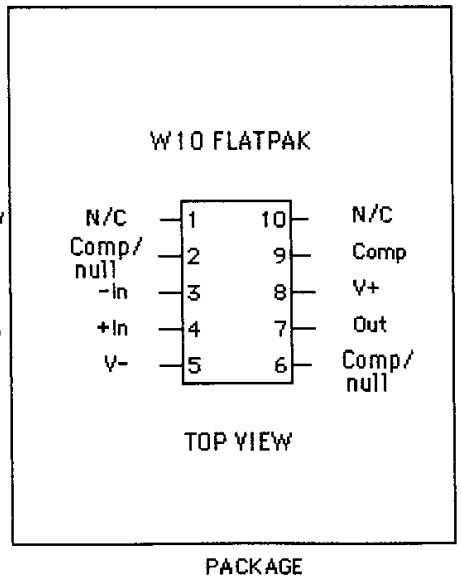


FIGURE 12

TOTAL DOSE BIAS CIRCUIT

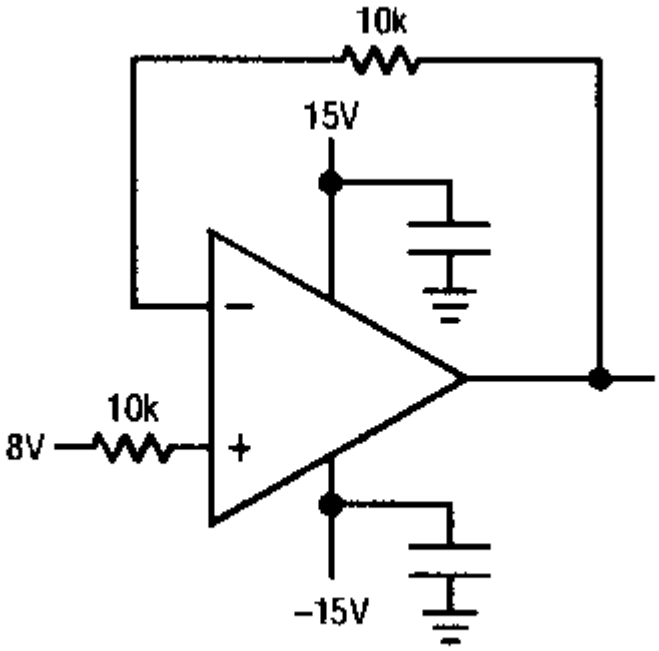


FIGURE 13

TABLE I: ELECTRICAL CHARACTERISTICS (PRE-IRRADIATION) NOTE 9

SYMBOL	PARAMETER	CONDITIONS	NOTES	T_A = 25°C MIN	TYP	MAX	SUB-GROUP	−55°C ≤ T_A ≤ 125°C MIN	TYP	MAX	SUB-GROUP	UNITS
V_{OS}	Input Offset Voltage		1			100	4			300	2, 3	µV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Offset Drift		4, 7							1.8		µV/°C
$\frac{\Delta V_{OS}}{\Delta Time}$	Long-Term Input Offset Voltage Stability		2, 4			2						µV/Month
I_{OS}	Input Offset Current					75	1			135	2, 3	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz	4, 5			0.25						μV_{P-P}
	Input Noise Voltage Density	f_O = 10Hz f_O = 30Hz f_O = 1000Hz	3 4 4			8.0 5.6 4.5						$nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
i_n	Input Noise Current Density	f_O = 1000Hz	4, 6			0.6						$pV/\sqrt{Hz}$
	Input Resistance Common Mode				2							GΩ
	Input Voltage Range		4	±11				±10.2				V
CMRR	Common Mode Rejection Ratio	V_{CM} = ±11V V_{CM} = ±10V		100			1	94			2, 3	dB dB
PSRR	Power Supply Rejection Ratio	V_S = ±4V to ±18V V_S = ±4.5V to ±18V		94			1	86			2, 3	dB dB
A_{VOL}	Large-Signal Voltage Gain	R_L ≥ 2k, V_O = ±10V R_L ≥ 600Ω, V_O = ±1V V_S = ±4V	4	700 200			4	300			5, 6	V/mV V/mV
V_{OUT}	Maximum Output Voltage Swing	R_L = 2k R_L = 600Ω		±11.5 ±10.0			4 4	±10.5			5, 6	V V
SR	Slew Rate	R_L = 2k, A_{VCL} ≥ 5		11			7					V/µs
GBW	Gain-Bandwidth Product	f_O = 10kHz (A_{VCL} ≥ 5) f_O = 1MHz (A_{VCL} ≥ 5)	4	45 40								MHz MHz
Z_O	Open-Loop Output Resistance	V_O = 0, I_O = 0			470							Ω
P_D	Power Dissipation					170	1					mW

See applicable notes on page 20.

TABLE II: ELECTRICAL CHARACTERISTICS (POST-IRRADIATION) NOTE 10

SYMBOL	PARAMETER	CONDITIONS	NOTES	10KRAD(Si) MIN	10KRAD(Si) MAX	20KRAD(Si) MIN	20KRAD(Si) MAX	50KRAD(Si) MIN	50KRAD(Si) MAX	100KRAD(Si) MIN	100KRAD(Si) MAX	200KRAD(Si) MIN	200KRAD(Si) MAX	UNITS
V_{OS}	Input Offset Voltage		1		100		130		180		280		400	µV
I_{OS}	Input Offset Current				75		75		90		120		180	nA
I_B	Input Bias Current				±80		±80		±125		±200		±400	nA
	Input Resistance Common Mode			2 (Typ)		2 (Typ)		2 (Typ)		2 (Typ)		2 (Typ)		GΩ
	Input Voltage Range		4	±11		±11		±11		±11		±11		V
CMRR	Common Mode Rejection Ratio	V_{CM} = ±11V		100		100		97		94		90		dB
PSRR	Power Supply Rejection Ratio	V_S = ±4V to ±18V		94		94		92		90		86		dB
A_{VOL}	Large-Signal Voltage Gain	$R_L \geq 2k$, V_O = ±10V		700		700		700		700		400		V/mV
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 10k$ $R_L \geq 600\Omega$		±11.5 ±10.0		±11.5 ±10.0		±11.5 ±10.0		±11.5 ±10.0		±11.5 ±10.0		V V
SR	Slew Rate	$R_L \geq 2k$		1.7		1.7		1.7		1.5		1		V/µs
Z_O	Open-Loop Output Resistance	V_O = 0, I_O = 0		70 (Typ)		70 (Typ)		70 (Typ)		70 (Typ)		70 (Typ)		Ω
P_D	Power Dissipation				170		170		170		170		170	mW

Note 1: Input offset voltage measurements are performed by automatic test equipment approximately 0.5 seconds after application of power.

Note 2: Long-term input offset voltage stability refers to the average trend line of offset voltage vs time over the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically 2.5µV. Refer to the typical performance curves.

Note 3: Sample tested to an LTPD of 15 on every lot. Contact factory for 100% testing of 10Hz voltage density noise.

Note 4: Parameter is guaranteed by design, characterization, or correlation to other tested parameters.

Note 5: See test circuit and frequency response curve for 0.1Hz to 10Hz tester on OP-27/OP-37 data sheet.

Note 6: See test circuit for current noise measurement on OP-27/OP-37 data sheet.

Note 7: The average input offset drift performance is within the specifications unnulled or when nulled with a pot having a range 8kΩ to 20kΩ.

Note 8: The RH37C's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.

Note 9: V_S = ±15V, V_{CM} = 0V unless otherwise noted.

Note 10: T_A = 25°C, V_S = ±15V, V_{CM} = 0V, unless otherwise noted.

0.1Hz TO 10Hz NOISE TEST CIRCUIT

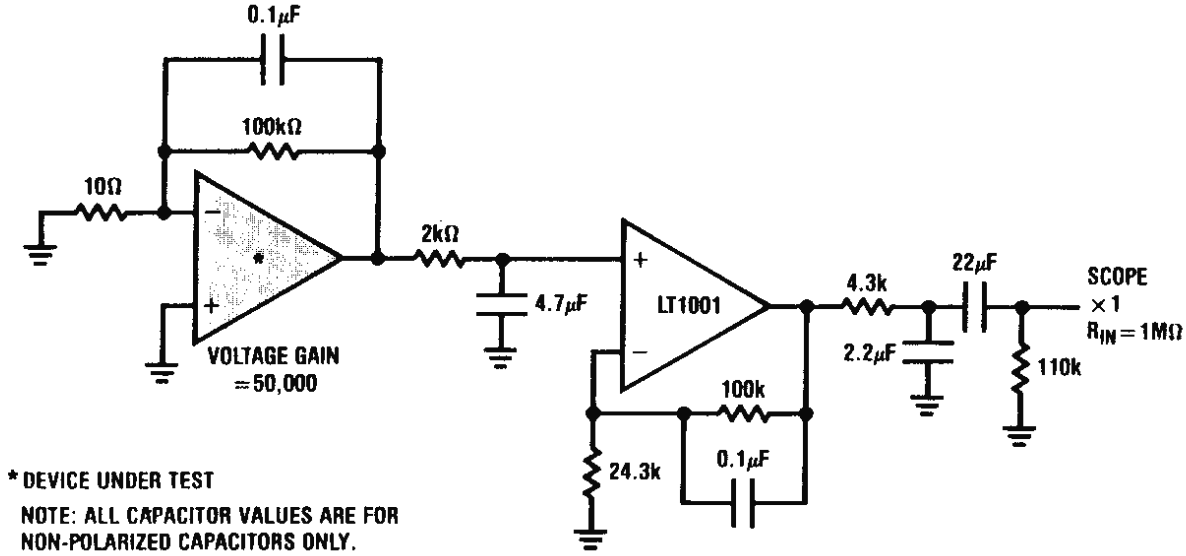


FIGURE 14

CURRENT NOISE MEASUREMENT

Current Noise is measured and calculated by the following formula:

$$i_n = \frac{[e^2_{no} - (130nV)^2]^{1/2}}{1M\Omega \times 100}$$

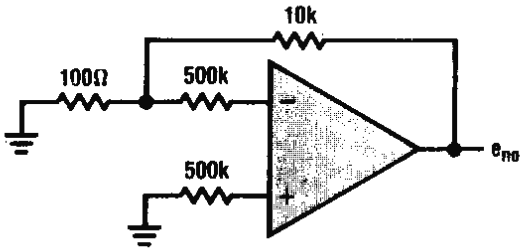


FIGURE 15

TABLE III: POST BURN-IN ENDPOINTS AND DELTA LIMIT REQUIREMENTS

T_A = 25°C

	ENDPOINT LIMIT		DELTA		
PARAMETER	MIN	MAX	MIN	MAX	UNITS
V_{OS}	-100	100	-75	75	μV
$+I_{IB}$	-80	80	-10	10	nA
$-I_{IB}$	-80	80	-10	10	nA

TABLE 1V: ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUP
FINAL ELECTRICAL TEST REQUIREMENTS (METHOD 5004)	1*, 2, 3, 4, 5, 6, 7
GROUP A TEST REQUIREMENTS (METHOD 5005)	1, 2, 3, 4, 5, 6, 7
GROUP B AND D FOR CLASS S ENDPOINT ELECTRICAL PARAMETERS (METHOD 5005)	1, 2, 3

*PDA APPLIES TO SUBGROUP 1.

PDA TEST NOTE: The PDA is specified as 5% based on failures from Group A, Subgroup 1, tests after cool down as the final electrical test in accordance with method 5004 of MIL-STD-883. The verified failures of Group A, Subgroup 1 and delta rejects after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent for the lot.