

REVISION RECORD		
REV	DESCRIPTION	DATE
0	INITIAL RELEASE	06/12/96
A	<ul style="list-style-type: none"> PAGE 2, ADDED PARAGRAPHS 3.2.1, 3.2.2, AND 3.2.3. PARAGRAPH 3.3.b: ADDED “(SEE PARAGRAPH 3.2)”. PAGE 3, ADDED PARAGRAPHS 3.8.1, 3.8.2, AND 3.8.3. PAGE 4, PARAGRAPH 3.12: WAFER LOT ACCEPTANCE, REDEFINED. PARAGRAPH 4.4.2, GROUP B INSPECTION, REDEFINED. PAGE 5, PARAGRAPH 4.4.3, GROUP D INSPECTION, REDEFINED. PARAGRAPH 4.5 SOURCE INSPECTION WAS REDEFINED. PAGE 8, FIGURE 3, CHANGED FROM “CERPAK” TO “FLATPACK, GLASS SEAL”. PAGE 9, FIGURE 6, CHANGED FROM “CERPAK” TO “FLATPACK, GLASS SEAL”. 	11/25/97
B	<ul style="list-style-type: none"> PAGE 4, AMENDED PARAGRAPHS 4.1 AND 4.1.1 TAKING EXCEPTION TO ANALYSIS OF CATASTROPHIC FAILURES. 	02/12/98
C	<ul style="list-style-type: none"> PAGE 6, ADDED θ_{ja} OF 150°C/W AND ADDED θ_{jc} OF 40°C/W TO FIGURE 1, TO5 CASE OUTLINE. PAGE 7, ADDED θ_{ja} OF 110°C/W AND ADDED θ_{jc} OF 30°C/W TO FIGURE 2, CERAMIC DIP CASE OUTLINE. PAGE 8, ADDED θ_{ja} OF 170°C/W AND ADDED θ_{jc} OF 40°C/W TO FIGURE 3, GLASS SEAL FLATPACK. 	11/17/99
D	<ul style="list-style-type: none"> PAGE 3, PARAGRAPHS 3.2.1, 3.2.2, 3.2.3 HAD FIGURES 1, 2, AND 3 REMOVED. PAGE 4, PARAGRAPH 3.7, CHANGED VERBIAGE FROM “SPECIFIED IN TABLE III” TO “AND AS SPECIFIED IN TABLE III HEREIN”, LINE 2. PARAGRAPH 3.9, ADDED “HEREIN” AFTER “TABLE II”, LINE 2. PAGE 5, PARAGRAPH 4.3, ADDED “HEREIN” AFTER “TABLE III”, LINE 2. PARAGRAPH 4.4.1, ADDED “HEREIN” AFTER “TABLE III”, LINE 2. PARAGRAPH 4.4.2.2, CHANGED VERBIAGE IN LINE 1 FROM “ALL FOOTNOTES OF TABLE IIA OF MIL-STD-883” TO “ALL FOOTNOTES PERTAINING TO TABLE IIA IN MIL-STD-883”. PAGE 6, PARAGRAPH 4.4.3.2, CHANGED VERBIAGE IN LINE 1 FROM “ALL FOOTNOTES OF TABLE IV OF MIL-STD-883” TO “ALL FOOTNOTES PERTAINING TO TABLE IV IN MIL-STD-883”. 	11/19/99
E	<ul style="list-style-type: none"> PAGE 9, CHANGED THETA JA TO $\theta_{JA}=170^\circ\text{C/W}$ AND THETA JC TO $\theta_{JC}=40^\circ\text{C/W}$ FROM $\theta_{JA}=225^\circ\text{C/W}$ AND $\theta_{JC}=18^\circ\text{C/W}$ PER PACKAGE ENGINEER. 	09/05/00

REVISION RECORD AND DESCRIPTION CONTINUED ON NEXT PAGE.

CAUTION: ELECTROSTATIC DISCHARGE SENSITIVE PART

REVISION	PAGE NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
INDEX	REVISION	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N
REVISION	PAGE NO.	18	19															
INDEX	REVISION	N	N															
		ORIG								LINEAR TECHNOLOGY CORPORATION MILPITAS, CALIFORNIA TITLE: MICROCIRCUIT, LINEAR, RH108A, OPERATIONAL AMPLIFIER								
		DSGN																
		ENGR																
		MFG																
		CM																
		QA																
		PROG									64155	05-08-5022		N				
APPLICATION	FUNCT	SIGNOFFS		DATE		CONTRACT:												

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REVISION RECORD		
REV	DESCRIPTION	DATE
F	<ul style="list-style-type: none"> • PAGE 3: PARAGRAPH 3.2.1 ADDED "OPTION 1", PARAGRAPH 3.2.2, ADDED "OPTION 2", PARAGRAPH 3.2.3, ADDED "OPTION 3". • PAGE 4: PARAGRAPH 3.6, TABLE IA CHANGED TO TABLE II. PARAGRAPH 3.7, TABLE III CHANGED TO TABLE IV. PARAGRAPH 3.9, TABLE II CHANGED TO TABLE III. PARAGRAPH 3.10.3, ADDED "DEVICE OPTIONS 1, 2, AND 3" TO LINE 1. PARAGRAPH 3.11.1 WAS CHANGED FROM "...dosage rate of approximately 20 Rads per second" TO "...dosage rate of less than or equal to 10 Rads per second". • PAGE 5: PARAGRAPHS 4.1 THROUGH 4.4.2.1 CHANGES WERE DONE TO CLARIFY GROUP SAMPLING. • PAGE 6: PARAGRAPH 4.4.3 CHANGE WAS DONE TO CLARIFY GROUP SAMPLING. PARAGRAPHS 4.6.2 THROUGH 4.6.4 WERE RE-WRITTEN. THESE DATA PROVIDED, AND DATA AVAILABLE. PARAGRAPH 4.6.10 NOTE, ADDED FURTHER EXPLANATION OF MINIMUM DELIVERED DATA. • PAGES 7 THROUGH 17, ALL FIGURE TITLES CHANGED TO HAVE DEVICE OPTIONS AND PACKAGE TYPES AT TOP OF PAGE, AND HAVE ALL FIGURES AT BOTTOM OF PAGE. • PAGE 8: CASE OUTLINE REVISED. LEAD DIMENSION CHANGED FROM .068 TO 0.065. • PAGE 9: CASE OUTLINE UPDATED TO MEET MIL-STD-1835 GUIDELINES. • PAGE 10, MOVED FIGURES TO BETTER FIT THE PAGE. • PAGE 18, TABLE I AND TABLE II HAVE BEEN PUT ON 1 PAGE. NOTES FOR TABLES I AND II HAVE CHANGED FROM ALPHA CHARACTERS TO NUMBERS. • SPECIFICATION IS NOW ONLY 19 PAGES. 	04/08/03
G	<ul style="list-style-type: none"> • PAGE 9: CASE OUTLINE DRAWING CHANGED PIN 1 NOTCH MOVED TO INSIDE LEAD LOCATION. 	05/19/03
H	<ul style="list-style-type: none"> • PAGE 18: CHANGED INPUT OFFSET CURRENT IN TABLE 1A FROM 0.2nA TO 0.3nA PER PRODUCT ENGINEER. 	07/16/04
J	<ul style="list-style-type: none"> • PAGE 4: CHANGED INITIAL RATE OF RADS TO 240 RADS/SEC. 	03/16/05
K	<ul style="list-style-type: none"> • PAGE 5, CHANGED IN BOTH PARAGRAPHS 4.2, 4.3 IN CONJUNCTION TO 3.3 CHANGED TO 3.4 AND PARAGRAPH 4.3 CHANGED 3.1.1 TO 3.1 AND 3.2.1 TO 3.1.1 • PAGE 4, PARAGRAPH 3.10.3 ADDED OPTION 3 IS ALLOY 42 FOR FLATPACK. 	03/07/08
L	<ul style="list-style-type: none"> • PAGE 4, PARAGRAPH 3.10.3 CHANGED OPTION 2 TO ALLOY 42 PACKAGE REQUIREMENT. PARAGRAPH 3.11.1 CHANGED VERBIAGE. 	04/29/08
M	<ul style="list-style-type: none"> • PAGE 5, PARAGRAPH 4.4.2 CHANGED VERBIGE. • PAGE 9, FIGURE 3 NOTE 2 ADDED TO LEAD THICKNESS. 	06/09/08
N	<ul style="list-style-type: none"> • PAGE 18, TABLE II: NOTE 4 REVISED AND ADDED TO POWER SUPPLY REJECTION RATIO. 	01/31/11

1.0 SCOPE:

- 1.1 This specification defines the performance and test requirements for a microcircuit processed to a space level manufacturing flow.

2.0 APPLICABLE DOCUMENTS:

- 2.1 Government Specifications and Standards: the following documents listed in the Department of Defense Index of Specifications and Standards, of the issue in effect on the date of solicitation, form a part of this specification to the extent specified herein.

SPECIFICATIONS:

MIL-PRF-38535 Integrated Circuits (Microcircuits) Manufacturing, General Specification for

MIL-STD-883 Test Method and Procedures for Microcircuits

MIL-STD-1835 Microcircuits Case Outlines

- 2.2 Order of Precedence: In the event of a conflict between the documents referenced herein and the contents of this specification, the order of precedence shall be this specification, MIL-PRF-38535 and other referenced specifications.

3.0 REQUIREMENTS:

- 3.1 General Description: This specification details the requirements for the RH108A Operational Amplifier, processed to space level manufacturing flow.

3.2 Part Number:

3.2.1 Option 1 – RH108AH (TO5 Metal Can, 8 Leads)

3.2.2 Option 2 – RH108AJ8 (Ceramic Dip, 8 Leads)

3.2.3 Option 3 – RH108AW (Glass Sealed Flatpack, 10 Leads)

3.3 Part Marking Includes:

- a. LTC Logo
- b. LTC Part Number (See Paragraph 3.2)
- c. Date Code
- d. Serial Number
- e. ESD Identifier per MIL-PRF-38535, Appendix A

3.4 The Absolute Maximum Ratings:

Supply Voltage	±20V
Differential Input Voltage <u>1/</u>	±10V
Input Voltage <u>2/</u>	±15V
Output Short Circuit Duration	Indefinite
Operating Temperature Range	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 sec)	+300°C

1/ Differential input voltages greater than 1V will cause excessive current to flow through the input diodes unless limiting resistance is used.

2/ For supply voltages less than ±15V, the maximum input voltage is equal to the supply voltage.

3.5 Electrostatic discharge sensitivity, ESDS, shall be Class 1.

3.6 Electrical Performance Characteristics: The electrical performance characteristics shall be as specified in Table I and **Table II**.

3.7 Electrical Test Requirements: Screening requirements shall be in accordance with 4.1 herein, MIL-STD-883, Method 5004, and as specified in **Table IV** herein.

3.8 Burn-In Requirement:

3.8.1 Option 1 (TO5): Static Burn-In, Figure 7; Dynamic Burn-In, Figure 8

3.8.2 Option 2 (Ceramic Dip): Static Burn-In, Figure 9; Dynamic Burn-In, Figure 10

3.8.3 Option 3 (Glass Sealed Flatpack) : Static Burn-In, Figure 11; Dynamic Burn-In, Figure 12

3.9 Delta Limit Requirement: Delta limit parameters are specified in **Table III** herein, are calculated after each burn-in, and the delta rejects are included in the PDA calculation.

3.10 Design, Construction, and Physical Dimensions: Detail design, construction, physical dimensions, and electrical requirements shall be specified herein.

3.10.1 Mechanical / Packaging Requirements: Case outlines and dimensions are in accordance with Figure 1, Figure 2, and Figure 3.

3.10.2 Terminal Connections: The terminal connections shall be as specified in Figure 4, Figure 5, and Figure 6.

3.10.3 Lead Material and Finish: The lead material and finish for Device Options 1, shall be Kovar and options 2, 3 are Alloy 42. The lead finishes shall be hot solder dip (Finish letter A) in accordance with MIL-PRF-38535.

3.11 Radiation Hardness Assurance (RHA):

3.11.1 The manufacturer shall perform a lot sample test as an internal process monitor for total dose radiation tolerance. The sample test is performed with MIL-STD-883 TM1019 Condition A as a guideline.

3.11.2 For guaranteed radiation performance to MIL-STD-883, Method 1019, total dose irradiation, the manufacturer will provide certified RAD testing and report through an independent test laboratory when required as a customer purchase order line item.

3.11.3 Total dose bias circuit is specified in Figure 13.

3.12 Wafer Lot Acceptance: Wafer lot acceptance shall be in accordance with MIL-PRF-38535, Appendix A, except for the following: Topside glassivation thickness shall be a minimum of 4KÅ.

3.13 Wafer Lot Acceptance Report: SEM is performed per MIL-STD-883, Method 2018 and copies of SEM photographs shall be supplied with the Wafer Lot Acceptance Report as part of a Space Data Pack when specified as a customer purchase order line item.

4.0 VERIFICATION (QUALITY ASSURANCE PROVISIONS)

4.1 Quality Assurance Provisions: Quality Assurance provisions shall be in accordance with MIL-PRF-38535. Linear Technology is a QML certified company and all Rad Hard candidates are assembled on qualified Class S manufacturing lines.

4.2 Sampling and Inspection: Sampling and Inspection shall be in accordance with MIL-STD-883, Method 5005 with QML allowed and TRB approved deviations in conjunction with paragraphs 3.1.1, 3.2.1, and 3.4 of the test method.

4.3 Screening: Screening requirements shall be in accordance with MIL-STD-883, Method 5004 with QML allowed and TRB approved deviations in conjunction with paragraphs 3.1, 3.1.1 and 3.4 of the test method. Electrical testing shall be as specified in Table IV herein.

4.3.1 Analysis of catastrophic (open/short) failures from burn-in will be conducted only when a lot fails the burn-in or re-burn-in PDA requirements.

4.4 Quality Conformance Inspection: Quality conformance inspection shall be in accordance with 4.2 and 4.3 herein and as follows:

4.4.1 Group A Inspection: Group A inspection shall be performed in accordance with 4.1 herein, per MIL-STD-883, Method 5005, and specified in Table IV herein.

4.4.2 Group B Inspection: When purchased, a full Group B is performed on an inspection lot. As a minimum, Subgroups 1-4 plus 6 are performed on every assembly lot, and Subgroup B2 (Resistance to Solvents / Mark Permanency) and Subgroup B3 (Solderability) are performed prior to the first shipment from any inspection lot and Attributes provided when a Full Space Data Pack is ordered. Subgroup B5 (Operating Life) is performed on each wafer lot. This subgroup may or may not be from devices built in the same package style as the current inspection lot. Attributes and variables data for this subgroup will be provided upon request at no charge.

4.4.2.1 Group B, Subgroup 2c = 10%

Group B, Subgroup 3 = 10%

Group B, Subgroup 4 = 5%

Group B, Subgroup 5 = *5%
(*per wafer or inspection lot
whichever is the larger quantity)

Group B, Subgroup 6 = 15%

4.4.2.2 All footnotes pertaining to Table IIa in MIL-STD-883, Method 5005 apply. The quantity (accept number) of all other subgroups are per MIL-STD-883, Method 5005, Table IIa.

4.4.3 Group D Inspection: When purchased, a full Group D is performed on an inspection lot. As a minimum, periodic full Group D sampling is performed on each package family for each assembly location every 26 weeks. A generic Group D Summary is provided when a full Space Data Pack is ordered.

4.4.3.1 Group D, Subgroups 3, 4 and 5 = 15% each (Sample Size Series).

4.4.3.2 All footnotes pertaining to Table IV in MIL-STD-883, Method 5005 apply. The quantity (accept number) or sample number and accept number of all other subgroups are per MIL-STD-883, Method 5005, Table IV.

4.5 Source Inspection:

4.5.1 The manufacturer will coordinate Source Inspection at wafer lot acceptance and pre-seal internal visual.

4.5.2 The procuring activity has the right to perform source inspection at the supplier's facility prior to shipment for each lot of deliverables when specified as a customer purchase order line item. This may include wafer lot acceptance and final data review.

4.6 Deliverable Data: Deliverable data that will ship with devices when a Space Data Pack is ordered:

4.6.1 Lot Serial Number Sheets identifying all devices accepted through final inspection by serial number.

4.6.2 100% attributes (completed lot specific traveler; includes Group A Summary)

4.6.3 Burn-In Variables Data and Deltas (if applicable)

4.6.4 Group B2, B3, and B5 Attributes (Variables data, if performed on lot shipping)

4.6.5 Generic Group D data (4.4.3 herein)

4.6.6 SEM photographs (3.13 herein)

4.6.7 Wafer Lot Acceptance Report (3.13 herein)

4.6.8 X-Ray Negatives and Radiographic Report

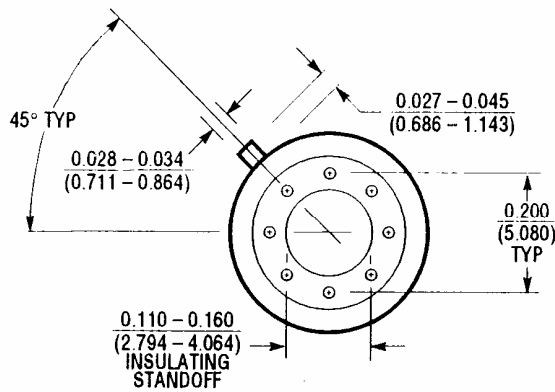
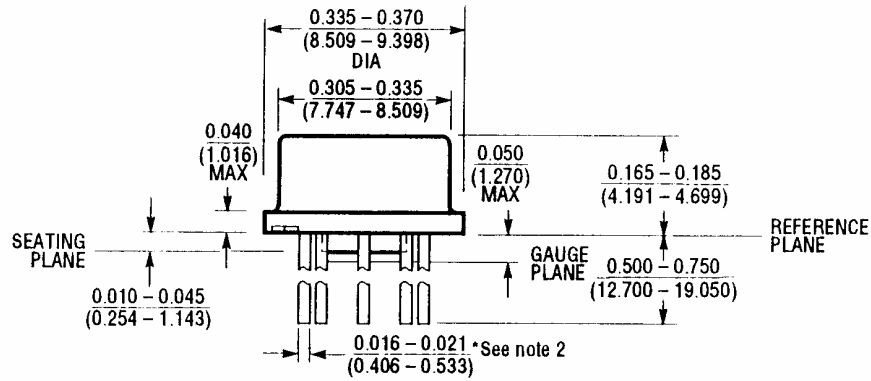
4.6.9 A copy of outside test laboratory radiation report if ordered

4.6.10 Certificate of Conformance certifying that the devices meet all the requirements of this specification and have successfully completed the mandatory tests and inspections herein.

Note: Items 4.6.1 and 4.6.10 will be delivered as a minimum, with each shipment. This is noted on the Purchase Order Review Form as "No Charge Data".

5.0 Packaging Requirements: Packaging shall be in accordance with Appendix A of MIL-PRF-38535. All devices shall be packaged in conductive material or packaged in anti-static material with an external conductive field shielding barrier.

DEVICE OPTION # 1
(H) TO5 / 8 LEADS CASE OUTLINE

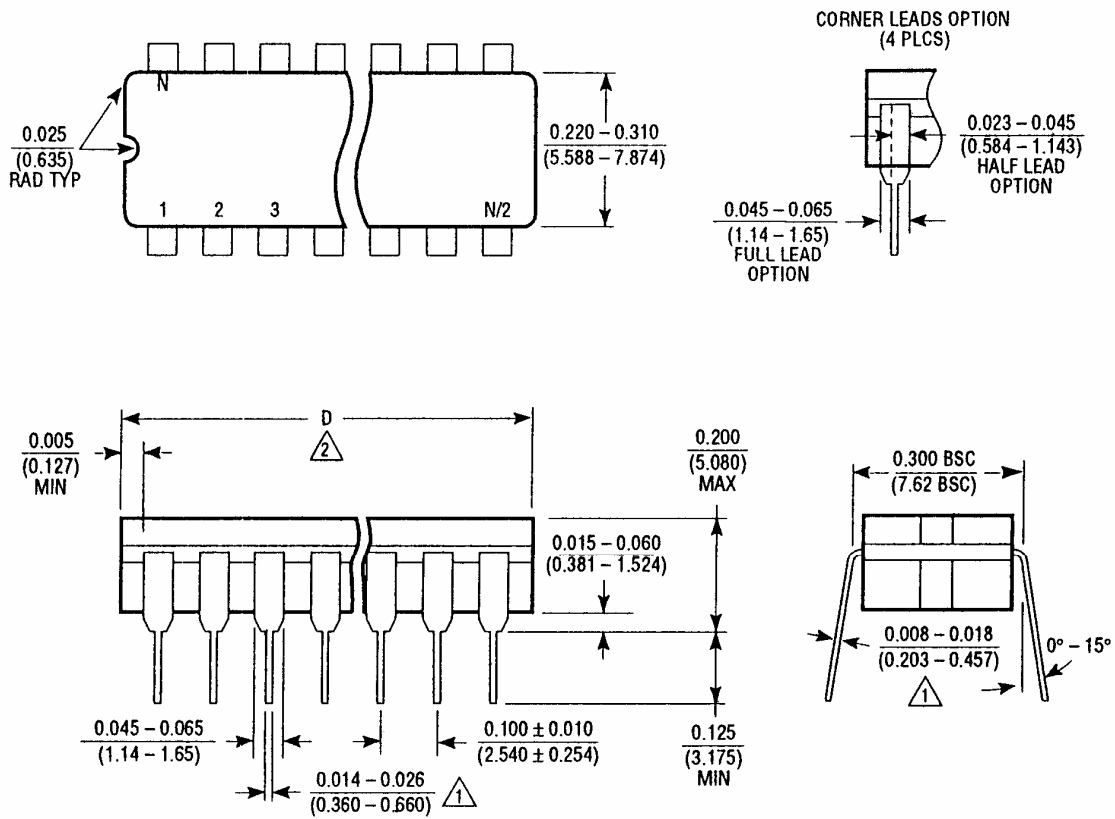


- NOTE: 1. LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND SEATING PLANE.
 2. FOR SOLDER DIP LEAD FINISH, LEAD DIAMETER IS $\frac{0.016 - 0.024}{(0.406 - 0.610)}$

$\theta_{ja} = +150^{\circ}\text{C/W}$
 $\theta_{jc} = +40^{\circ}\text{C/W}$

FIGURE 1

DEVICE OPTION # 2
(J8) CERAMIC DIP / 8 LEADS CASE OUTLINE

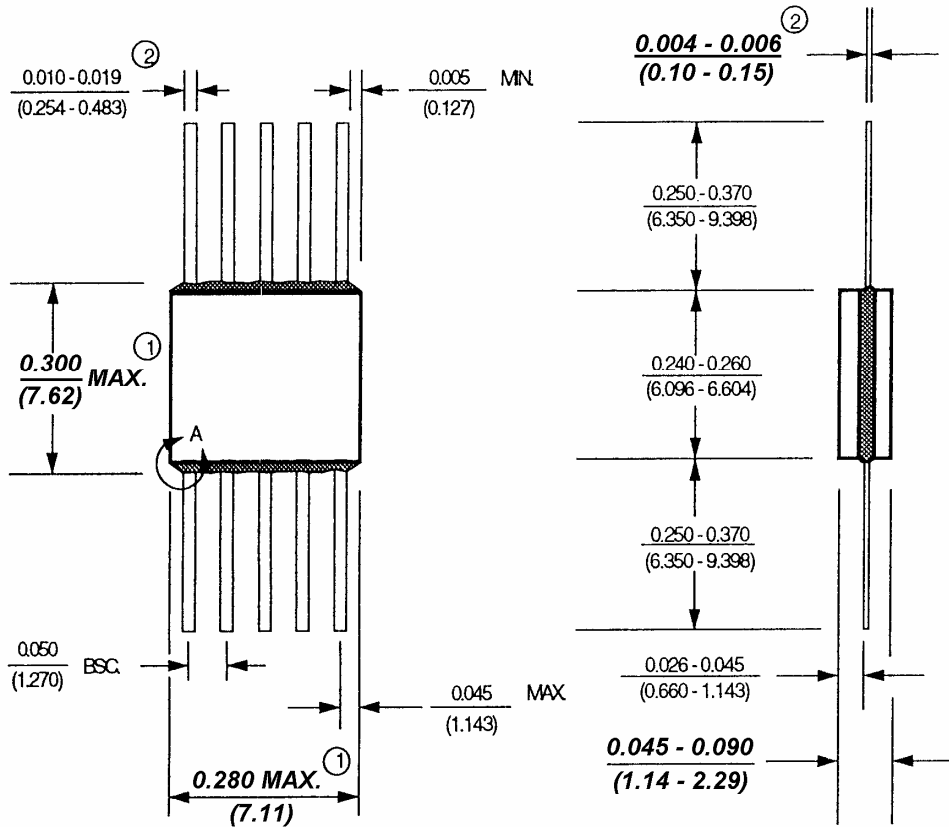


NOTE: 1. LEAD DIMENSIONS APPLY TO SOLDER DIP OR TIN PLATE LEADS.
 2. 8 LEAD D MAX = .405 (10.287)

$\theta_{ja} = +110^\circ\text{C/W}$
 $\theta_{jc} = +30^\circ\text{C/W}$

FIGURE 2

DEVICE OPTION # 3
(W10) GLASS SEALED FLATPACK / 10LEADS CASE OUTLINE



NOTE: 1. THIS DIMENSION ALLOWS FOR OFF-CENTER LID, MENISCUS AND GLASS OVER RUN.

NOTE: 2. INCREASE DIMENSION BY 0.003 INCH WHEN LEAD FINISH IS APPLIED (SOLDER DIPPED).

$\theta_{ja} = +170^{\circ}\text{C/W}$
 $\theta_{jc} = +40^{\circ}\text{C/W}$

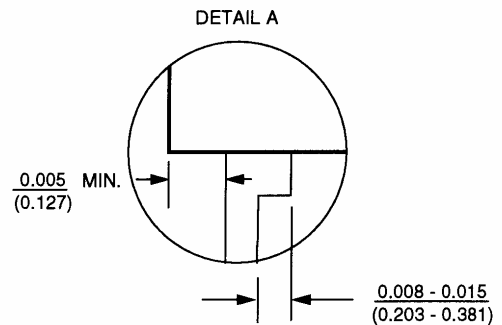


FIGURE 3

TERMINAL CONNECTIONS

DEVICE OPTION #1, TO5 8 LEAD METAL CAN

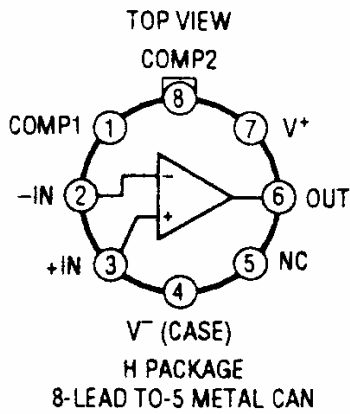


FIGURE 4

DEVICE OPTION #2, 8 LEAD CERAMIC DIP

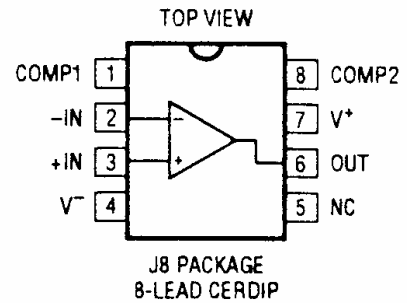


FIGURE 5

**DEVICE OPTION #3, GLASS SEALED
10 LEAD FLATPACK**

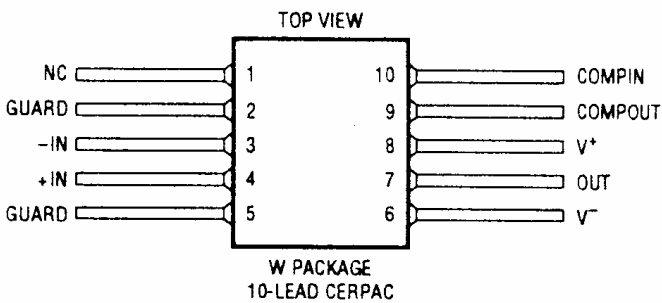
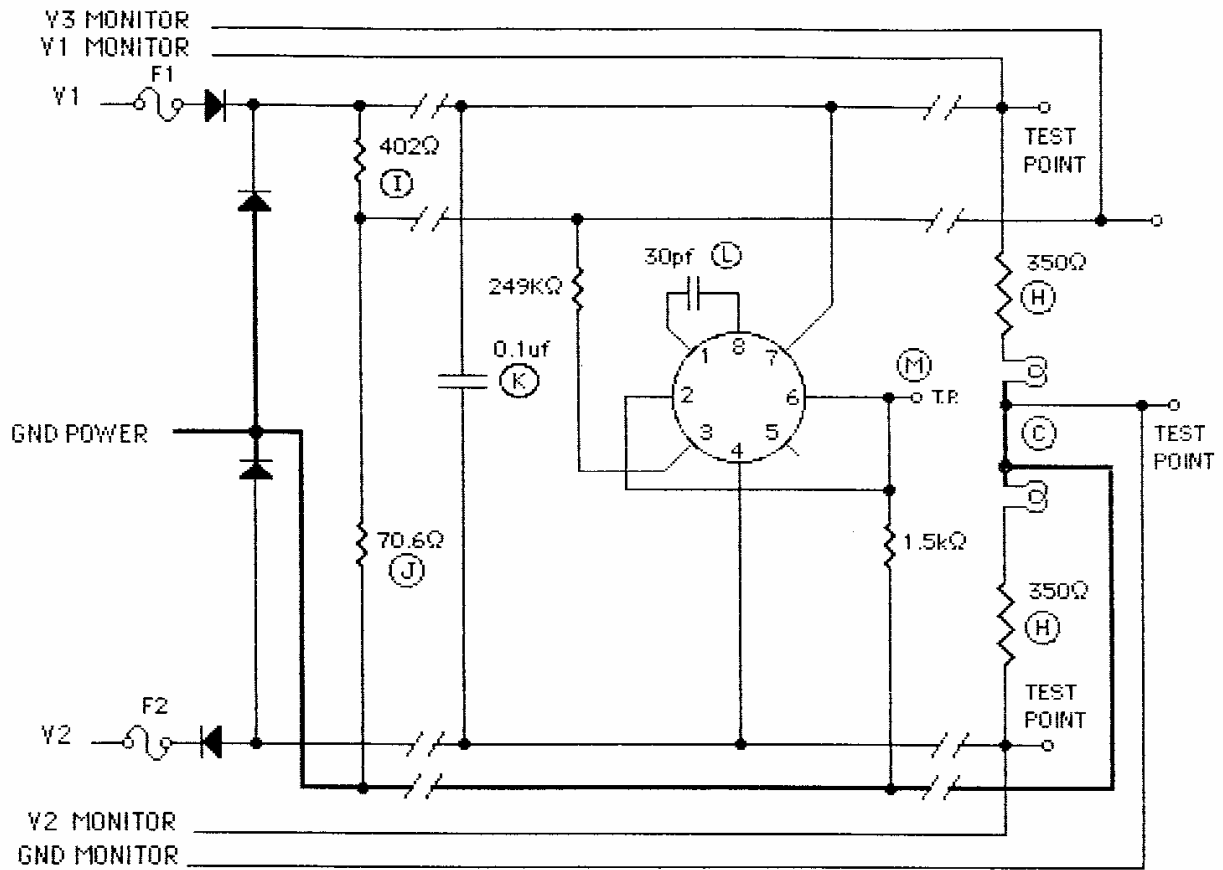


FIGURE 6

**STATIC BURN-IN CIRCUIT
OPTION 1, TO5 METAL CAN / 8 LEADS**



NOTES:

1. Unless otherwise specified, component tolerances shall be per military specification.
2. $T_j = 166^\circ\text{C}$ maximum at 150°C ambient.
3. Burn-in Voltages: $V_1 = +20\text{V}$ to $+22\text{V}$
 $V_2 = -20\text{V}$ to -22V
 $V_3 = +3.0\text{V}$ to $+3.3\text{V}$ MONITOR ONLY

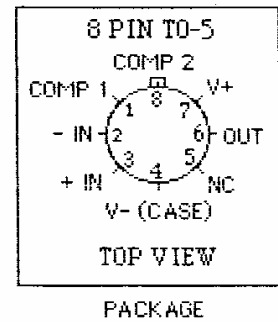
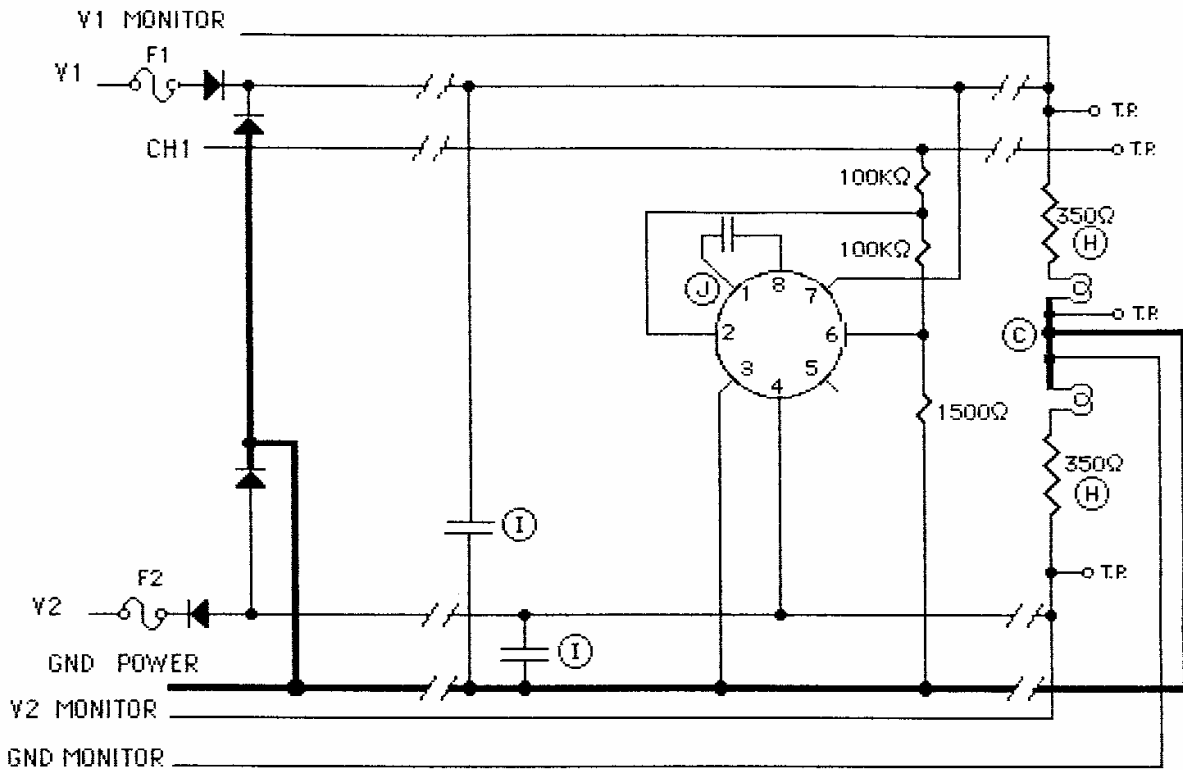


FIGURE 7

**DYNAMIC BURN-IN CIRCUIT
OPTION 1, TO5 METAL CAN / 8 LEADS**



NOTES:

1. Unless otherwise specified, component tolerances shall be per military specification.
2. $T_j = 166\text{ }^\circ\text{C}$ maximum.
3. $T_a = 150\text{ }^\circ\text{C}$.
4. Burn-in Voltages: $V_1 = + 20\text{V}$ to $+22\text{V}$
 $V_2 = - 20\text{V}$ to -22V

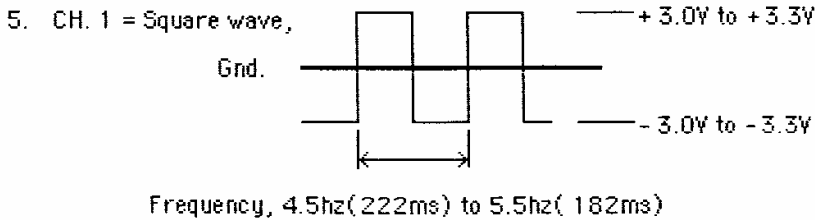
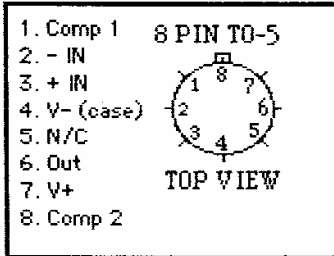
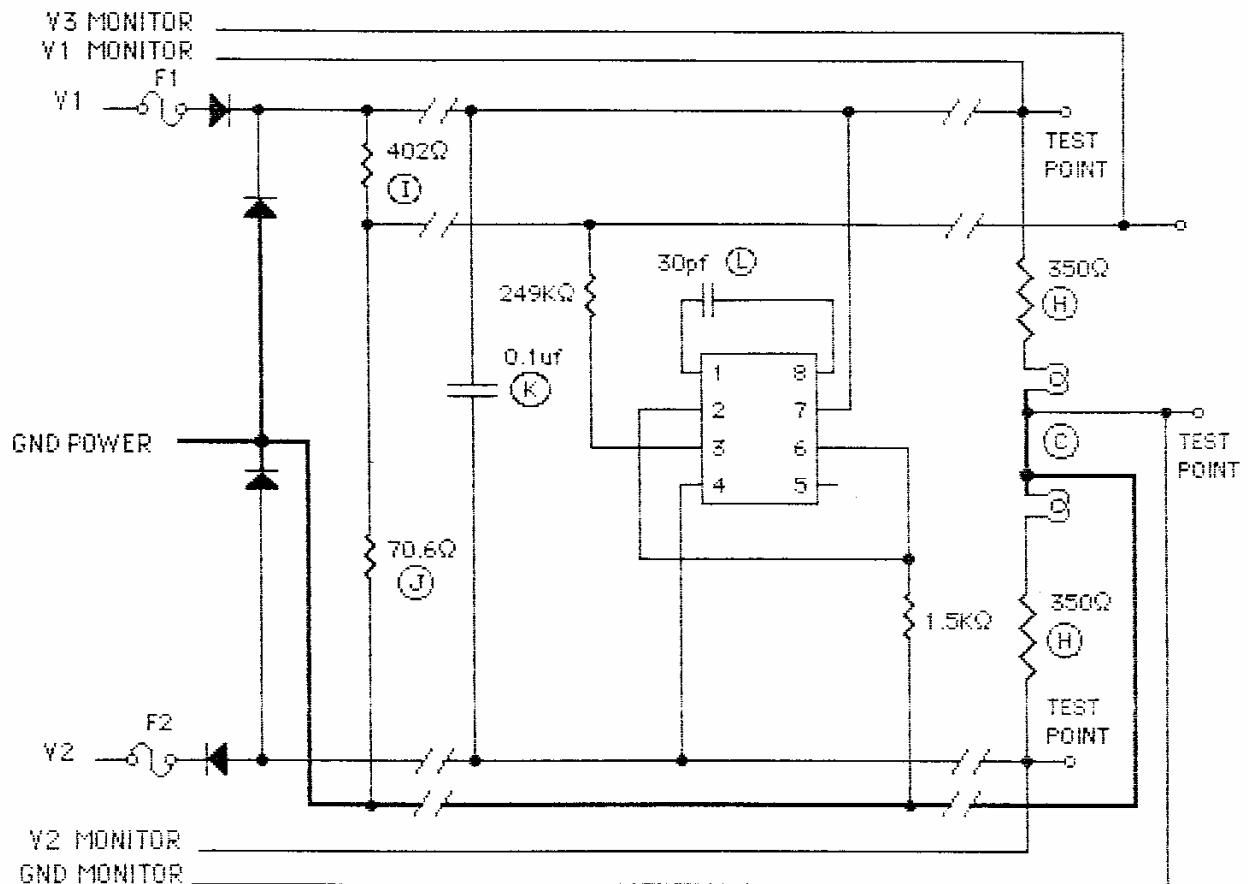


FIGURE 8

**STATIC BURN-IN CIRCUIT
OPTION #2, CerdIP / 8 LEADS**



NOTES:

1. Unless otherwise specified, component tolerances shall be per military specification.
2. $T_j = 169^\circ\text{C}$ maximum at 150°C ambient.
3. Burn-in Voltages: $V_1 = +20\text{V}$ to $+22\text{V}$
 $V_2 = -20\text{V}$ to -22V
 $V_3 = +3.0\text{V}$ to $+3.3\text{V}$ MONITOR ONLY

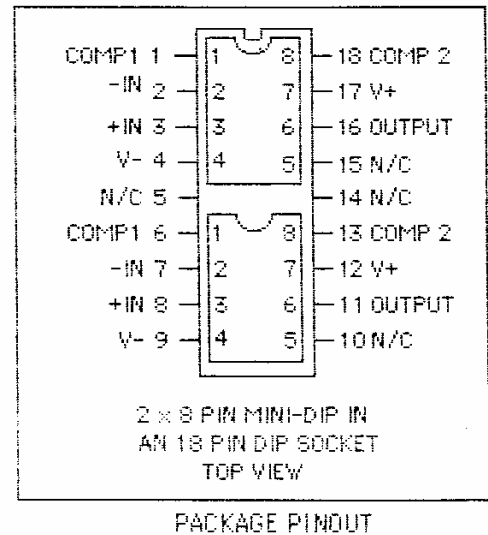
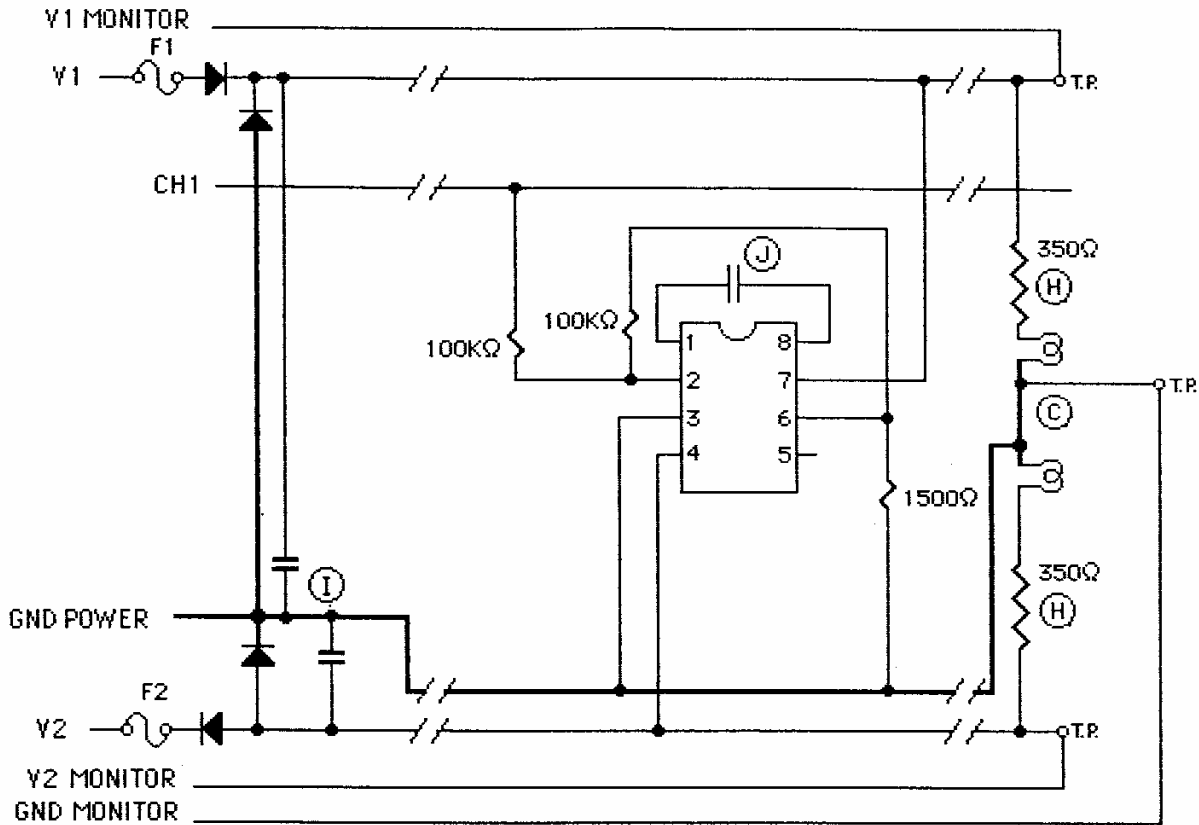


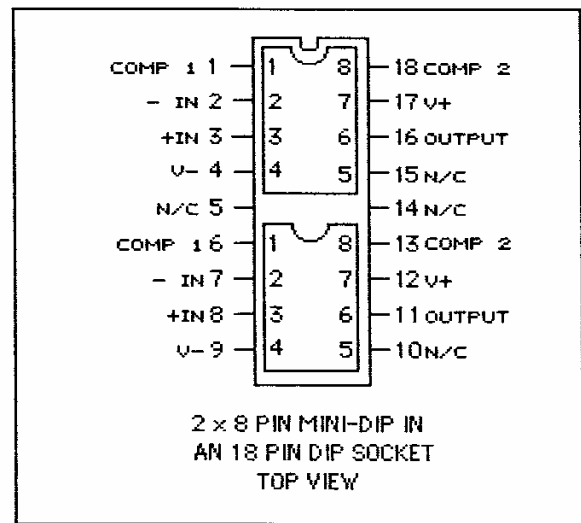
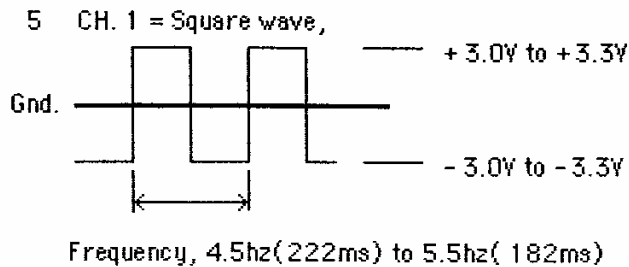
FIGURE 9

**DYNAMIC BURN-IN CIRCUIT
OPTION 2, CerdIP / 8 LEADS**



NOTES:

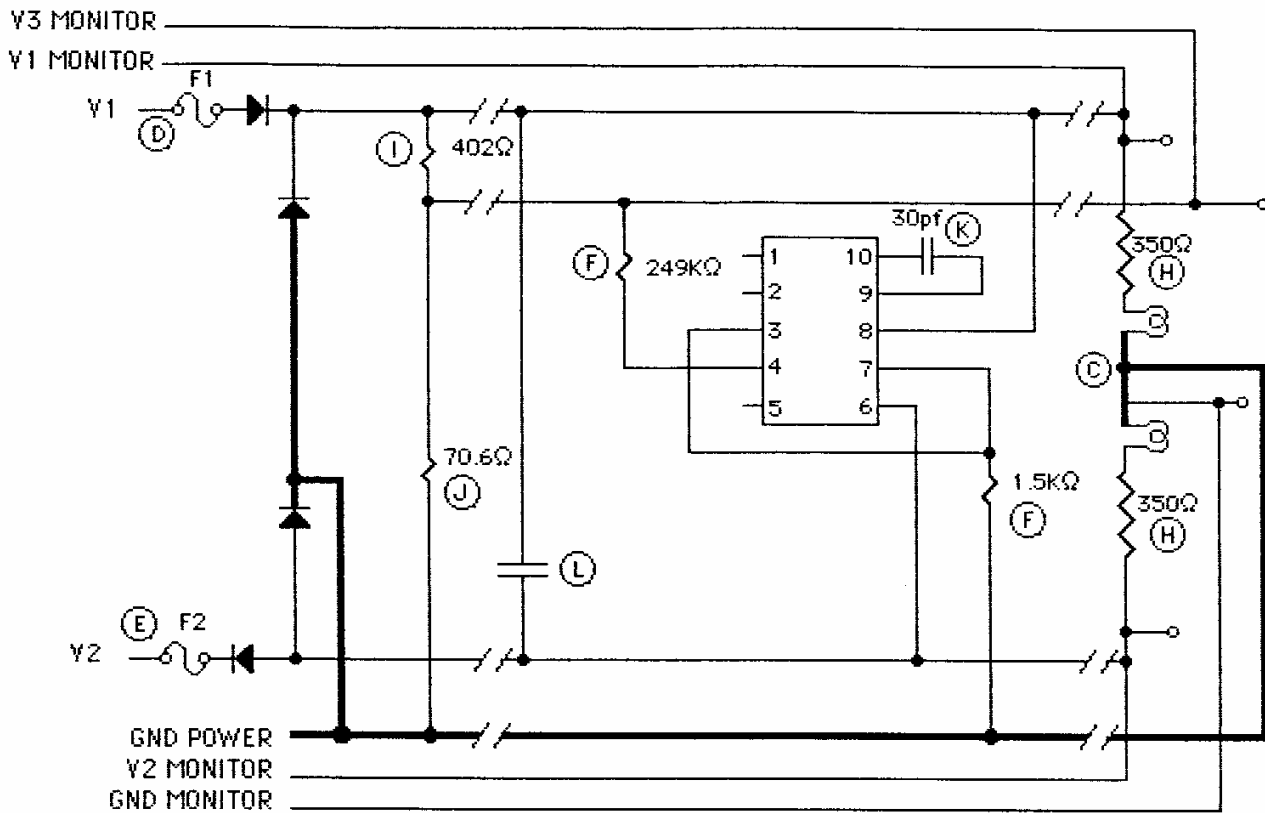
1. Unless otherwise specified, component tolerances shall be per military specification.
2. $T_j = 171^\circ\text{C}$ maximum.
3. $T_a = 150^\circ\text{C}$.
4. Burn-in Voltages: $V_1 = +20\text{V to } +22\text{V}$
 $V_2 = -20\text{V to } -22\text{V}$



PACKAGE AND PINOUT

FIGURE 10

**STATIC BURN-IN CIRCUIT
OPTION 3, GLASS SEALED FLATPACK / 10 LEAD**



NOTES:

1. Unless otherwise specified, component tolerances shall be per military specification.
2. $T_j = 165^\circ\text{C}$ maximum, at 150°C ambient.
3. Burn-in Voltages: $V_1 = +20\text{V}$ to $+22\text{V}$
 $V_2 = -20\text{V}$ to -22V
 $V_3 = +3\text{V}$ to $+3.3\text{V}$ MONITOR ONLY

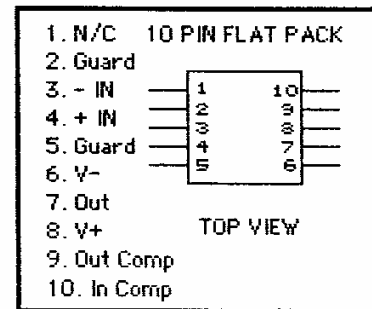
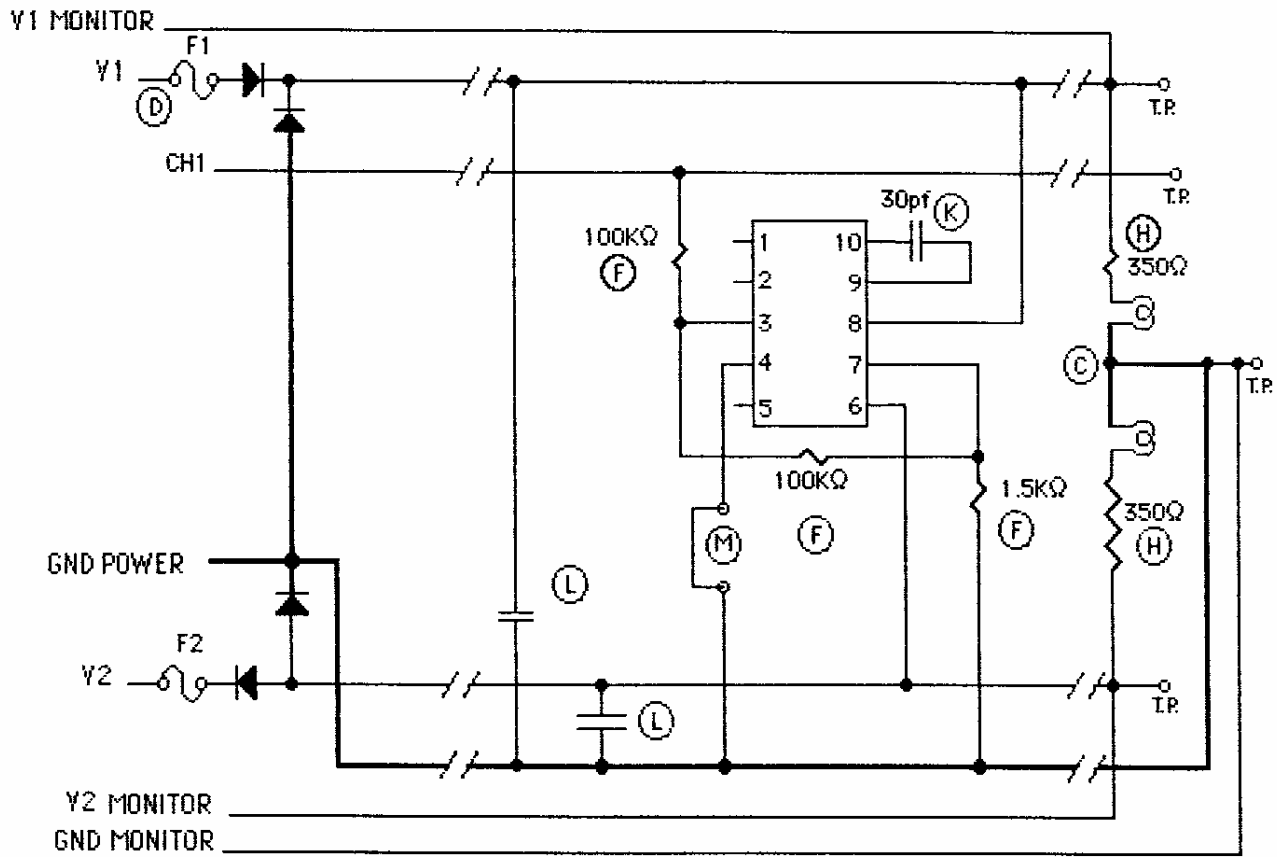


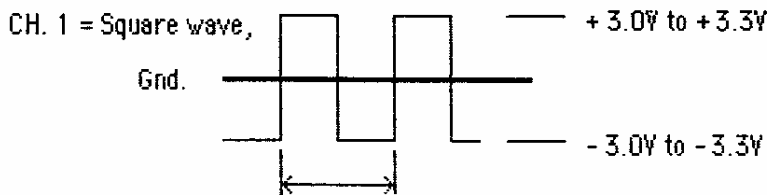
FIGURE 11

**DYNAMIC BURN-IN CIRCUIT
OPTION 3, GLASS SEALED FLATPACK / 10 LEAD**



NOTES:

1. Unless otherwise specified, component tolerances shall be per military specification.
2. $T_j = 169^\circ\text{C}$ maximum, at 150°C ambient.
3. Burn-in Voltages: $V_1 = + 20\text{V}$ to $+ 22\text{V}$
 $V_2 = - 20\text{V}$ to $- 22\text{V}$



Frequency, 4.5hz(222ms) to 5.5hz(182ms)

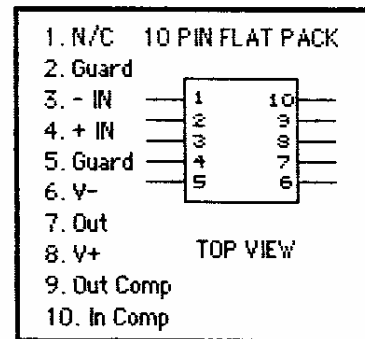


FIGURE 12

TOTAL DOSE BIAS CIRCUIT

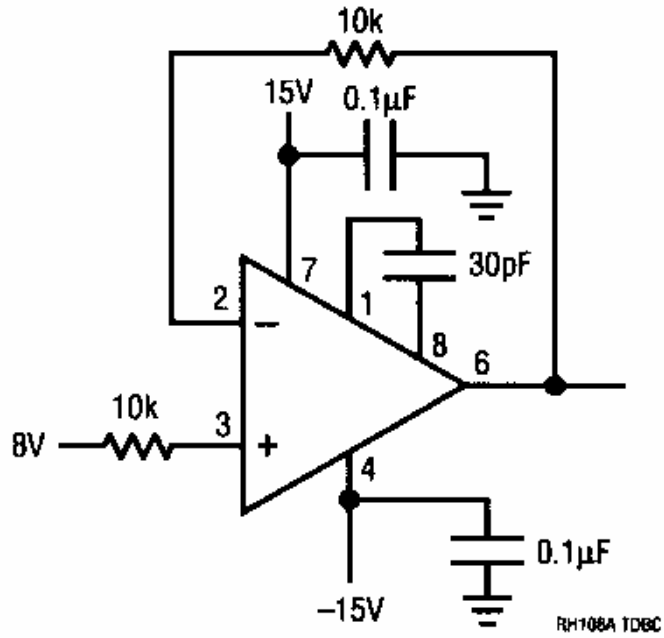


FIGURE 13

TABLE I: ELECTRICAL CHARACTERISTICS (PRE-IRRADIATION) NOTE 4

SYMBOL	PARAMETER	CONDITIONS	NOTES	$T_A = 25^\circ\text{C}$			SUB-GROUP	$-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$			SUB-GROUP	UNITS
				MIN	TYP	MAX		MIN	TYP	MAX		
V_{OS}	Input Offset Voltage				0.5		1		1.0		2,3	mV
$\frac{\Delta V_{OS}}{\Delta \text{Temp}}$	Average Tempco of Offset Voltage		3						5.0			$\mu\text{V}/^\circ\text{C}$
I_{OS}	Input Offset Current				0.2		1		0.4		2,3	nA
$\frac{\Delta I_S}{\Delta \text{Temp}}$	Average Tempco of Offset Current		3						2.5			$\text{pA}/^\circ\text{C}$
I_B	Input Bias Current				2.0		1		3.0		2,3	nA
A_{VOL}	Large-Signal Voltage Gain	$V_S = \pm 15\text{V}$, $V_{OUT} = \pm 10\text{V}$ $R_L \geq 10\text{k}$			80		4		40		5,6	V/mV
CMRR	Common Mode Rejection Ratio				96		1		96		2,3	dB
PSRR	Power Supply Rejection Ratio				96		1		96		2,3	dB
	Input Voltage Range	$V_S = \pm 15\text{V}$	3		± 13.5				± 13.5			V
V_{OUT}	Output Voltage Swing	$V_S = \pm 15\text{V}$, $R_L = 10\text{k}$			± 13		4		± 13		5,6	V
R_{IN}	Input Resistance		3		30							$\text{M}\Omega$
I_S	Supply Current	(Note 6)			0.6		1		0.4		2	mA

TABLE II: ELECTRICAL CHARACTERISTICS (POST-IRRADIATION) NOTE 5

SYMBOL	PARAMETER	CONDITIONS	NOTES	10KRAD (Si)		20KRAD (Si)		50KRAD (Si)		80KRAD (Si)		UNITS
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OS}	Input Offset Voltage				0.5		0.5		0.5		1.0	mV
I_{OS}	Input Offset Current				0.3		0.3		0.3		0.3	nA
I_B	Input Bias Current				± 2.0		± 2.0		± 2.0		± 4.0	nA
A_{VOL}	Large-Signal Voltage Gain	$V_S = \pm 15\text{V}$, $V_{OUT} = \pm 10\text{V}$ $R_L \geq 10\text{k}$			98		98		90		86	dB
CMRR	Common Mode Rejection Ratio				96		96		84		70	dB
PSRR	Power Supply Rejection Ratio		4		96		96		84		70	dB
	Input Voltage Range		3		± 13.5		± 13.5		± 13.5		± 13.5	V
V_{OUT}	Output Voltage Swing				± 13		± 13		± 13		± 13	V
R_{IN}	Input Resistance		3		30		30		30		30	$\text{M}\Omega$
I_S	Supply Current				0.6		0.6		0.6		0.6	mA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: For supply voltages less than $\pm 15\text{V}$, the maximum input voltage is equal to the supply voltage.

Note 3: Guaranteed by design, characterization or correlation to other tested parameters.

Note 4: $\pm 5\text{V} \leq V_S \leq \pm 20\text{V}$ preirradiation, $\pm 5\text{V} \leq V_S \leq \pm 15\text{V}$ postirradiation, unless otherwise noted.

Note 5: $V_S = \pm 15\text{V}$, $V_{CM} = 0\text{V}$, $T_A = 25^\circ\text{C}$ unless otherwise noted.

Note 6: $25^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$.

TABLE III: POST BURN-IN ENDPOINTS AND DELTA LIMIT REQUIREMENTS

$$T_A = 25^\circ\text{C}$$

PARAMETER	ENDPOINT LIMIT		DELTA		UNITS
	MIN	MAX	MIN	MAX	
V_{OS}	-500	500	-250	250	μV
$+I_B$	-0.1	2.0	-0.5	0.5	nA
$-I_B$	-0.1	2.0	-0.5	0.5	nA

TABLE IV: ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUP
FINAL ELECTRICAL TEST REQUIREMENTS (METHOD 5004)	1*, 2, 3, 4, 5, 6
GROUP A TEST REQUIREMENTS (METHOD 5005)	1, 2, 3, 4, 5, 6
GROUP B AND D FOR CLASS S ENDPOINT ELECTRICAL PARAMETERS (METHOD 5005)	1, 2, 3

*PDA APPLIES TO SUBGROUP 1.

PDA TEST NOTE: The PDA is specified as 5% based on failures from Group A, Subgroup 1, tests after cooldown as the final electrical test in accordance with method 5004 of MIL-STD-883. The verified failures of Group A, Subgroup 1 and delta rejects after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent for the lot.