

REVISION RECORD		
REV	DESCRIPTION	DATE
0	INITIAL RELEASE	02/12/09
A	PAGE 11, REMOVE UNNECESSARY TEST CONDITIONS FROM PSRR AND CMRR. CHANGED TEST CONDITIONS ON PSRR.	04/13/09
B	CORRECT REVISION TYPOS ON PAGE 1 OF DOCUMENT; UP-REV FROM '0' TO 'B'	09/24/09
C	Page 2, amended section 3.3, <u>Special Handling of Dice</u> , to more accurately describe our current procedures and requirements.	03/30/12
D	Page 13, Changed RH Canned Sample Table for Qualifying Dice Sales: Subgroup 6 Sample Size Series changed from 45 (3) to 65 (3). First note had the Sample Size Series from "15%" to "10%". ECN #: 13C13929	09/24/13
E	Updated Die Sales table on pg 13.	03/25/15
F	<b>Replace electrical characteristic Table II on page 12</b>	<b>04/16/15</b>

**CAUTION: ELECTROSTATIC DISCHARGE SENSITIVE PART**

REVISION	PAGE NO.	1	2	3	4	5	6	7	8	9	10	11	12	13			
INDEX	REVISION	F	F	F	F	F	F	F	F	F	F	F	F	F			
REVISION	PAGE NO.																
INDEX	REVISION																
										<b>LINEAR TECHNOLOGY CORPORATION</b> <b>MILPITAS, CALIFORNIA</b>							
										TITLE: <b>MICROCIRCUIT, LINEAR, RH1028 / RH1128 ULTRALOW NOISE PRECISION HIGH SPEED OP AMP DICE</b>							
										SIZE	CAGE CODE	DRAWING NUMBER				REV	
											<b>64155</b>	<b>05-08-5238</b>				<b>F</b>	
APPLICATION	FUNCT	SIGNOFFS					DATE	CONTRACT:									

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1.0 SCOPE:

- 1.1 This specification defines the performance and test requirements for a microcircuit processed to a space level manufacturing flow.

2.0 APPLICABLE DOCUMENTS:

- 2.1 Government Specifications and Standards: the following documents listed in the Department of Defense Index of Specifications and Standards, of the issue in effect on the date of solicitation, form a part of this specification to the extent specified herein.

SPECIFICATIONS:

MIL-PRF-38535 Integrated Circuits (Microcircuits) Manufacturing, General Specification for

MIL-STD-883 Test Method and Procedures for Microcircuits

MIL-STD-1835 Microcircuits Case Outlines

- 2.2 Order of Precedence: In the event of a conflict between the documents referenced herein and the contents of this specification, the order of precedence shall be this specification, MIL-PRF-38535 and other referenced specifications.

3.0 REQUIREMENTS:

- 3.1 General Description: This specification details the requirements for the RH1028M / RH1128M, Ultra Noise Precision High Speed Op Amps Dice and Element Evaluation Test Samples, processed to space level manufacturing flow as specified herein.

- 3.2 Part Number: **RH1028M Dice / RH1128M Dice**

- 3.3 Special Handling of Dice: Rad Hard dice require special handling as compared to standard IC dice. Rad Hard dice are susceptible to surface damage due to the absence of silicon nitride passivation that is present on most standard dice. Silicon nitride protects the dice surface from scratches by its hard and dense properties. The passivation on Linear Technology's Rad Hard dice is silicon dioxide which is much "softer" than silicon nitride. During the visual and preparation for shipment, ESD safe Tweezers are used and only the edge of the die are touched.

LTC recommends that dice handling be performed with extreme care so as to protect the die surface from scratches. If the need arises to move the die in or out of the chip shipment tray (waffle pack), use an ESD-Safe-Plastic-tipped Bent Metal Vacuum Probe, preferably .020" OD x .010" ID (for use with tiny parts). The wand should be compatible with continuous air vacuums. The tip material should be static dissipative Delrin (or equivalent) plastic.

During die attach, care must be exercised to ensure no tweezers, or other equipment, touch the top of the dice.

3.4 The Absolute Maximum Ratings (Note 1)

Supply Voltage (-55°C TO 125°C)	±16V
Differential Input Current (Note 9)	±25mA
Input Voltage	Equal to Supply Voltage
Output Short Circuit Duration	Indefinite
Operating Temperature Range	-55°C to 125°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

3.5 Design, Construction, and Physical Dimensions: Detail design, construction, physical dimensions, and electrical requirements shall be specified herein.

3.6 Outline Dimensions and Pad Functions: Dice outline dimensions, pad functions, and locations shall be specified in **Figure 1**.

3.7 Radiation Hardness Assurance (RHA):

3.7.1 The manufacturer shall perform a lot sample test as an internal process monitor for total dose radiation tolerance. The sample test is performed with MIL-STD-883 TM1019 Condition A as a guideline.

3.7.2 For guaranteed radiation performance to MIL-STD-883, Method 1019, total dose irradiation, the manufacturer will provide certified RAD testing and report through an independent test laboratory when required as a customer purchase order line item.

3.7.3 Total dose bias circuit is specified in **Figure 2**.

3.8 Wafer (or Dice) Probe: Dice shall be 100% probed at Ta = +25°C to the limits shown in **Table I** herein. All reject dice shall be removed from the lot. This testing is normally performed prior to dicing the wafer into chips. Final specifications after assembly are sample tested during the element evaluation.

3.9 Wafer Lot Acceptance: Wafer lot acceptance shall be in accordance with MIL-PRF-38535, Appendix A, except for the following: Top side glassivation thickness shall be a **minimum of 4KÅ**.

3.10 Wafer Lot Acceptance Report: SEM is performed per MIL-STD-883, Method 2018. Copies of SEM photographs shall be supplied with the Wafer Lot Acceptance Report as part of a Space Data Pack when specified as a customer purchase order line item.

3.11 Traceability: Wafer Diffusion Lot and Wafer traceability shall be maintained through Quality Conformance Inspection.

4.0 **QUALITY CONFORMANCE INSPECTION:** Quality Conformance Inspection shall consist of the tests and inspections specified herein.

5.0 **SAMPLE ELEMENT EVALUATION:** A sample from **each wafer supplying dice** shall be assembled and subjected to element evaluation per **Table III** herein.

- 5.1 100 Percent Visual Inspection: All dice supplied to this specification shall be inspected in accordance with MIL-STD-883, Method 2010, Condition A. All reject dice shall be removed from the lot.
- 5.2 Electrical Performance Characteristics for Element Evaluation: The electrical performance characteristics shall be as specified in **Table I and Table II** herein.
- 5.3 Sample Testing: Each wafer supplying dice for delivery to this specification shall be subjected to element evaluation sample testing. No dice shall be delivered until all the lot sample testing has been performed and the results found to be acceptable unless the customer supplies a written approval for shipment prior to completion of wafer qualification as specified in this specification.
- 5.4 Part Marking of Element Evaluation Sample Includes:
  - 5.4.1 LTC Logo
  - 5.4.2 LTC Part Number
  - 5.4.3 Date Code
  - 5.4.4 Serial Number
  - 5.4.5 ESD Identifier per MIL-PRF-38535, Appendix A
  - 5.4.6 Diffusion Lot Number
  - 5.4.7 Wafer Number
- 5.5 Burn-In Requirement: Burn-In circuit for W package is specified in **Figure 3**.
- 5.6 Mechanical/Packaging Requirements: Case Outline and Dimensions are in accordance with **Figure 4**.
- 5.7 Terminal Connections: The terminal connections shall be as specified in **Figure 5**.
- 5.8 Lead Material and Finish: The lead material and finish shall be alloy 42 with hot solder dip (Finish letter A) in accordance with MIL-PRF-38535.

## 6.0 VERIFICATION (QUALITY ASSURANCE PROVISIONS)

- 6.1 Quality Assurance Provisions: Quality Assurance provisions shall be in accordance with MIL-PRF-38535. Linear Technology is a QML certified company and all Rad Hard candidates are assembled on qualified Class S manufacturing lines.
- 6.2 Sampling and Inspection: Sampling and Inspection shall be in accordance with **Table III** herein.
- 6.3 Screening: Screening requirements shall be in accordance with **Table III** herein.
- 6.4 Source Inspection:

- 6.4.1 The manufacturer will coordinate Source Inspection at wafer lot acceptance and pre-seal internal visual.
- 6.4.2 The procuring activity has the right to perform source inspection at the supplier's facility prior to shipment for each lot of deliverables when specified as a customer purchase order line item. This may include wafer lot acceptance, die visual, and final data review.

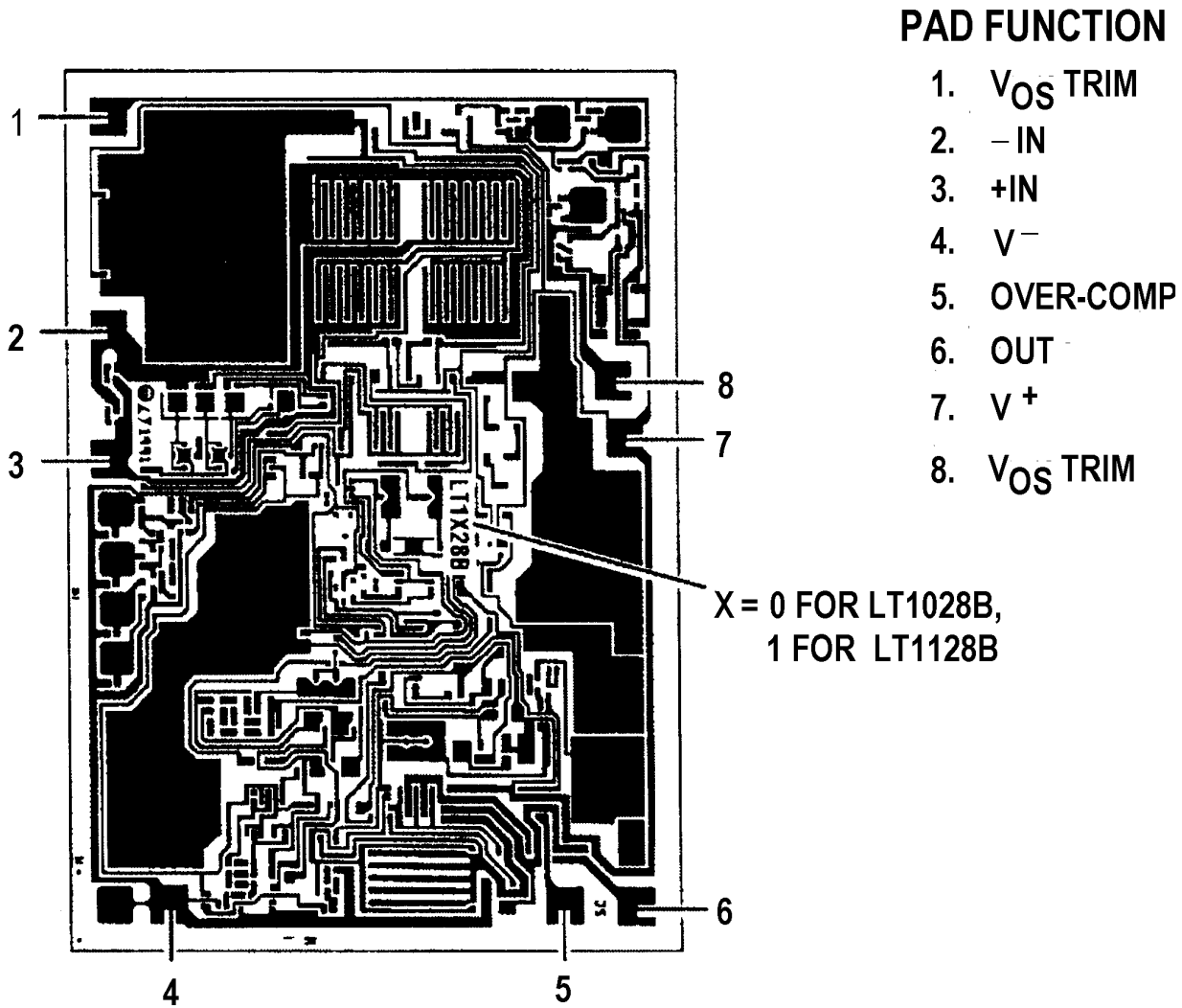
6.5 Deliverable Data: Deliverable data that will ship with devices when a Space Data Pack is ordered:

- 6.5.1 Lot Serial Number Sheets identifying all Canned Sample devices accepted through final inspection by serial number.
- 6.5.2 100% attributes (completed element evaluation traveler).
- 6.5.3 Element Evaluation variables data, including Burn-In and Op Life
- 6.5.4 SEM photographs (3.10 herein)
- 6.5.5 Wafer Lot Acceptance Report (3.9 herein)
- 6.5.6 A copy of outside test laboratory radiation report if ordered
- 6.5.7 Certificate of Conformance certifying that the devices meet all the requirements of this specification and have successfully completed the mandatory tests and inspections herein.

Note: Items 6.5.1 and 6.5.7 will be delivered as a minimum, with each shipment.

7.0 Packaging Requirements: Packaging shall be in accordance with Appendix A of MIL-PRF-38535. All dice shall be packaged in multicavity containers composed of conductive, anti-static, or static dissipative material with an external conductive field shielding barrier.

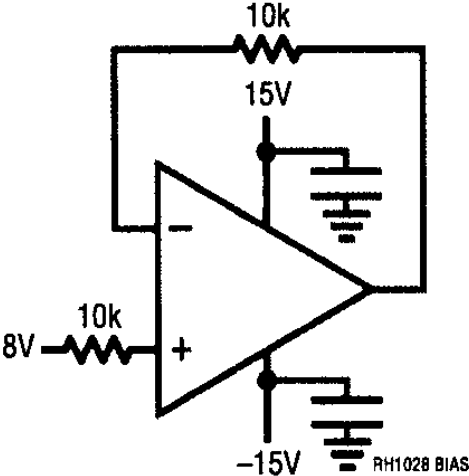
**DICE OUTLINE DIMENSIONS AND PAD FUNCTIONS**



114mils x 81mils,  
 Backside (substrate) metal: Alloye gold layer  
 Backside potential: Connect to  $V^-$

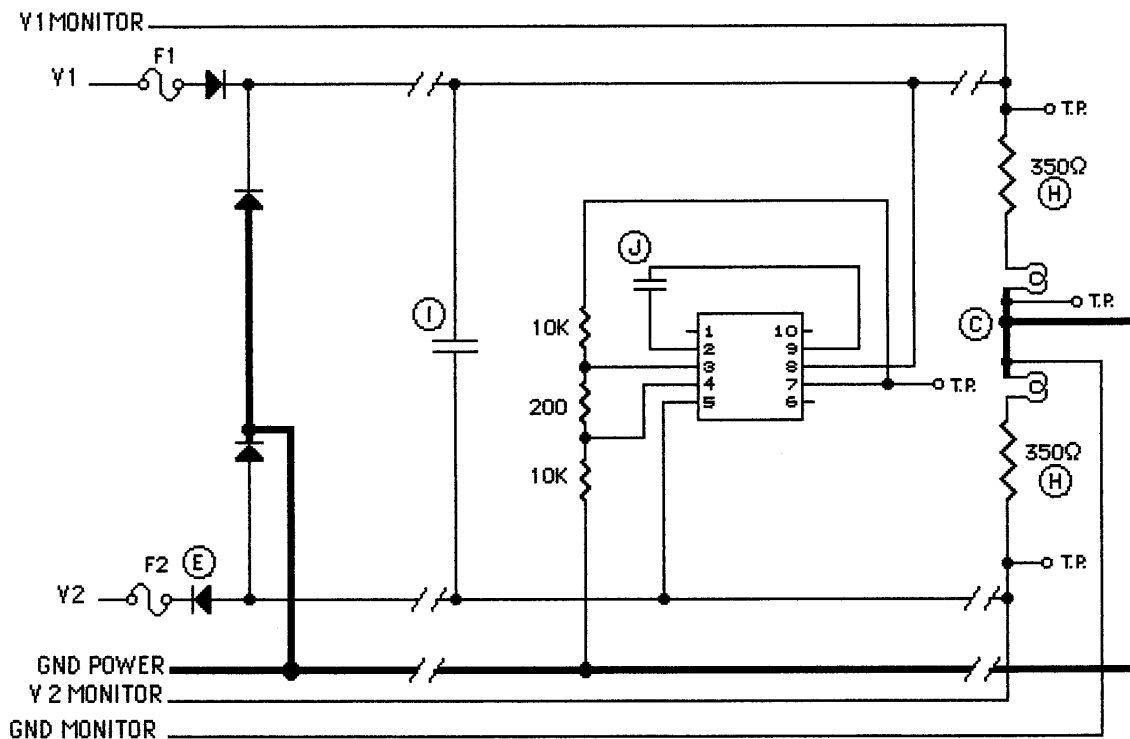
**FIGURE 1**

**TOTAL DOSE BIAS CIRCUIT**



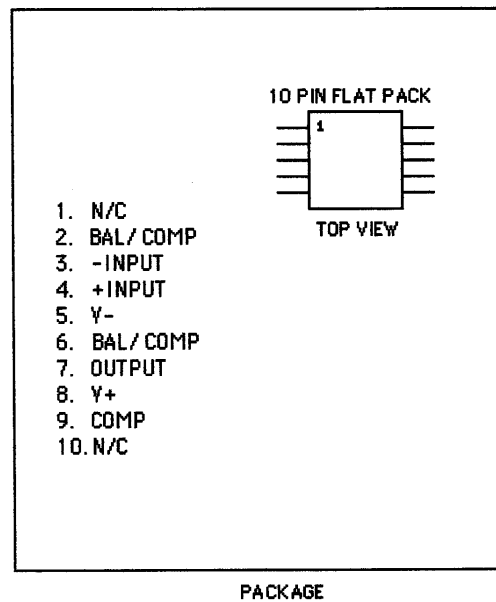
**FIGURE 2**

**BURN-IN CIRCUIT**



**NOTES:**

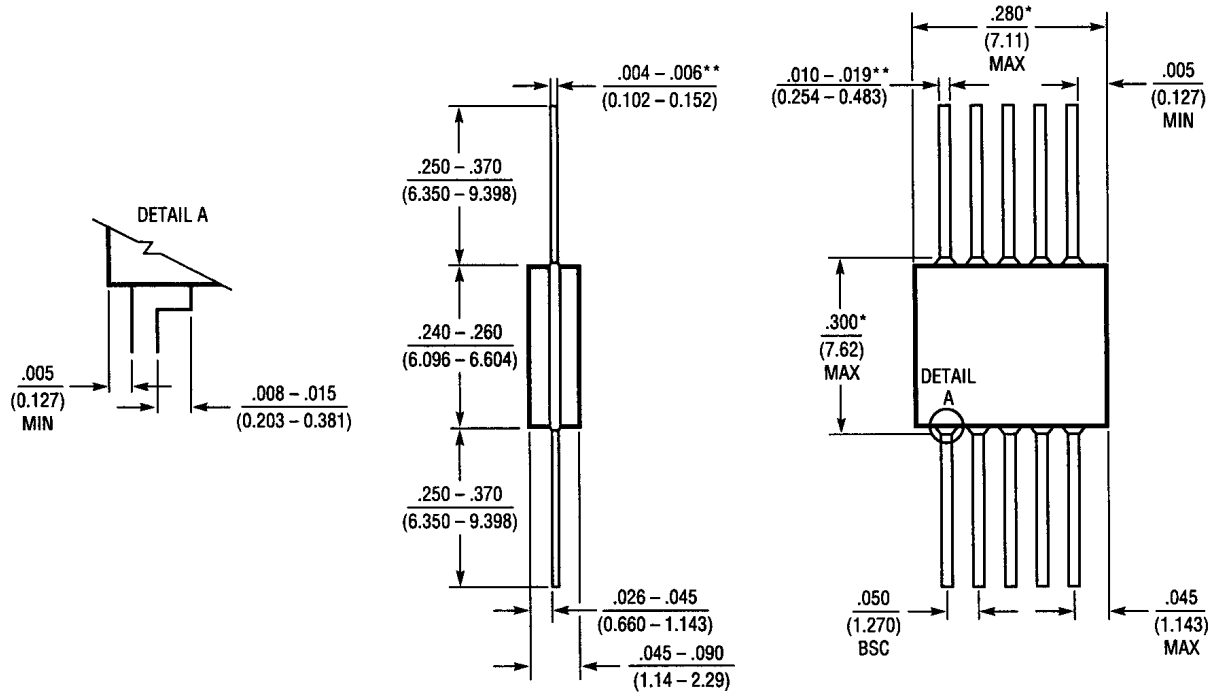
1. Unless otherwise specified, component tolerances shall be per military specification.
2.  $T_a = +90^\circ\text{C}$ .
3.  $T_j = +164^\circ\text{C}$  maximum.
4.  $T_c = +136^\circ\text{C}$  minimum.
5. Burn-in Voltages:  $V_1 = +16\text{V}$  to  $+17\text{V}$   
 $V_2 = -16\text{V}$  to  $-17\text{V}$
6. Device current = 12mA.
7. USE ALL OTHER INFORMATION ON # 04-06-0141



**FIGURE 3**



**(W10) GLASS SEALED FLATPACK / 10LEADS CASE OUTLINE**



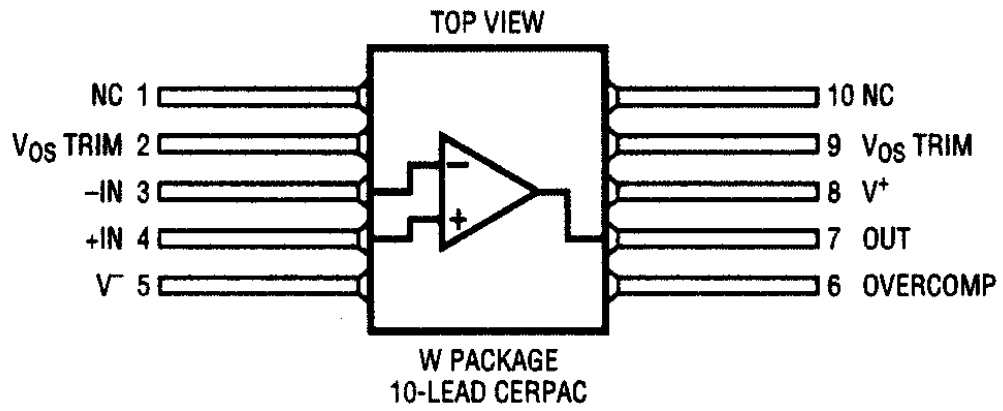
NOTES:  
 \*THIS DIMENSION ALLOWS FOR OFF-CENTER LID, MENISCUS AND GLASS OVERRUN  
 \*\*INCREASE DIMENSIONS BY 0.003 INCHES (0.076 mm) WHEN LEAD FINISH A IS APPLIED (SOLDER DIPPED)

W10 (GLASS) 0603

$\theta_{ja} = +170^{\circ}\text{C/W}$   
 $\theta_{jc} = +40^{\circ}\text{C/W}$

**FIGURE 4**

**TERMINAL CONNECTIONS**



**FIGURE 5**

**TABLE I DICE ELECTRICAL CHARACTERISTICS – Element Evaluation (Notes 1, 2)  
(PRE-IRRADIATION)**

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
$V_{OS}$	Input Offset Voltage (Note 1)			300	$\mu\text{V}$
$I_{OS}$	Input Offset Current	$V_{CM} = 0\text{V}$		150	nA
$I_B$	Input Bias Current	$V_{CM} = 0\text{V}$		$\pm 400$	nA
$V_{IN}$	Input Voltage Range		$\pm 11$		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 11\text{V}$	110		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4\text{V to } \pm 18\text{V}$	110		dB
$A_{VOL}$	Large Scale Voltage Gain	$R_L \geq 2\text{k}, V_O = \pm 10\text{V}$ $R_L \geq 1\text{k}, V_O = \pm 10\text{V}$ $R_L \geq 600\Omega, V_O = \pm 10\text{V}$	5 3.5 2		$\text{V}/\mu\text{V}$ $\text{V}/\mu\text{V}$ $\text{V}/\mu\text{V}$
$V_{OUT}$	Maximum Output Voltage Swing	$R_L \geq 2\text{k}$ $R_L \geq 600\Omega$	$\pm 12$ $\pm 10.5$		V V
SR	Slew Rate	$A_{VCL} = -1$ (RH1028) $A_{VCL} = -1$ (RH1128)	11 4.5		$\text{V}/\mu\text{s}$ $\text{V}/\mu\text{s}$
$I_S$	Supply Current			10.5	mA

**Note 1:** Input offset voltage measurements are performed by automatic test equipment approximately 0.5 seconds after application of power.

**Note 2:** Wafer level testing is performed per the indicated specifications for dice.

Considerable differences in performance can often be observed for dice versus packaged units due to the influences of packaging and assembly on certain devices and/or parameters. Please refer to LTC standard product data sheet for other applicable product information. Please consult factory for more information on dice performance and lot qualifications via lot sampling test procedures.

Dice data sheet subject to change. Please consult factory for current revision in production.

**TABLE II: ELECTRICAL CHARACTERISTICS (NOTE 4)  
(POST-IRRADIATION)**

(Postirradiation)  $V_S = \pm 15V$ ,  $V_{CM} = 0V$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	NOTES	10KRAD(Si)		20KRAD(Si)		50KRAD(Si)		100KRAD(Si)		200KRAD(Si)		UNITS
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$V_{OS}$	Input Offset Voltage		2	100		120		140		160		180		$\mu V$
$I_{OS}$	Input Offset Current			200		200		200		300		500		nA
$I_B$	Input Bias Current			$\pm 600$		$\pm 700$		$\pm 950$		$\pm 1100$		$\pm 1700$		nA
SR	Slew Rate	$A_{VCL} = -1$ (RH1028) $A_{VCL} = -1$ (RH1128)		7.5 3.0		7.5 3.0		7.5 3.0		7.5 3.0		7.5 3.0		V/ $\mu s$ V/ $\mu s$
	Input Voltage Range			$\pm 11$		$\pm 11$		$\pm 11$		$\pm 11$		$\pm 11$		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 11V$		106		106		106		106		106		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4V$ to $\pm 18V$		104		104		104		104		104		dB
$A_{VOL}$	Large-Signal Voltage Gain	$R_L \geq 2k$ , $V_O = \pm 10V$		2		2		2		2		2		V/ $\mu V$
$V_{OUT}$	Maximum Output Voltage Swing	$R_L \geq 2k$ $R_L \geq 600\Omega$		$\pm 11.5$		$\pm 11.5$		$\pm 11.5$		$\pm 11.5$		$\pm 11.5$		V
				$\pm 10$		$\pm 10$		$\pm 10$		$\pm 10$		$\pm 10$		V

**Note 3:** Input offset voltage measurements are performed by automatic test equipment approximately 0.5 seconds after application of power. In addition, at  $T_A = 25^\circ C$ , offset voltage is measured with the chip heated to approximately  $55^\circ C$  to account for the chip temperature rise when the device is fully warmed up.

**Note 4:** Post-Irradiation electrical characteristics are based on LTC standard product data sheet.



**RH CANNED SAMPLE TABLE FOR QUALIFYING DICE SALES**

**TABLE III RH ELEMENT EVALUATION TABLE QUALIFICATION OF DICE SALES**

SUBGROUP	CLASS			OPERATION	MIL-STD-883		QUANTITY (ACCEPT NUMBER) REF. METHOD 2018 FOR S/S
	K/S	V	H/B		METHOD	CONDITION	
1	X	X		SEM	2018	N/A	100%
2	X	X	X	ELEMENT ELECTRICAL (WAFER SORT @ 25°C)			100%
3	X	X	X	ELEMENT VISUAL (2nd OP)	2010	A	100%
4	X	X	X	INTERNAL VISUAL (3rd OP)	2010	A	ASSEMBLED PARTS ONLY
	X	X		DIE SHEAR MONITOR	2019		
	X	X		BOND PULL MONITOR	2011		ASSEMBLED PARTS ONLY
5	X	X		STABILIZATION BAKE	1008	C	
	X	X		TEMPERATURE CYCLE	1010	C	
	X	X		CONSTANT ACCELERATION	2001	E	
	X	X		FINE LEAK	1014	A	ASSEMBLED PARTS ONLY
	X	X		GROSS LEAK	1014	C	
6	X	X		FIRST ROOM ELECTRICAL - READ & RECORD (REPLACE ANY ASSEMBLY-RELATED REJECTS)			
	X	X		PRE BURN-IN ELECT. READ & RECORD @ +125°C or +150°C, -55°C			+ 125°C MINIMUM 240 HOURS
	X	X		BURN-IN: +125°C/240 hrs. or +150°C/120 hrs.	1015		
	X	X		POST BURN-IN ELECT. READ & RECORD @ 25°C			
	X	X		POST BURN-IN ELECT. READ & RECORD @ +125°C or +150°C, -55°C			
	X	X		TOTAL IRRADIATION DOSE	1019	A	+ 125°C MINIMUM 1000 HOURS
	X	X		PRE OP-LIFE ELECTRICAL @ 25°C READ & RECORD			
	X	X		OPERATING LIFE: +125°C/1000 hrs. or +150°C/500 hrs.	1005		
	X	X		POST OP-LIFE ELECT. (R & R @ 25°C, +125°C DR +150°C, -55°C			15(0) OR 25(1) - # of wires
7	X	X	X	WIRE BOND EVALUATION	2011		

**NOTE:** LTC is not qualified to process to MIL-PRF-38534. This is an LTC imposed element evaluation that follows MIL-STD-883 test methods and conditions. Please note the quantity and accept number from Sample Size Series of 5%, accept on 0, and note that the actual sample and accept number does not begin until Subgroup 6 OP-LIFE.

**NOTE:** Tests within Subgroup 5 may be performed in any sequence.

**NOTE:** LTC's radiation tolerance (RH) die has a topside glassivation thickness of 4KA minimum.

**NOTE:** Sample sizes on the travelers may be larger than that indicated in the above table; however, the larger sample size is to accommodate extra units for replacement devices in the event of equipment or operator error and for assembly related rejects in Subgroup 6, and for Wire Bond Evaluation, Subgroup 7. The larger sample size is at all times kept segregated and, if used for qualification, has all the required processing imposed.