

REVISION RECORD		
REV	DESCRIPTION	DATE
0	INITIAL RELEASE	05/13/08
A	PAGE 11: TABLE 1, ELECTRICAL CHARACTERISTICS AMENDED. PAGE 12: RE-ARRANGED NOTES FOLLOWING TABLE II. PAGE 13: ADDED TABLE III FOR POST BURN-IN ENDPOINTS AND DELTA LIMIT REQUIREMENTS. ADDED POST B5 AND B6 25°C LIMITS AFTER TABLE IV.	02/24/09
B	<b>REPLACE ELECTRICAL CHARACTERISTIC TABLE II WITH UPDATED ELECTRICAL CHARACTERISTIC ON PG 12</b>	<b>04/16/15</b>

**REVISION RECORD AND DESCRIPTION CONTINUED ON NEXT PAGE.**

**CAUTION: ELECTROSTATIC DISCHARGE SENSITIVE PART**

REVISION	PAGE NO.	1	2	3	4	5	6	7	8	9	10	11	12	13				
INDEX	REVISION	B	B	B	B	B	B	B	B	B	B	B	B	B				
REVISION	PAGE NO.																	
INDEX	REVISION																	

			<b>LINEAR TECHNOLOGY CORPORATION</b>								
	ORIG		<b>MILPITAS, CALIFORNIA</b>								
	DSGN		TITLE:								
	ENGR		<b>MICROCIRCUIT, LINEAR,</b>								
	MFG		<b>RH1028M, ULTRALOW NOISE PRECISION</b>								
	CM		<b>HIGH SPEED OP AMPS</b>								
	QA		SIZE	CAGE CODE	DRAWING NUMBER	REV					
	PROG			64155	05-08-5217	B					
APPLICATION	FUNCT	SIGNOFFS	DATE	CONTRACT:							

FOR OFFICIAL USE ONLY

**1.0 SCOPE:**

- 1.1 This specification defines the performance and test requirements for a microcircuit processed to a space level manufacturing flow.

**2.0 APPLICABLE DOCUMENTS:**

- 2.1 Government Specifications and Standards: the following documents listed in the Department of Defense Index of Specifications and Standards, of the issue in effect on the date of solicitation, form a part of this specification to the extent specified herein.

**SPECIFICATIONS:**

MIL-PRF-38535 Integrated Circuits (Microcircuits) Manufacturing, General Specification for

MIL-STD-883 Test Method and Procedures for Microcircuits

MIL-STD-1835 Microcircuits Case Outlines

- 2.2 Order of Precedence: In the event of a conflict between the documents referenced herein and the contents of this specification, the order of precedence shall be this specification, MIL-PRF-38535 and other referenced specifications.

**3.0 REQUIREMENTS:**

- 3.1 General Description: This specification details the requirements for the RH1028 REFERENCE processed to space level manufacturing flow.

- 3.2 Part Number:

**3.2.1 Option 1 – RH1028MW (Glass Sealed Flatpack, 10 Leads)**

- 3.3 Part Marking Includes:

- a. LTC Logo
- b. LTC Part Number (See Paragraph 3.2)
- c. Date Code
- d. Serial Number
- e. ESD Identifier per MIL-PRF-38535, Appendix A

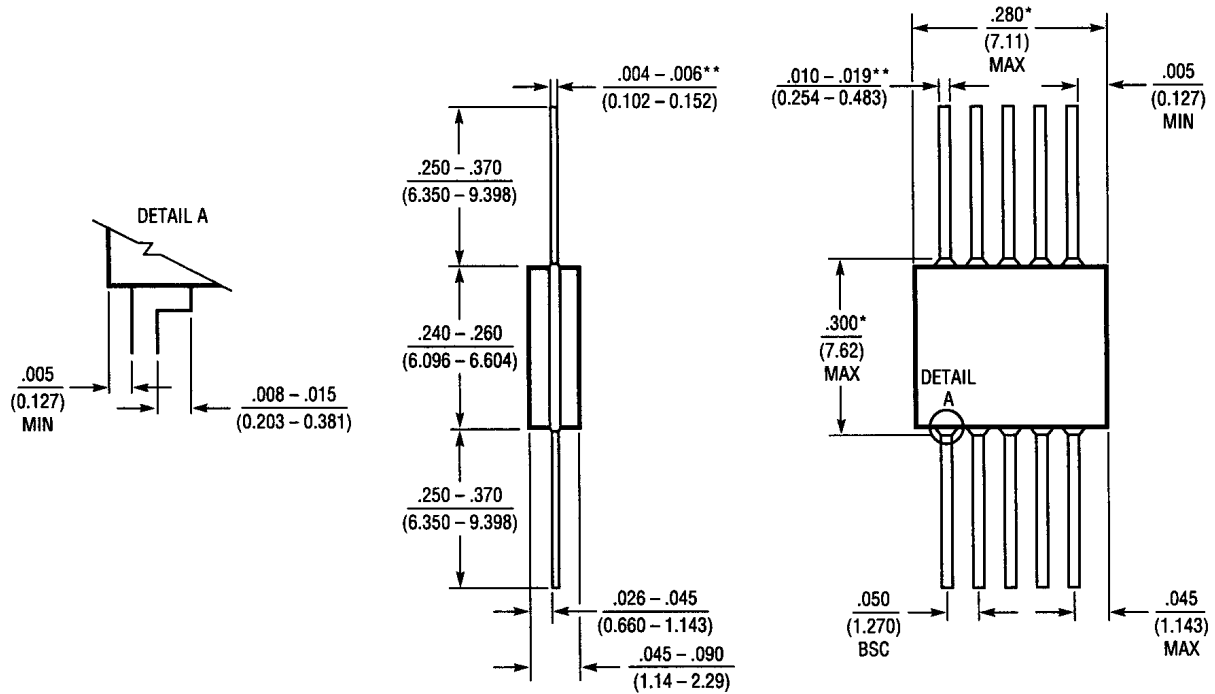
- 3.4 The Absolute Maximum Ratings:  
(Note1)
- |                                       |                         |
|---------------------------------------|-------------------------|
| Supply Voltage (-55°C TO 125°C)       | ±16V                    |
| Differential Input Current (Note 9)   | ±25mA                   |
| Input Voltage                         | Equal to Supply Voltage |
| Output Short Circuit Duration         | Indefinite              |
| Operating Temperature Range           | -55°C to 125°C          |
| Storage Temperature Range             | -65°C to 150°C          |
| Lead Temperature (Soldering, 10 sec.) | 300°C                   |
- 3.5 Electrostatic discharge sensitivity, ESDS, shall be Class 1.
- 3.6 Electrical Performance Characteristics: The electrical performance characteristics shall be as specified in Table I and Table II.
- 3.7 Electrical Test Requirements: Screening requirements shall be in accordance with 4.1 herein, MIL-STD-883, Method 5004 and as specified in Table IV herein.
- 3.8 Burn-In Requirement: Burn-in circuit is specified in Figure 4, 5.
- 3.9 Delta Limit Requirement: Delta limit parameters are specified in Table III herein, are calculated after each burn-in, and the delta rejects are included in the PDA calculation.
- 3.10 Design, Construction, and Physical Dimensions: Detail design, construction, physical dimensions, and electrical requirements shall be specified herein.
- 3.10.1 Mechanical / Packaging Requirements: Case outlines and dimensions are in accordance with Figure 1.
- 3.10.2 Terminal Connections: The terminal connections shall be as specified in Figure 2.
- 3.10.3 Lead Material and Finish: The lead material and finish for Option 1 shall be Alloy 42 for Flatpack with lead finish hot solder dip (Finish litter A) in accordance with MIL-PRF-38535.
- 3.11 Radiation Hardness Assurance (RHA):
- 3.11.1 The manufacturer shall perform a lot sample test as an internal process monitor for total dose radiation tolerance. The sample test is performed with MIL-STD-883 TM1019 Condition A as a guideline.
- 3.11.2 For guaranteed radiation performance to MIL-STD-883, Method 1019, total dose irradiation, the manufacturer will provide certified RAD testing and report through an independent test laboratory when required as a customer purchase order line item.
- 3.11.3 Total dose bias circuit is specified in Figure 3.
- 3.12 Wafer Lot Acceptance: Wafer lot acceptance shall be in accordance with MIL-PRF-38535, Appendix A, except for the following: Topside glassivation thickness shall be a minimum of 4KÅ.
- 3.13 Wafer Lot Acceptance Report: SEM is performed per MIL-STD-883, Method 2018 and copies of SEM photographs shall be supplied with the Wafer Lot Acceptance Report as part of a Space Data Pack when specified as a customer purchase order line item.

## 4.0 VERIFICATION (QUALITY ASSURANCE PROVISIONS)

- 4.1 Quality Assurance Provisions: Quality Assurance provisions shall be in accordance with MIL-PRF-38535. Linear Technology is a QML certified company and all Rad Hard candidates are assembled on qualified Class S manufacturing lines.
- 4.2 Sampling and Inspection: Sampling and Inspection shall be in accordance with MIL-STD-883, Method 5005 with QML allowed and TRB approved deviations in conjunction with paragraphs 3.1.1, 3.2.1, and 3.4 of the test method.
- 4.3 Screening: Screening requirements shall be in accordance with MIL-STD-883, Method 5004 with QML allowed and TRB approved deviations in conjunction with paragraphs 3.1, 3.1.1, and 3.4 of the test method. Electrical testing shall be as specified in Table IV herein.
- 4.3.1 Analysis of catastrophic (open/short) failures from burn-in will be conducted only when a lot fails the burn-in or re-burn-in PDA requirements.
- 4.4 Quality Conformance Inspection: Quality conformance inspection shall be in accordance with 4.2 and 4.3 herein and as follows:
- 4.4.1 Group A Inspection: Group A inspection shall be performed in accordance with 4.1 herein, per MIL-STD-883, Method 5005, and specified in Table IV herein.
- 4.4.2 Group B Inspection: When purchased, a full Group B is performed on an inspection lot. As a minimum, Subgroup B2 (Resistance to Solvents / Mark Permanency) and Subgroup B3 (Solderability) are performed prior to the first shipment from any inspection lot and Attributes provided when a Full Space Data Pack is ordered. Subgroup B5 (Operating Life) is performed on each wafer lot. This subgroup may or may not be from devices built in the same package style as the current inspection lot. Attributes and variables data for this subgroup will be provided upon request at no charge.
- |         |                            |  |
|---------|----------------------------|--|
| 4.4.2.1 | Group B, Subgroup 2c = 10% | Group B, Subgroup 5 = *5%  |
|         | Group B, Subgroup 3 = 10%  | (*per wafer or inspection lot<br>whichever is the larger quantity) |
|         | Group B, Subgroup 4 = 5%   | Group B, subgroup 6 = 15%  |
- 4.4.2.2 All footnotes pertaining to Table IIa in MIL-STD-883, Method 5005 apply. The quantity (accept number) of all other subgroups are per MIL-STD-883, Method 5005, Table IIa.
- 4.4.3 Group D Inspection: When purchased, a full Group D is performed on an inspection lot. As a minimum, periodic full Group D sampling is performed on each package family for each assembly location every 26 weeks. A generic Group D Summary is provided when a full Space Data Pack is ordered.
- 4.4.3.1 Group D, Subgroups 3, 4 and 5 = 15% each (Sample Size Series).
- 4.4.3.2 All footnotes pertaining to Table IV in MIL-STD-883, Method 5005 apply. The quantity (accept number) or sample number and accept number of all other subgroups are per MIL-STD-883, Method 5005, Table IV.

- 4.5 Source Inspection:
- 4.5.1 The manufacturer will coordinate Source Inspection at wafer lot acceptance and pre-seal internal visual.
  - 4.5.2 The procuring activity has the right to perform source inspection at the supplier's facility prior to shipment for each lot of deliverables when specified as a customer purchase order line item. This may include wafer lot acceptance and final data review.
- 4.6 Deliverable Data: Deliverable data that will ship with devices when a Space Data Pack is ordered:
- 4.6.1 Lot Serial Number Sheets identifying all devices accepted through final inspection by serial number.
  - 4.6.2 100% attributes (completed lot specific traveler; includes Group A Summary)
  - 4.6.3 Burn-In Variables Data and Deltas (if applicable)
  - 4.6.4 Group B2, B3, and B5 Attributes (Variables data, if performed on lot shipping)
  - 4.6.5 Generic Group D data (4.4.3 herein)
  - 4.6.6 SEM photographs (3.13 herein)
  - 4.6.7 Wafer Lot Acceptance Report (3.13 herein)
  - 4.6.8 X-Ray Negatives and Radiographic Report
  - 4.6.9 A copy of outside test laboratory radiation report if ordered
  - 4.6.10 Certificate of Conformance certifying that the devices meet all the requirements of this specification and have successfully completed the mandatory tests and inspections herein.
- Note: Items 4.6.1 and 4.6.10 will be delivered as a minimum, with each shipment. This is noted on the Purchase Order Review Form as "No Charge Data".
- 5.0 Packaging Requirements: Packaging shall be in accordance with Appendix A of MIL-PRF-38535. All devices shall be packaged in conductive material or packaged in anti-static material with an external conductive field shielding barrier.

**(W10) GLASS SEALED FLATPACK / 10LEADS CASE OUTLINE**



NOTES:

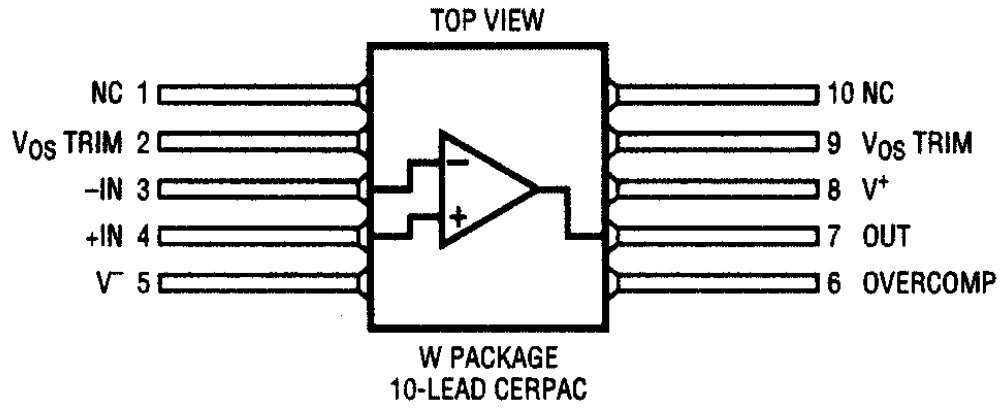
- \*THIS DIMENSION ALLOWS FOR OFF-CENTER LID, MENISCUS AND GLASS OVERRUN
- \*\*INCREASE DIMENSIONS BY 0.003 INCHES (0.076 mm) WHEN LEAD FINISH A IS APPLIED (SOLDER DIPPED)

W10 (GLASS) 0603

$\theta_{ja} = +170^{\circ}\text{C/W}$   
 $\theta_{jc} = +40^{\circ}\text{C/W}$

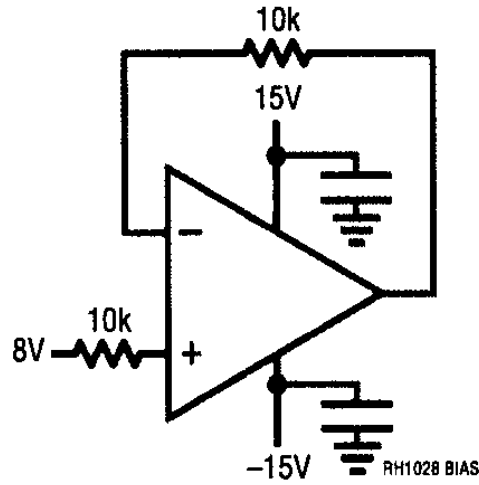
**FIGURE 1**

**TERMINAL CONNECTIONS**



**FIGURE 2**

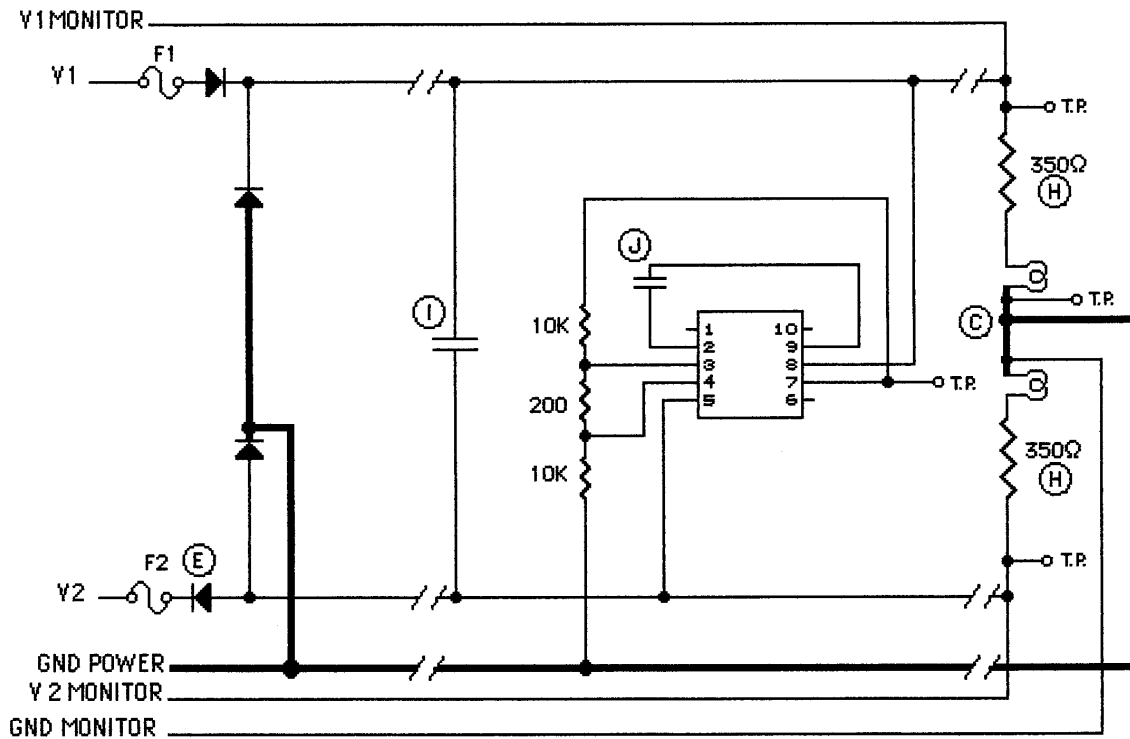
**TOTAL DOSE BIAS CIRCUIT**



**FIGURE 3**

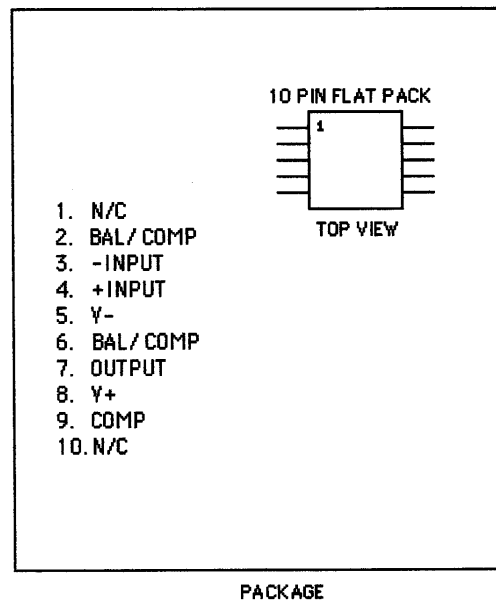


**STATIC BURN-IN CIRCUIT  
GLASS SEALED FLATPACK / 10 LEAD**



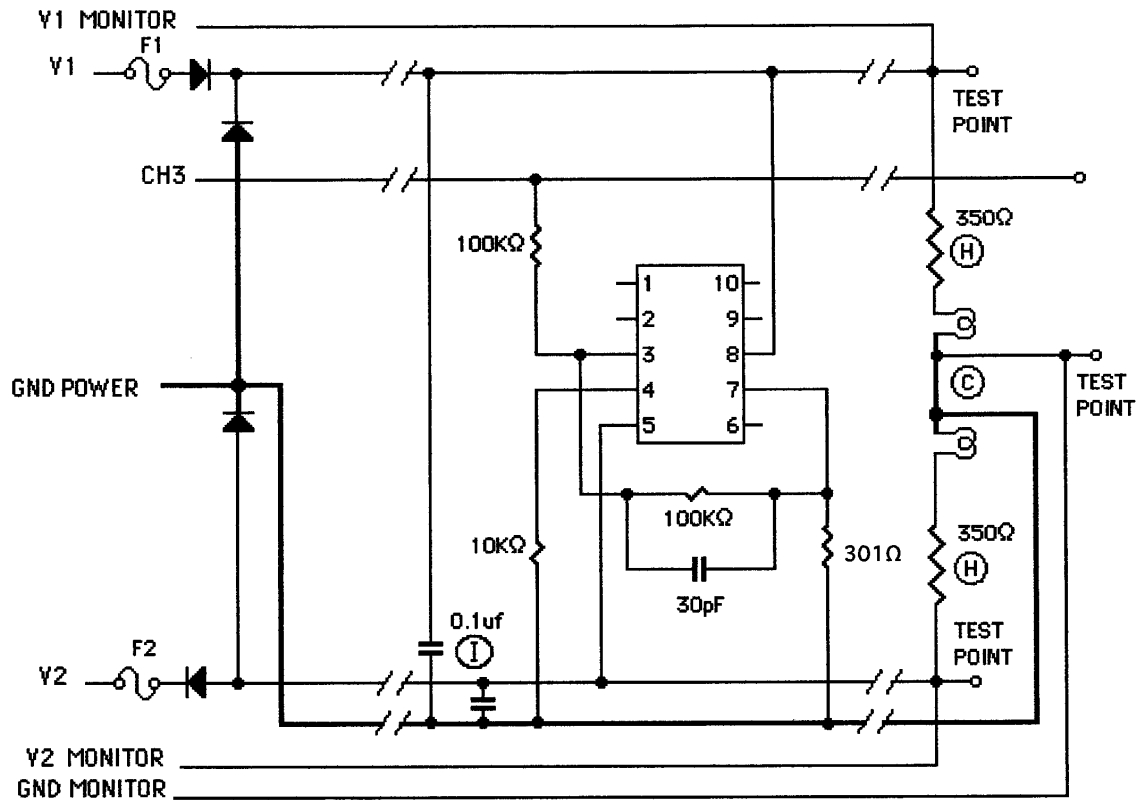
**NOTES:**

1. Unless otherwise specified, component tolerances shall be per military specification.
2.  $T_a = +90^\circ \text{C}$ .
3.  $T_j = +164^\circ \text{C}$  maximum.
4.  $T_c = +136^\circ \text{C}$  minimum.
5. Burn-in Voltages:  $V_1 = +16\text{V}$  to  $+17\text{V}$   
 $V_2 = -16\text{V}$  to  $-17\text{V}$
6. Device current = 12mA.
7. USE ALL OTHER INFORMATION ON # 04-06-0141



**FIGURE 4**

**DYNAMIC BURN-IN CIRCUIT  
GLASS SEALED FLATPACK / 10 LEAD**



NOTES:

1. Unless otherwise specified, component tolerances shall be per military specification.
2.  $T_a = +90^\circ\text{C}$ .
3.  $T_j = +169^\circ\text{C}$  maximum.
4.  $T_c = +140^\circ\text{C}$  minimum.
5. Burn-in Voltages:  $V_1 = +16\text{V to } +17\text{V}$   
 $V_2 = -16\text{V to } -17\text{V}$
6. Device current = 13mA.
7. USE ALL OTHER INFORMATION ON # 04-06-0513

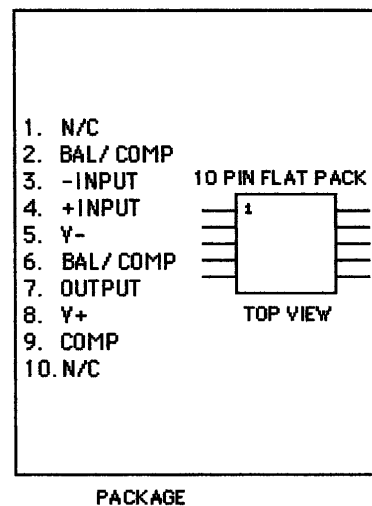
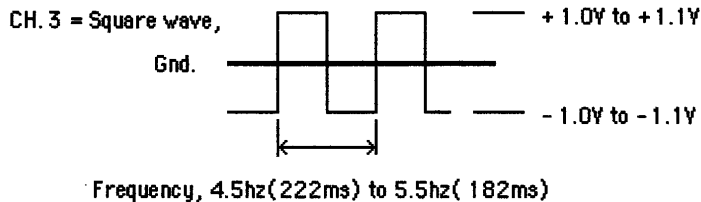


FIGURE 5

**TABLE I: ELECTRICAL CHARACTERISTICS (PRE-IRRADIATION)**

ALL NOTES ON PAGE 12.

**(Preirradiation)  $V_S = \pm 15V$ ,  $V_{CM} = 0V$ , unless otherwise noted.**

SYMBOL	PARAMETER	CONDITIONS	NOTES	$T_A = 25^\circ C$			SUB-GROUP	$-55^\circ C \leq T_A \leq 125^\circ C$			SUB-GROUP	UNITS
				MIN	TYP	MAX		MIN	TYP	MAX		
$V_{OS}$	Input Offset Voltage		2		20	80	1		45	180	2, 3	$\mu V$
$\frac{\Delta V_{OS}}{\Delta Time}$	Long-Term Input Offset Voltage Stability		3		0.3							$\mu V/MO$
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift		8					0.25	1.0			$\mu V/^\circ C$
$I_{OS}$	Input Offset Current	$V_{CM} = 0V$			18	150	1		30	200	2, 3	nA
$I_B$	Input Bias Current	$V_{CM} = 0V$			$\pm 50$	$\pm 400$	1		$\pm 100$	$\pm 600$	2, 3	nA
$e_n$	Input Noise Voltage Density	$f_0 = 10Hz$ $f_0 = 1000Hz$ , 100% Tested	5		1.0	2.5						$nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
$I_n$	Input Noise Current Density	$f_0 = 10Hz$ $f_0 = 1000Hz$ , 100% Tested	4, 6		4.7	24						$pA/\sqrt{Hz}$ $pA/\sqrt{Hz}$

PRE-IRRADIATION CHARACTERISTICS CONTINUED.

**(Preirradiation)  $V_S = \pm 15V$ ,  $V_{CM} = 0V$ , unless otherwise noted.**

SYMBOL	PARAMETER	CONDITIONS	NOTES	$T_A = 25^\circ C$			SUB-GROUP	$-55^\circ C \leq T_A \leq 125^\circ C$			SUB-GROUP	UNITS
				MIN	TYP	MAX		MIN	TYP	MAX		
	Input Resistance Common Mode Differential Mode				300 20							M $\Omega$ k $\Omega$
	Input Capacitance				5							pF
	Input Voltage Range			$\pm 11.0$	$\pm 12.2$			$\pm 10.3$	$\pm 11.7$			V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 11V$ $V_{CM} = \pm 10.3V$		110	126		1	100	120		2, 3	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4V$ to $\pm 16V$ $V_S = \pm 4.5V$ to $\pm 16V$		110	132		1	104	130		2, 3	dB
$A_{VOL}$	Large-Scale Voltage Gain	$R_L \geq 2k$ , $V_O = \pm 10V$ $R_L \geq 1k$ , $V_O = \pm 10V$ $R_L \geq 600\Omega$ , $V_O = \pm 10V$		5.0 3.5 2.0	25 20 15		4	2.0 1.5	14 10		5, 6	V/ $\mu V$ V/ $\mu V$ V/ $\mu V$
$V_{OUT}$	Maximum Output Voltage Swing	$R_L \geq 2k$ $R_L \geq 600\Omega$		$\pm 12.0$ $\pm 10.5$	$\pm 13.0$ $\pm 12.2$		4	$\pm 10.3$	$\pm 11.6$		5, 6	V V
SR	Slew Rate	$A_{VCL} = -1$ (RH1028) $A_{VCL} = -1$ (RH1128)		11.0 4.5	15 6		4					V/ $\mu s$ V/ $\mu s$
GWB	Gain Bandwidth Product	$f_0 = 20kHz$ (RH1028) $f_0 = 200kHz$ (RH1128)	7 7	50 11	75 20							MHz MHz
$Z_O$	Open-Loop Output Impedance	$V_O = 0$ , $I_O = 0$			80							$\Omega$
$I_S$	Supply Current				7.6	10.5	1		9	13	2, 3	mA

**TABLE II: ELECTRICAL CHARACTERISTICS (POST-IRRADIATION)**(Postirradiation)  $V_S = \pm 15V$ ,  $V_{CM} = 0V$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	NOTES	10KRAD(Si)		20KRAD(Si)		50KRAD(Si)		100KRAD(Si)		200KRAD(Si)		UNITS
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$V_{OS}$	Input Offset Voltage		2	100	120	140	160	180						$\mu V$
$I_{OS}$	Input Offset Current			200	200	200	300	500						nA
$I_B$	Input Bias Current			$\pm 600$	$\pm 700$	$\pm 950$	$\pm 1100$	$\pm 1700$						nA
SR	Slew Rate	$A_{VCL} = -1$ (RH1028)		7.5	7.5	7.5	7.5	7.5						$V/\mu s$
		$A_{VCL} = -1$ (RH1128)		3.0	3.0	3.0	3.0	3.0						$V/\mu s$
	Input Voltage Range			$\pm 11$	$\pm 11$	$\pm 11$	$\pm 11$	$\pm 11$						V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 11V$		106	106	106	106	106						dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4V$ to $\pm 18V$		104	104	104	104	104						dB
$A_{VOL}$	Large-Signal Voltage Gain	$R_L \geq 2k$ , $V_O = \pm 10V$		2	2	2	2	2						$V/\mu V$
$V_{OUT}$	Maximum Output Voltage Swing	$R_L \geq 2k$		$\pm 11.5$	$\pm 11.5$	$\pm 11.5$	$\pm 11.5$	$\pm 11.5$						V
		$R_L \geq 600\Omega$		$\pm 10$	$\pm 10$	$\pm 10$	$\pm 10$	$\pm 10$						V

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** Input offset voltage measurements are performed by automatic test equipment approximately 0.5 seconds after application of power. In addition, at  $T_A = 25^\circ C$ , offset voltage is measured with the chip heated to approximately  $55^\circ C$  to account for the chip temperature rise when the device is fully warmed up.

**Note 3:** Long-term input offset voltage stability refers to the average trend line of Offset Voltage vs Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in  $V_{OS}$  during the first 30 days are typically  $2.5\mu V$ .

**Note 4:** This parameter is tested on a sample basis only.

**Note 5:** 10Hz noise voltage density is sample tested on every lot. Devices 100% tested at 10Hz are available on request.

**Note 6:** Current noise is defined and measured with balanced source resistors. The resultant voltage noise (after subtracting the resistor noise on an RMS basis) is divided by the sum of the two source resistors to obtain current noise. Maximum 10Hz current noise can be inferred from 100% testing at 1kHz.

**Note 7:** Gain-bandwidth product is not tested. It is guaranteed by design and by inference from the slew rate measurement.

**Note 8:** This parameter is not 100% tested.

**Note 9:** The inputs are protected by back-to-back diodes. Current-limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds  $\pm 1.8V$ , the input current should be limited to 25mA.

**TABLE III: POST BURN-IN ENDPOINTS AND DELTA LIMIT REQUIREMENTS****T<sub>A</sub> = 25°C, V<sub>CC</sub> = ±15V**

PARAMETER	ENDPOINT LIMIT		DELTA		UNITS
	MIN	MAX	MIN	MAX	
V <sub>OS</sub>	-80	80	-160	160	μV
I <sub>OS</sub>	-150	150	-200	200	nA
I <sub>B</sub>	-400	400	-360	360	nA

**TABLE IV: ELECTRICAL TEST REQUIREMENTS**

MIL-STD-883 TEST REQUIREMENTS	SUBGROUP
FINAL ELECTRICAL TEST REQUIREMENTS (METHOD 5004)	1*, 2, 3, 4, 5
GROUP A TEST REQUIREMENTS (METHOD 5005)	1*, 2, 3, 4, 5
GROUP B** AND D FOR CLASS S ENDPOINT ELECTRICAL PARAMETERS (METHOD 5005)	1, 2, 3

\*PDA APPLIES TO SUBGROUP 1.

**\*\*POST B5 AND B6 25°C LIMITS ARE AS FOLLOWS:**

	SUBGROUP 1	SUBGROUP 2, 3	UNITS
V <sub>OS</sub>	± 240	± 340	μV
I <sub>OS</sub>	± 350	± 400	nA
I <sub>B</sub>	± 760	± 960	nA

PDA TEST NOTE: The PDA is specified as 5% based on failures from Group A, Subgroup 1, tests after cool down as the final electrical test in accordance with method 5004 of MIL-STD-883. The verified failures of Group A, Subgroup 1 and delta rejects after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent for the lot.