

REVISION RECORD

REV	DESCRIPTION	DATE
L	Updated Die Sales table on pg 13.	05/20/15
M	ADD MAXIMUM JUNCTION TEMPERATURE 150°C TO SECTION 3.4 CHANGED CAGE CODE 94155 TO 64155 CHANGED LINEAR TECH FOOTER TO ANALOG DEVICES INC.	08/10/18

1.0 SCOPE:

1.1 This specification defines the performance and test requirements for a microcircuit processed to a space level manufacturing flow.

2.0 APPLICABLE DOCUMENTS:

2.1 Government Specifications and Standards: the following documents listed in the Department of Defense Index of Specifications and Standards, of the issue in effect on the date of solicitation, form a part of this specification to the extent specified herein.

SPECIFICATIONS:

- MIL-PRF-38535 Integrated Circuits (Microcircuits) Manufacturing, General Specification for
- MIL-STD-883 Test Method and Procedures for Microcircuits
- MIL-STD-1835 Microcircuits Case Outlines

2.2 Order of Precedence: In the event of a conflict between the documents referenced herein and the contents of this specification, the order of precedence shall be this specification, MIL-PRF-38535 and other referenced specifications.

3.0 REQUIREMENTS:

3.1 General Description: This specification details the requirements for the RH1021C-5 Precision 5V Reference Dice and Element Evaluation Test Samples, processed to space level manufacturing flow as specified herein.

3.2 Part Number: **RH1021C-5 Dice**

3.3 Special Handling of Dice: Rad Hard dice require special handling as compared to standard IC dice. Rad Hard dice are susceptible to surface damage due to the absence of silicon nitride passivation that is present on most standard dice. Silicon nitride protects the dice surface from scratches by its hard and dense properties. The passivation on Linear Technology’s Rad Hard dice is silicon dioxide which is much “softer” than silicon nitride. During the visual and preparation for shipment, ESD safe Tweezers are used and only the edge of the die are touched.

LTC recommends that dice handling be performed with extreme care so as to protect the die surface from scratches. If the need arises to move the die in or out of the chip shipment tray (waffle pack), use an ESD-Safe-Plastic-tipped Bent Metal Vacuum Probe, preferably .020” OD x .010” ID (for use with tiny parts). The wand should be compatible with continuous air vacuums. The tip material should be static dissipative Delrin (or equivalent) plastic.

During die attach, care must be exercised to ensure no tweezers, or other equipment, touch the top of the dice.

3.4 The Absolute Maximum Ratings:

Input Voltage	40V
Input-Output Voltage Differential	35V
Output to Ground Voltage	
(Sink Mode Current Limit)	10V
Trim Pin to Ground Voltage	

Positive	Equal to V_{OUT}
Negative	-20V
Output Short Circuit Duration		
$V_{IN} = 35V$	10 sec
$V_{IN} = \leq 20V$	Indefinite
Operating Temperature Range	-55°C to 125°C
Maximum Junction Temperature	! ! ! ! ! ! ! ! ! !	150°C
Storage Temperature Range	-65°C to 150°C

NOTE: Absolute maximum ratings are those values beyond which the life of a device may be impaired.

- 3.5 **Design, Construction, and Physical Dimensions:** Detail design, construction, physical dimensions, and electrical requirements shall be specified herein.
- 3.6 **Outline Dimensions and Pad Functions:** Dice outline dimensions, pad functions, and locations shall be specified in **Figure 1**.
- 3.7 **Radiation Hardness Assurance (RHA):**
- 3.7.1 The manufacturer shall perform a lot sample test as an internal process monitor for total dose radiation tolerance. The sample test is performed with MIL-STD-883 TM1019 Condition A as a guideline.
- 3.7.2 For guaranteed radiation performance to MIL-STD-883, Method 1019, total dose irradiation, the manufacturer will provide certified RAD testing and report through an independent test laboratory when required as a customer purchase order line item.
- 3.7.3 Total dose bias circuit is specified in **Figure 2**.
- 3.8 **Wafer (or Dice) Probe:** Dice shall be 100% probed at $T_a = +25^\circ\text{C}$ to the limits shown in **Table I** herein. All reject dice shall be removed from the lot. This testing is normally performed prior to dicing the wafer into chips. Final specifications after assembly are sample tested during the element evaluation.
- 3.9 **Wafer Lot Acceptance:** Wafer lot acceptance shall be in accordance with MIL-PRF-38535, Appendix A, except for the following: Top side glassivation thickness shall be a **minimum of 4KÅ**.
- 3.10 **Wafer Lot Acceptance Report:** SEM is performed per MIL-STD-883, Method 2018. Copies of SEM photographs shall be supplied with the Wafer Lot Acceptance Report as part of a Space Data Pack when specified as a customer purchase order line item.
- 3.11 **Traceability:** Wafer Diffusion Lot and Wafer traceability shall be maintained through Quality Conformance Inspection.
- 4.0 **QUALITY CONFORMANCE INSPECTION:** Quality Conformance Inspection shall consist of the tests and inspections specified herein.
- 5.0 **SAMPLE ELEMENT EVALUATION:** A sample from **each wafer supplying dice** shall be assembled and subjected to element evaluation per **Table III** herein.
- 5.1 **100 Percent Visual Inspection:** All dice supplied to this specification shall be inspected in accordance with MIL-STD-883, Method 2010, Condition A. All reject dice shall be removed from the lot.
- 5.2 **Electrical Performance Characteristics for Element Evaluation:** The electrical performance characteristics shall be as specified in **Table I** and **Table II** herein.

- 5.3 Sample Testing: Each wafer supplying dice for delivery to this specification shall be subjected to element evaluation sample testing. No dice shall be delivered until all the lot sample testing has been performed and the results found to be acceptable unless the customer supplies a written approval for shipment prior to completion of wafer qualification as specified in this specification.
- 5.4 Part Marking of Element Evaluation Sample Includes:
- 5.4.1 LTC Logo
 - 5.4.2 LTC Part Number
 - 5.4.3 Date Code
 - 5.4.4 Serial Number
 - 5.4.5 ESD Identifier per MIL-PRF-38535, Appendix A
 - 5.4.6 Diffusion Lot Number
 - 5.4.7 Wafer Number
- 5.5 Burn-In Requirement: Burn-In circuit for TO5 package is specified in **Figure 3**.
- 5.6 Mechanical/Packaging Requirements: Case Outline and Dimensions are in accordance with **Figure 4**.
- 5.7 Terminal Connections: The terminal connections shall be as specified in **Figure 5**.
- 5.8 Lead Material and Finish: The lead material and finish shall be Kovar with hot solder dip (Finish letter A) in accordance with MIL-PRF-38535.
- 6.0 VERIFICATION (QUALITY ASSURANCE PROVISIONS)
- 6.1 Quality Assurance Provisions: Quality Assurance provisions shall be in accordance with MIL-PRF-38535. Linear Technology is a QML certified company and all Rad Hard candidates are assembled on qualified Class S manufacturing lines.
- 6.2 Sampling and Inspection: Sampling and Inspection shall be in accordance with **Table III** herein.
- 6.3 Screening: Screening requirements shall be in accordance with **Table III** herein.
- 6.4 Source Inspection:
- 6.4.1 The manufacturer will coordinate Source Inspection at wafer lot acceptance and pre-seal internal visual.
 - 6.4.2 The procuring activity has the right to perform source inspection at the supplier's facility prior to shipment for each lot of deliverables when specified as a customer purchase order line item. This may include wafer lot acceptance, die visual, and final data review.
- 6.5 Deliverable Data: Deliverable data that will ship with devices when a Space Data Pack is ordered:

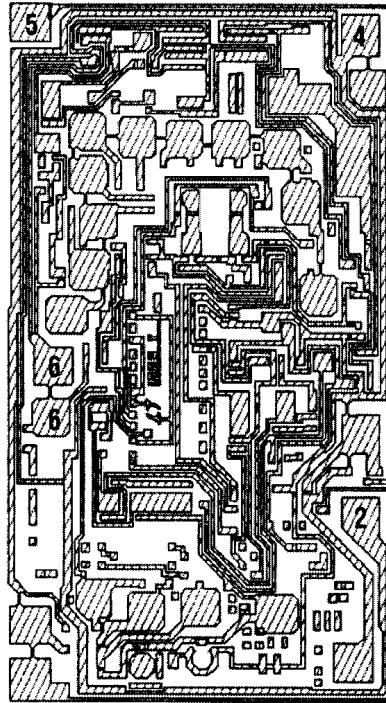
- 6.5.1 Lot Serial Number Sheets identifying all Canned Sample devices accepted through final inspection by serial number.
- 6.5.2 100% attributes (completed element evaluation traveler).
- 6.5.3 Element Evaluation variables data, including Burn-In and Op Life
- 6.5.4 SEM photographs (3.10 herein)
- 6.5.5 Wafer Lot Acceptance Report (3.9 herein)
- 6.5.6 A copy of outside test laboratory radiation report if ordered
- 6.5.7 Certificate of Conformance certifying that the devices meet all the requirements of this specification and have successfully completed the mandatory tests and inspections herein.

Note: Items 6.5.1 and 6.5.7 will be delivered as a minimum, with each shipment.

- 7.0 Packaging Requirements: Packaging shall be in accordance with Appendix A of MIL-PRF-38535. All dice shall be packaged in multicavity containers composed of conductive, anti-static, or static dissipative material with an external conductive field shielding barrier.

DICE OUTLINE DIMENSIONS AND PAD FUNCTIONS

RH1021C-5



94 × 55 mils

PAD FUNCTION

- 2. Input
- 4. Ground
- 5. Trim
- 6. Output

FIGURE 1

TOTAL DOSE BIAS CIRCUIT

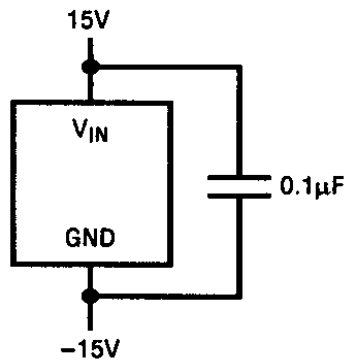
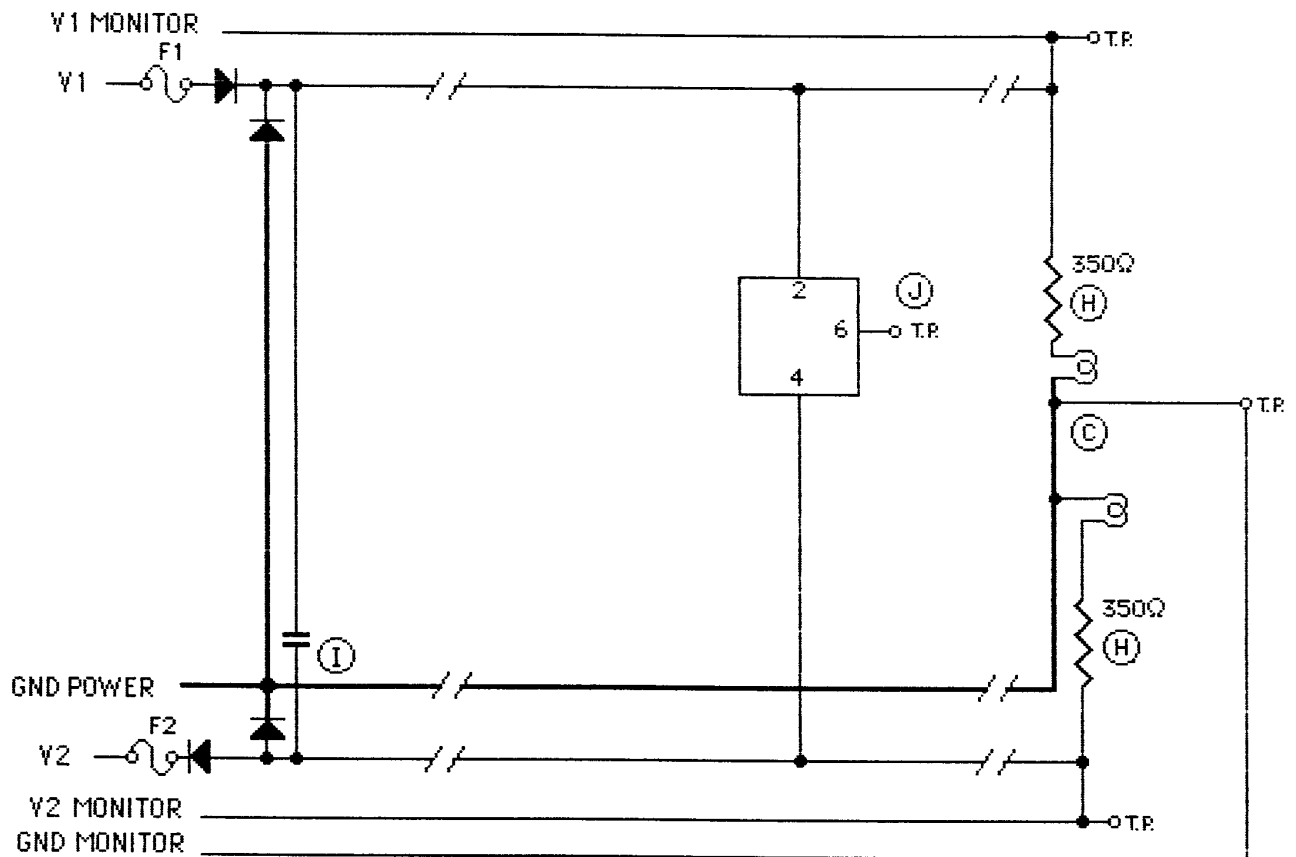


FIGURE 2

BURN-IN CIRCUIT

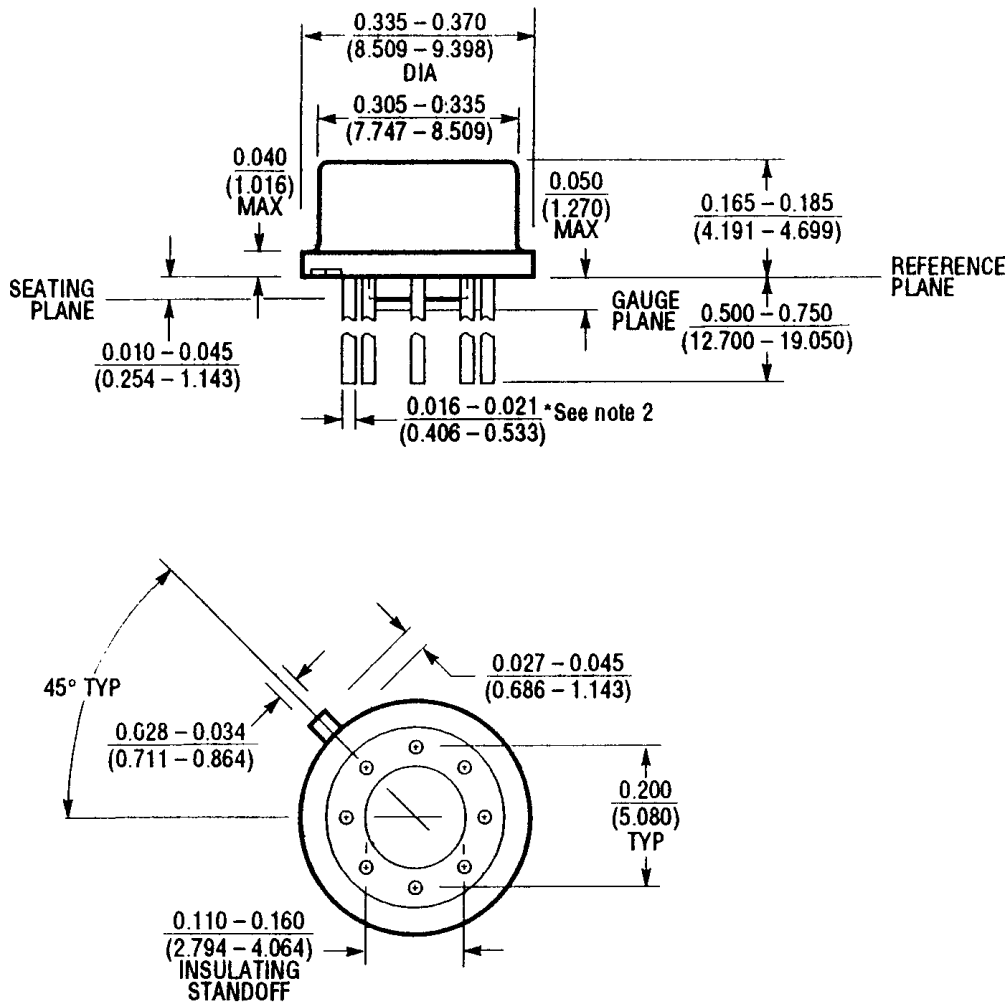


NOTES:

1. Unless otherwise specified, component tolerances shall be per military specification.
2. $T_j = 168^\circ\text{C}$ maximum.
3. $T_a = 150^\circ\text{C}$.
4. Burn-in Voltages: $V_1 = +20\text{V to } +22\text{V}$
 $V_2 = -20\text{V to } -22\text{V}$

FIGURE 3

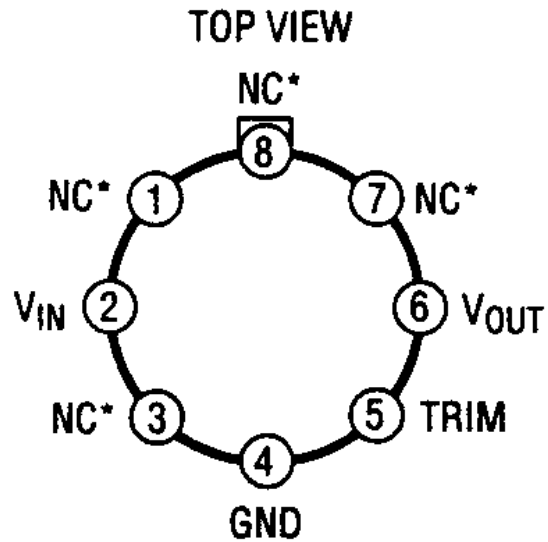
TO5, 8 LEADS, CASE OUTLINE



- NOTE: 1. LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND SEATING PLANE.
 2. FOR SOLDER DIP LEAD FINISH, LEAD DIAMETER IS $0.016 - 0.024$ (0.406 - 0.610)

FIGURE 4

$\theta_{ja} = +150^\circ\text{C/W}$
 $\theta_{jc} = +40^\circ\text{C/W}$

TERMINAL CONNECTIONS

H PACKAGE
8-LEAD TO-5 METAL CAN

* CONNECTED INTERNALLY.
DO NOT CONNECT EXTERNAL
CIRCUITRY TO THESE PINS.

FIGURE 5

TABLE I DICE ELECTRICAL CHARACTERISTICS – Element Evaluation (Note 3) $V_S = 10V$, $I_{OUT} = 0$, $T_A = 25^\circ C$ unless otherwise noted.

PARAMETER	CONDITIONS	RH1021C-5		UNITS
		MIN	MAX	
Output Voltage (Note 1)	RH1021C-5	4.9975	5.0025	V
Line Regulation (Note 2)	$7.2V \leq V_{IN} \leq 10V$ $10V \leq V_{IN} \leq 40V$		12 6	ppm/V ppm/V
Load Regulation (Sourcing Current)	$0 \leq I_{OUT} \leq 10mA$ (Note 2)		440	ppm/mA
Load Regulation (Sinking Current)	$0 \leq I_{OUT} \leq 10mA$ (Note 2)		440	ppm/mA
Supply Current			1.2	mA

Note 1: Output voltage is measured immediately after turn-on. Changes due to chip warm-up are typically less than 0.005%.

Note 2: Line and load regulation are measured on a pulse basis. Output changes due to die temperature change must be taken into account separately.

Note 3: Dice are probe tested at $25^\circ C$ to the limits shown. Final specs after assembly are sample tested during the element evaluation. Refer to the standard RH1021-5 Data Sheet for absolute maximum rating, performance curves, typical specifications, and finished product specifications.

TABLE II ELECTRICAL CHARACTERISTICS – Post-Irradiation (Note 6)

SYMBOL	PARAMETER	CONDITIONS	NOTES	10Krad(Si)		20Krad(Si)		50Krad(Si)		100Krad(Si)		200Krad(Si)		UNITS
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OUT}	Output Voltage	RH1021CM-5	1	4.9945	5.0055	4.993	5.007	4.991	5.009	4.9875	5.0125	4.984	5.016	V
		RH1021BM-5, DM-5	1	4.95	5.05	4.945	5.055	4.942	5.058	4.94	5.06	4.935	5.065	V
TCV_{OUT}	Output Voltage Temperature Coefficient	RH1021BM-5	2		5		5		5		7		10	ppm/ $^\circ C$
		RH1021CM-5, DM-5	2		20		20		20		22		25	ppm/ $^\circ C$
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	$7.2V \leq V_{IN} \leq 10V$	3		12		12		13.5		15		18	ppm/V
		$10V \leq V_{IN} \leq 40V$	3		6		6		6		7		9	ppm/V
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation (Sourcing Current)	$0 \leq I_{OUT} \leq 10mA$	3,7		20		20		20		20		20	ppm/mA
		$0 \leq I_{OUT} \leq 10mA$	3		100		100		100		100		150	ppm/mA
I_S	Supply Current				1.2		1.2		1.2		1.2		1.2	mA

Note 1: Output voltage is measured immediately after turn-on. Changes due to chip warm-up are typically less than 0.005%.

Note 2: Temperature coefficient is measured by dividing the change in output voltage over the temperature range by the change in temperature. Separate tests are done for hot and cold; T_{MIN} to $25^\circ C$ and $25^\circ C$ to T_{MAX} . Incremental slope is also measured at $25^\circ C$.

Note 3: Line and load regulation are measured on a pulse basis. Output change due to die temperature change must be taken into account separately. Package thermal resistance is $150^\circ C/W$ for the TO-5 (H) package and $170^\circ C/W$ for the 10-lead flatpack (W) package.

Note 6: $V_{IN} = 10V$, $I_{OUT} = 0$, $T_A = 25^\circ C$, unless otherwise noted.

Note 7: $I_{OUT(MAX)}$ (Sourcing) is 5mA for exposures greater than 100Krad (Si).



RH CANNED SAMPLE TABLE FOR QUALIFYING DICE SALES

SUBGROUP	CLASS			OPERATION	MIL-STD-883		QUANTITY (ACCEPT NUMBER) REF: METHOD 2018 FOR S/S
	K/S	V	H/B		METHOD	CONDITION	
1	X	X		SEM	2018	N/A	100%
2	X	X	X	ELEMENT ELECTRICAL (WAEER SORT @ 25°C)			100%
3	X	X	X	ELEMENT VISUAL (2nd OP)	2010	A	100%
4	X	X	X	INTERNAL VISUAL (3rd OP)	2010	A	ASSEMBLED PARTS ONLY
	X	X		DIE SHEAR MONITOR	2019		
5	X	X		BOND PULL MONITOR	2011		ASSEMBLED PARTS ONLY
	X	X		STABILIZATION BAKE	1008	C	
	X	X		TEMPERATURE CYCLE	1010	C	
	X	X		CONSTANT ACCELERATION	2001	E	
	X	X		FINE LEAK	1014	A	
6	X	X		GROSS LEAK	1014	C	45(0)
	X	X		FIRST ROOM ELECTRICAL - READ & RECORD (REPLACE ANY ASSEMBLY-RELATED REJECTS)			
	X	X		PRE BURN-IN ELECT. READ & RECORD @ +125°C or +150°C, -55°C			
	X	X		BURN-IN: +125°C/240 hrs. or +150°C/120 hrs	1015	+ 125°C MINIMUM 240 HOURS	
	X	X		POST BURN-IN ELECT. READ & RECORD @ 25°C			
	X	X		POST BURN-IN ELECT. READ & RECORD @ +125°C or +150°C, -55°C			
7	X	X		TOTAL IRRADIATION DOSE	1019	A	15(0) OR 25(1) - # of wires
	X	X		PRE OP-LIFE ELECTRICAL @ 25°C READ & RECORD			
	X	X		OPERATING LIFE: +125°C/1000 hrs. or +150°C/500 hrs.	1005	+ 125°C MINIMUM 1000 HOURS	
	X	X		POST OP-LIFE ELECT. (R & R @ 25°C, +125°C DR +150°C, -55°C WIRE BOND EVALUATION	2011		

NOTE: LTC is not qualified to process to MIL-PRF-38534. This is an LTC imposed element evaluation that follows MIL-STD-883 test methods and conditions. Please note the quantity and accept number from Sample Size Series of 5%, accept on 0, and note that the actual sample and accept number does not begin until Subgroup 6 OP-LIFE.

NOTE: Tests within Subgroup 5 may be performed in any sequence.

NOTE: LTC's radiation tolerance (RH) die has a topside glassivation thickness of 4KA minimum.

NOTE: Sample sizes on the travelers may be larger than that indicated in the above table; however, the larger sample size is to accommodate extra units for replacement devices in the event of equipment or operator error and for assembly related rejects in Subgroup 6, and for Wire Bond Evaluation, Subgroup 7. The larger sample size is at all times kept segregated and, if used for qualification, has all the required processing imposed.