

REVISION RECORD

REV	DESCRIPTION	DATE
0	INITIAL RELEASE	06/12/96
A	<ul style="list-style-type: none"> PAGE 2, ADDED PARAGRAPHS 3.2.1 AND 3.2.2 TO IDENTIFY "01" AND "02" AS PACKAGE OPTIONS. CHANGED THE PART NUMBER FROM "RH1014MWB14 TO "RH1014MWB". PAGE 5, PARAGRAPH 5.6.10, NOTE – CORRECTED TYPO ON ITEM PARAGRAPH NUMBER FROM "4.6.1" TO "5.6.1" AND "4.6.10" TO "5.6.10". PAGE 6 AND 7 – ADDED θ_{ja} AND θ_{jc}, T_j MAX TO CASE OUTLINES. CHANGED THE "WB14" TO "WB" ON FIGURE 2 CASE OUTLINE. PAGE 8 – CHANGED TERMINAL CONNECTIONS DWG FOR "WB" PACKAGE, OPTION 2. 	05/12/97
B	<ul style="list-style-type: none"> PAGE 4, PARAGRAPH 5.4.2, GROUP B INSPECTION WAS REDEFINED. PARAGRAPH 5.4.3, GROUP D INSPECTION WAS REDEFINED. PARAGRAPH 5.5.1, SOURCE INSPECTION WAS REDEFINED. PAGE 8, FIGURE 4 – CORRECTED TYPO ON PIN 11 CONNECTION: SHOULD BE "V". 	10/08/97
C	<ul style="list-style-type: none"> PAGE 2, PARAGRAPH 3.2.2 – CHANGED PACKAGE TYPE FROM 14 LEAD BOTTOM BRAZED FLATPACK TO 14 LEAD FLATPACK, GLASS SEAL. PAGE 3, ADDED PARAGRAPH 3.8.1 AND 3.8.2 PAGE 7, FIGURE 2, PAGE 8, FIGURE 4, PAGE 11, FIGURE 7, PAGE 12, FIGURE 8, CHANGED PACKAGE TYPE FROM 14 LEAD BOTTOM BRAZED FLATPACK TO 14 LEAD CERPAK. 	11/25/97
D	<ul style="list-style-type: none"> PAGE 16, CHANGED VOS MIN DELTA LIMIT FROM $-60 \mu V$ TO $-200 \mu V$, AND CHANGED VOS MAX DELTA LIMIT FROM $60 \mu V$ TO $200 \mu V$. 	12/18/97
E	<ul style="list-style-type: none"> PAGE 2, WAS ADDED TO ACCOMMODATE REVISION RECORD. PAGE 4, CORRECTED OPTION NUMBER FROM "02" to "01", PARA 3.8.1 AND CORRECTED OPTION NUMBER FROM "03" TO "02", PARA 3.8.2. PAGE 5, AMENDED PARAGRAPHS 4.1 AND 4.1.1. TAKING EXCEPTION TO ANALYSIS OF CATASTROPHIC FAILURES. 	03/13/98
F	<ul style="list-style-type: none"> PAGE 17, CHANGED DELTA LIMITS ON +IB FROM -3 AND 3 TO -4 AND 4. CHANGED DELTA LIMITS ON -IB FROM -3 AND 3 TO -4 AND 4. 	05/15/98
G	<ul style="list-style-type: none"> PAGE 8, CORRECTED PACKAGE OUTLINE DRAWING FOR FIGURE 2 CASE OUTLINE, (W) FLAT PACK 14 LEAD GLASS SEAL. 	01/11/99
H	<ul style="list-style-type: none"> PAGE 7, 8, FIGURE 1, 2, CHANGED θ_{ja} AND θ_{jc}. 	09/29/99
J	<ul style="list-style-type: none"> PAGE 3, PARAGRAPH 3.2.1, 3.2.2, HAD FIGURES 1 AND 2 REMOVED. PAGE 4, PARAGRAPH 3.7 CHANGED VERBIAGE FROM "SPECIFIED IN TABLE III" TO "AND AS SPECIFIED IN TABLE III HEREIN", LINE 2. PARAGRAPH 3.9, ADDED "HEREIN" AFTER "TABLE II", LINE 2. PAGE 5, PARAGRAPH 4.3, ADDED "HEREIN" AFTER "TABLE III", LINE 2. PARAGRAPH 4.4.1, ADDED "HEREIN" AFTER "TABLE II", LINE 2. 	11/17/99

CONTINUED ON NEXT PAGE...

REVISION RECORD AND DESCRIPTION CONTINUED ON NEXT PAGE.

CAUTION: ELECTROSTATIC DISCHARGE SENSITIVE PART

REVISION	PAGE NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
INDEX	REVISION	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V
REVISION	PAGE NO.	18																
INDEX	REVISION	V																
	ORIG																	
	DSGN																	
	ENGR																	
	MFG																	
	CM																	
	QA																	
	PROG									SIZE	CAGE	DRAWING						
	FUNCT										CODE	NUMBER						REV
											64155	05-08-5014						V
APPLICATION							SIGNOFFS	DATE	CONTRACT:									

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REVISION RECORD		
REV	DESCRIPTION	DATE
J	<p>PARAGRAPH 4.4.2.2, CHANGED VERBIAGE I LINE 1 FROM "ALL FOOTNOTES OF TABLE IIA OF MIL-STD-883" TO "ALL FOOTNOTES PERTAINING TO TABLE IIA IN MIL-STD-883".</p> <p>PARAGRAPH 4.4.3.2, CHANGED VERBIAGE IN LINE 1 FROM "ALL FOOTNOTES OF TABLE IV OF MIL-STD-883" TO "ALL FOOTNOTES PERTAINING TO TABLE IV IN MIL-STD-883".</p>	11/17/99
K	<ul style="list-style-type: none"> PAGE 8, CHANGED THETA JA TO $\theta_{JA}=160^{\circ}\text{C/W}$ AND THETA JC TO $\theta_{JC}=40^{\circ}\text{C/W}$ FROM $\theta_{JA}=160^{\circ}\text{C/W}$, $\theta_{JC}=40^{\circ}\text{C/W}$. 	08/30/00
L	<ul style="list-style-type: none"> CORRECTION TO REVISION K, REVISION RECORD. SHOULD BE PAGE 8, CHANGED THETA JA TO $\theta_{JA}=160^{\circ}\text{C/W}$ AND THETA JC TO $\theta_{JC}=40^{\circ}\text{C/W}$ FROM $\theta_{JA}=165^{\circ}\text{C/W}$, $\theta_{JC}=13^{\circ}\text{C/W}$. ADDED PAGE 3 WAS ADDED TO ACCOMMODATE REVISION RECORDS. CONVERSION FROM WORD PERFECT TO MICROSOFT WORD. REDUCED SPEC PAGES TO 14 TOTAL. PAGE 4: PARAGRAPH 3.2.1 AND 3.2.2, ADDED THE WORD "OPTION" PRECEDING THE NUMBER OF EACH LTC PART NUMBER FOR BETTER CUSTOMER ORDERING CONVENIENCE. PAGE 5: PARAGRAPH 3.6, CHANGED "TABLE IA" TO "TABLE II". PARAGRAPH 3.7, CHANGED "TABLE III" TO "TABLE IV". PARAGRAPHS 3.8.1 AND 3.8.2, ADDED THE PACKAGE TYPES AND OPTIONS AFTER EACH FIGURE. PARAGRAPH 3.9, CHANGED "TABLE II" TO "TABLE III". PARAGRAPHS 3.10.1 AND 3.10.2, ADDED THE PACKAGE TYPES AFTER EACH FIGURE. PARAGRAPHS 3.10.3, REMOVED REFERENCE TO GOLD PLATED (WB) PACKAGE. PARAGRAPH 3.11.1 WAS CHANGED FROM "...dosage rate of approximately 20 Rads per second" TO "...dosage rate of less than or equal to 10 Rads per second". PAGE 6: PARAGRAPHS 4.1 THROUGH 4.4.2.1 CHANGES WERE DONE TO CLARIFY GROUP SAMPLING. PAGE 7: PARAGRAPH 4.4.3 CHANGE WAS DONE TO CLARIFY GROUP SAMPLING. PARAGRAPHS 4.5 THROUGH 4.5.2, CHANGED PARAGRAPH NUMBERS FROM "5.0" TO "4.5". PARAGRAPHS 4.6 THROUGH 4.6.10, CHANGED PARAGRAPH NUMBERS FROM "6.0" TO "4.6 THROUGH "4.6.10" PARAGRAPHS 4.6.2 THROUGH 4.6.4 WERE RE-WRITTEN. THESE DATA PROVIDED, AND DATA AVAILABLE. PARAGRAPH 4.6.10 NOTE, ADDED FURTHER EXPLANATION OF MINIMUM DELIVERED DATA. 	03/26/02

REVISION RECORD		
REV	DESCRIPTION	DATE
L	<ul style="list-style-type: none"> PARAGRAPH 5.Ø CHANGED PARAGRAPH NUMBER FROM “7.Ø” TO “5.Ø”. PAGES 8 THROUGH 15, ALL FIGURE TITLES CHANGED TO HAVE DEVICE OPTIONS AND PACKAGE TYPES AT TOP OF PAGE, AND HAVE ALL FIGURES AT BOTTOM OF PAGE. PAGE 12, NOTE 2 WAS CHANGED FROM 171°C TO +152°C, NOTE 3 WAS CHANGED FROM 150°C TO +125°C, NOTE 4 HAD A FREQUENCY LIMIT ADDED, NOTES 5 AND 6 WERE DELETED AND REPLACE WITH A NEW NOTE 5. PAGES 16 THROUGH 18, SCANNED DIRECTLY FROM DATA SHEET. 	3/26/02
M	<p>PAGE 1:</p> <ul style="list-style-type: none"> CORRECTED THE CAGE CODE NUMBER FROM 94155 TO 64155. <p>PAGE 9:</p> <ul style="list-style-type: none"> CORRECTED OPTION 2, FIGURE 2 HEADER, CASE OUTLINE, FROM W10 GLASS SEALED FLATPACK / 10 LEADS CASE OUTLINE TO W14 GLASS SEALED FLATPACK / 14 LEADS CASE OUTLINE. <p>PAGE 10:</p> <ul style="list-style-type: none"> CORRECTED OPTION 2, FIGURE 4, TERMINAL CONNECTION, FROM WB PACKAGE 14-LEAD METAL SEALED BOTTOM BRAZED TO W PACKAGE 14 LEAD FLATPACK GLASS SEALED. 	5/30/02
N	<p>PAGE 5:</p> <ul style="list-style-type: none"> CHANGED INITIAL RATE OF RADS TO 240 RADS/SEC. 	3/16/05
P	<ul style="list-style-type: none"> PAGE 6, CHANGED IN BOTH PARAGRAPHS 4.2, 4.3 IN CONJUNCTION TO 3.3 CHANGED TO 3.4 AND PARAGRAPH 4.3 CHANGED 3.1.1 TO 3.1 AND 3.2.1 TO 3.1.1 	12/10/07
R	<ul style="list-style-type: none"> PAGE 5, PARAGRAPH 3.103 CHANGED TO ALLOY 42 PACKAGE REQUIREMENT. PARAGRAPH 3.11.1 CHANGED VERBIAGE. 	05/01/08
S	<ul style="list-style-type: none"> PAGE 5, ADDED PARAGRAPH 3.10 FOR 60 TEMP. CYCLES AT EOL. REST OF THE PARAGRAPHS WERE RE-NUMBERED. 	02/12/09
T	<ul style="list-style-type: none"> PAGE 12, CORRECTED BURN-IN NEGATAIVE VOLTAGE FROM V1 TO V2. 	03/08/12
U	<ul style="list-style-type: none"> Changed the $+I_B$ and $-I_B$ ‘Max Endpoint Limit’ from 0 to +30 on page 18. 	08/28/13
V	<p>Removed & replace figure 2 package drawing on pg 9</p>	12/13/16

1.0 SCOPE:

- 1.1 This specification defines the performance and test requirements for a microcircuit processed to a space level manufacturing flow.

2.0 APPLICABLE DOCUMENTS:

- 2.1 Government Specifications and Standards: the following documents listed in the Department of Defense Index of Specifications and Standards, of the issue in effect on the date of solicitation, form a part of this specification to the extent specified herein.

SPECIFICATIONS:

MIL-PRF-38535 Integrated Circuits (Microcircuits) Manufacturing, General Specification for

MIL-STD-883 Test Method and Procedures for Microcircuits

MIL-STD-1835 Microcircuits Case Outlines

- 2.2 Order of Precedence: In the event of a conflict between the documents referenced herein and the contents of this specification, the order of precedence shall be this specification, MIL-PRF-38535 and other referenced specifications.

3.0 REQUIREMENTS:

- 3.1 General Description: This specification details the requirements for the RH1014, Operational Amplifier, processed to space level manufacturing flow.

3.2 Part Number:

3.2.1 Option 1 – RH1014MJ (CERDIP, 14 LEAD)

3.2.2 Option 2 – RH1014MW (FLATPACK, GLASS SEAL, 14 LEAD)

3.3 Part Marking Includes:

3.3.1 LTC Logo

3.3.2 LTC Part Number (See Paragraph 3.2)

3.3.3 Date Code

3.3.4 Serial Number

3.3.5 ESD Identifier per MIL-PRF-38535, Appendix A

3.4 The Absolute Maximum Ratings:

Supply Voltage	±22V
Differential Input Voltage	±30V
Input Voltage	Equal to Positive Supply Voltage 5V Below Negative Supply Voltage
Output Short Circuit Duration <u>1/</u>	Indefinite
Operating Temperature Range	-55°C to 125°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

1/ Parameter is guaranteed by design, characterization, or correlation to other tested parameters.

3.5 Electrostatic discharge sensitivity, ESDS, shall be Class 1.

3.6 Electrical Performance Characteristics: The electrical performance characteristics shall be as specified in Table I and Table II.

3.7 Electrical Test Requirements: Screening requirements shall be in accordance with 4.1 herein, MIL-STD-883, Method 5004, and as specified in Table IV herein.

3.8 Burn-In Requirement:

3.8.1 Option 1 (Ceramic Dip) Static Burn-In, Figure 5; Dynamic Burn-In, Figure 6.

3.8.2 Option 2 (Glass Sealed Flatpack) : Static Burn-In, Figure 7; Dynamic Burn-In, Figure 8.

3.9 Delta Limit Requirement: Delta limit parameters are specified in Table III herein, are calculated after each burn-in, and the delta rejects are included in the PDA calculation.

3.10 Part Number Option 2: The manufacturer performs 60 Temperature Cycles per MIL-STD-883, TM1010, Condition C at end of line testing.

3.11 Design, Construction, and Physical Dimensions: Detail design, construction, physical dimensions, and electrical requirements shall be specified herein.

3.11.1 Mechanical / Packaging Requirements: Case outlines and dimensions are in accordance with Figure 1 (Ceramic Dip/14 Leads) and Figure 2 (Glass Sealed Flatpack/14 Leads).

3.11.2 Terminal Connections: The terminal connections shall be as specified in Figure 3 (Ceramic Dip/14 Leads) and Figure 4 (Glass Sealed Flatpack/14 Leads).

3.11.3 Lead Material and Finish: The lead material shall be Alloy 42 for option 1, 2. The lead finishes shall be hot solder dip (Finish letter A) in accordance with MIL-PRF-38535.

3.12 Radiation Hardness Assurance (RHA):

3.12.1 The manufacturer shall perform a lot sample test as an internal process monitor for total dose radiation tolerance. The sample test is performed with MIL-STD-883 TM1019 Condition A as a guideline.

3.12.2 For guaranteed radiation performance to MIL-STD-883, Method 1019, total dose irradiation, the manufacturer will provide certified RAD testing and report through an independent test laboratory when required as a customer purchase order line item.

3.12.3 Total dose bias circuit is specified in Figure 9.

3.13 Wafer Lot Acceptance: Wafer lot acceptance shall be in accordance with MIL-PRF-38535, Appendix A, except for the following: Topside glassivation thickness shall be a minimum of 4KÅ.

3.14 Wafer Lot Acceptance Report: SEM is performed per MIL-STD-883, Method 2018 and copies of SEM photographs shall be supplied with the Wafer Lot Acceptance Report as part of a Space Data Pack when specified as a customer purchase order line item.

4.0 VERIFICATION (QUALITY ASSURANCE PROVISIONS)

4.1 Quality Assurance Provisions: Quality Assurance provisions shall be in accordance with MIL-PRF-38535. Linear Technology is a QML certified company and all Rad Hard candidates are assembled on qualified Class S manufacturing lines.

4.2 Sampling and Inspection: Sampling and Inspection shall be in accordance with MIL-STD-883, Method 5005 with QML allowed and TRB approved deviations in conjunction with paragraphs 3.1.1, 3.2.1, and 3.4 of the test method.

4.3 Screening: Screening requirements shall be in accordance with MIL-STD-883, Method 5004 with QML allowed and TRB approved deviations in conjunction with paragraphs 3.1, 3.1.1, and 3.4 of the test method. Electrical testing shall be as specified in Table IV herein.

4.3.1 Analysis of catastrophic (open/short) failures from burn-in will be conducted only when a lot fails the burn-in or re-burn-in PDA requirements.

4.4 Quality Conformance Inspection: Quality conformance inspection shall be in accordance with 4.2 and 4.3 herein and as follows:

4.4.1 Group A Inspection: Group A inspection shall be performed in accordance with 4.1 herein, per MIL-STD-883, Method 5005, and specified in Table IV herein.

4.4.2 Group B Inspection: When purchased, a full Group B is performed on an inspection lot. As a minimum, Subgroup B2 (Resistance to Solvents / Mark Permanency) and Subgroup B3 (Solderability) are performed prior to the first shipment from any inspection lot and Attributes provided when a Full Space Data Pack is ordered. Subgroup B5 (Operating Life) is performed on each wafer lot. This subgroup may or may not be from devices built in the same package style as the current inspection lot. Attributes and variables data for this subgroup will be provided upon request at no charge.

4.4.2.1 Group B, Subgroup 2c = 10%

Group B, Subgroup 3 = 10%

Group B, Subgroup 4 = 5%

Group B, Subgroup 5 = *5%
(*per wafer or inspection lot
whichever is the larger quantity)

Group B, Subgroup 6 = 15%

4.4.2.2 All footnotes pertaining to Table IIa in MIL-STD-883, Method 5005 apply. The quantity (accept number) of all other subgroups are per MIL-STD-883, Method 5005, Table IIa.

4.4.3 Group D Inspection: When purchased, a full Group D is performed on an inspection lot. As a minimum, periodic full Group D sampling is performed on each package family for each assembly location every 26 weeks. A generic Group D Summary is provided when a full Space Data Pack is ordered.

4.4.3.1 Group D, Subgroups 3, 4 and 5 = 15% each (Sample Size Series).

4.4.3.2 All footnotes pertaining to Table IV in MIL-STD-883, Method 5005 apply. The quantity (accept number) or sample number and accept number of all other subgroups are per MIL-STD-883, Method 5005, Table IV.

4.5 Source Inspection:

4.5.1 The manufacturer will coordinate Source Inspection at wafer lot acceptance and pre-seal internal visual.

4.5.2 The procuring activity has the right to perform source inspection at the supplier's facility prior to shipment for each lot of deliverables when specified as a customer purchase order line item. This may include wafer lot acceptance and final data review.

4.6 Deliverable Data: Deliverable data that will ship with devices when a Space Data Pack is ordered:

4.6.1 Lot Serial Number Sheets identifying all devices accepted through final inspection by serial number.

4.6.2 100% attributes (completed lot specific traveler; includes Group A Summary)

4.6.3 Burn-In Variables Data and Deltas (if applicable)

4.6.4 Group B2, B3, and B5 Attributes (Variables data, if performed on lot shipping)

4.6.5 Generic Group D data (4.4.3 herein)

4.6.6 SEM photographs (3.13 herein)

4.6.7 Wafer Lot Acceptance Report (3.13 herein)

4.6.8 X-Ray Negatives and Radiographic Report

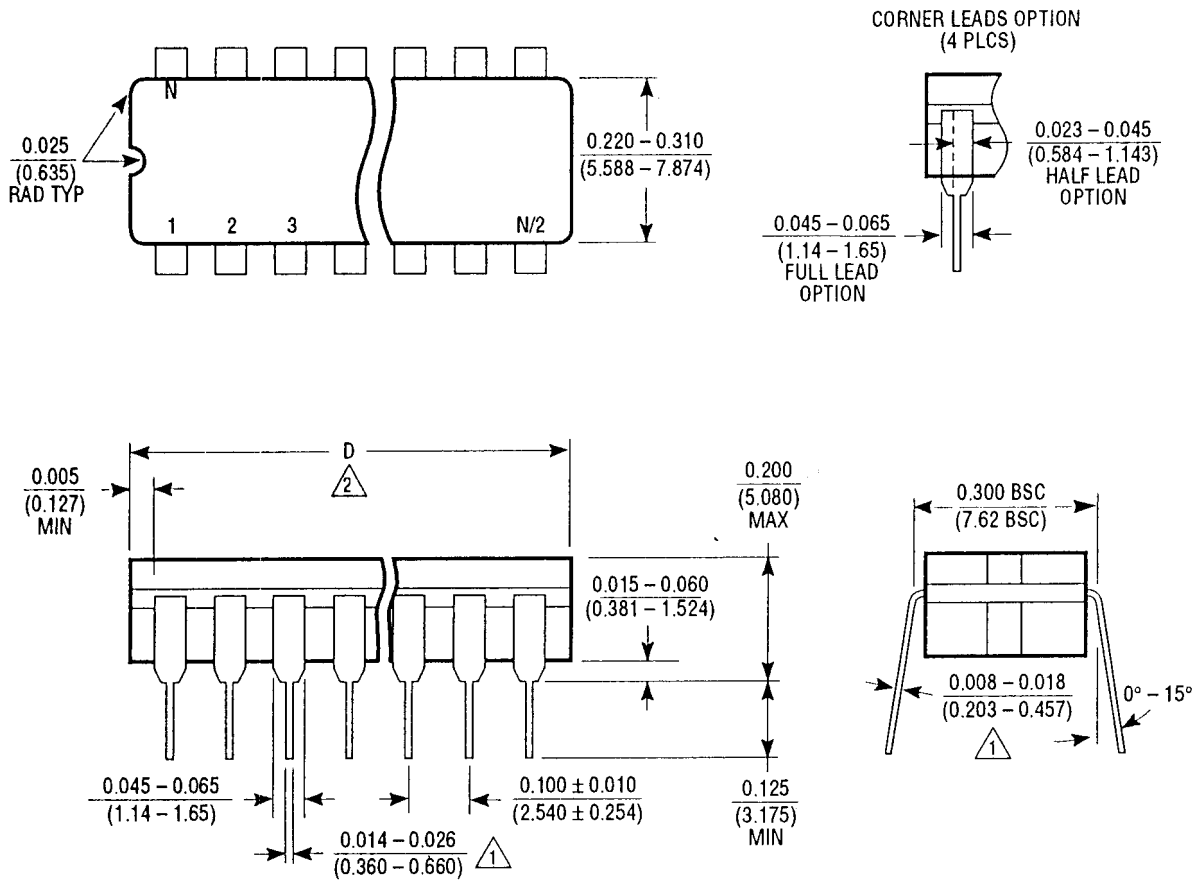
4.6.9 A copy of outside test laboratory radiation report if ordered

4.6.10 Certificate of Conformance certifying that the devices meet all the requirements of this specification and have successfully completed the mandatory tests and inspections herein.

Note: Items 4.6.1 and 4.6.10 will be delivered as a minimum, with each shipment. This is noted on the Purchase Order Review Form as "No Charge Data".

5.0 Packaging Requirements: Packaging shall be in accordance with Appendix A of MIL-PRF-38535. All devices shall be packaged in conductive material or packaged in anti-static material with an external conductive field shielding barrier.

DEVICE OPTION 1
 CERAMIC DIP / 14 LEADS CASE OUTLINE



LEAD COUNT, N	D MAX
14	Ø.785 (19.939)

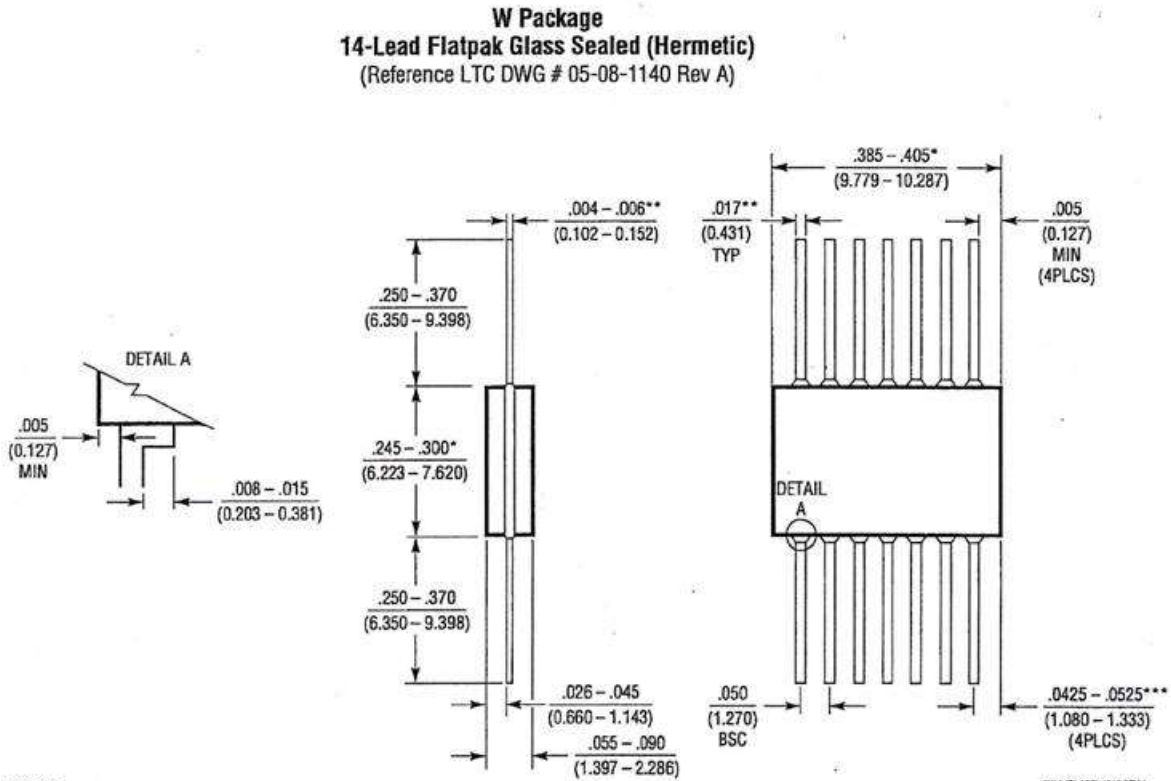
NOTE: 1. LEAD DIMENSIONS APPLY TO SOLDER DIP OR TIN PLATE LEADS.
 2. THIS DIMENSION ALLOWS FOR OFF-CENTER LID, MENISCUS, AND GLASS OVERRUN.

$\theta_{ja} = 95^\circ\text{C/W}$
 $\theta_{jc} = 25^\circ\text{C/W}$
 $T_j \text{ Max} = 174^\circ\text{C}$

FIGURE 1

DEVICE OPTION 2

W14, GLASS SEALED FLATPACK / 14 LEADS CASE OUTLINE



- NOTES:
- *THIS DIMENSION DOES NOT ALLOW FOR OFF-CENTER LID, MENISCUS AND GLASS OVERRUN
 - **INCREASE DIMENSIONS BY 0.003 INCHES (0.076mm) WHEN LEAD FINISH A IS APPLIED (SOLDER DIPPED)
 - ***THIS DIMENSION NOT INCLUDE FOR A MAXIMUM 0.020 INCHES (0.508mm) OFF-SET TO CENTER LID

W14 (GLASS) 1016 REV A

FIGURE 2

TERMINAL CONNECTIONS
OPTION 1, CERAMIC DIP / 14 LEAD

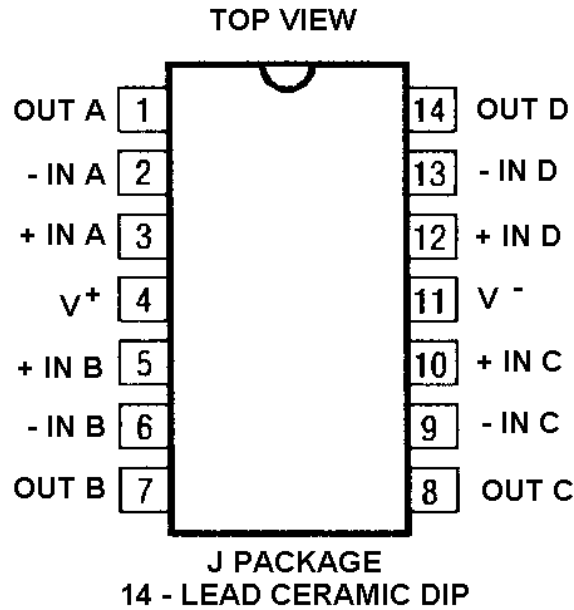


FIGURE 3

OPTION 2, GLASS SEALED FLATPACK / 14 LEADS

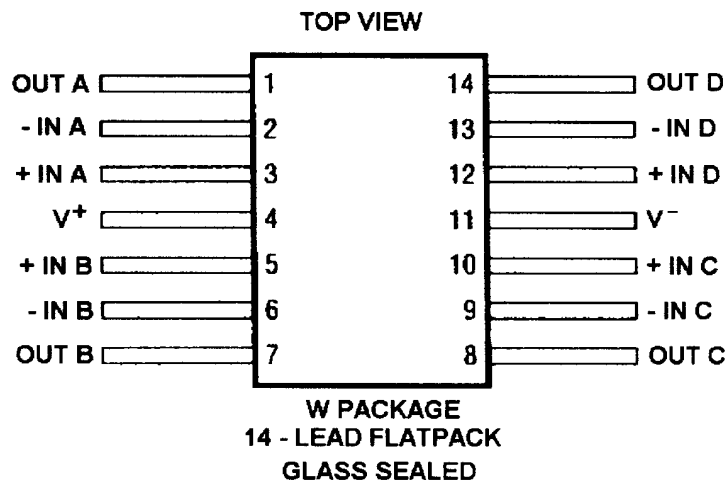
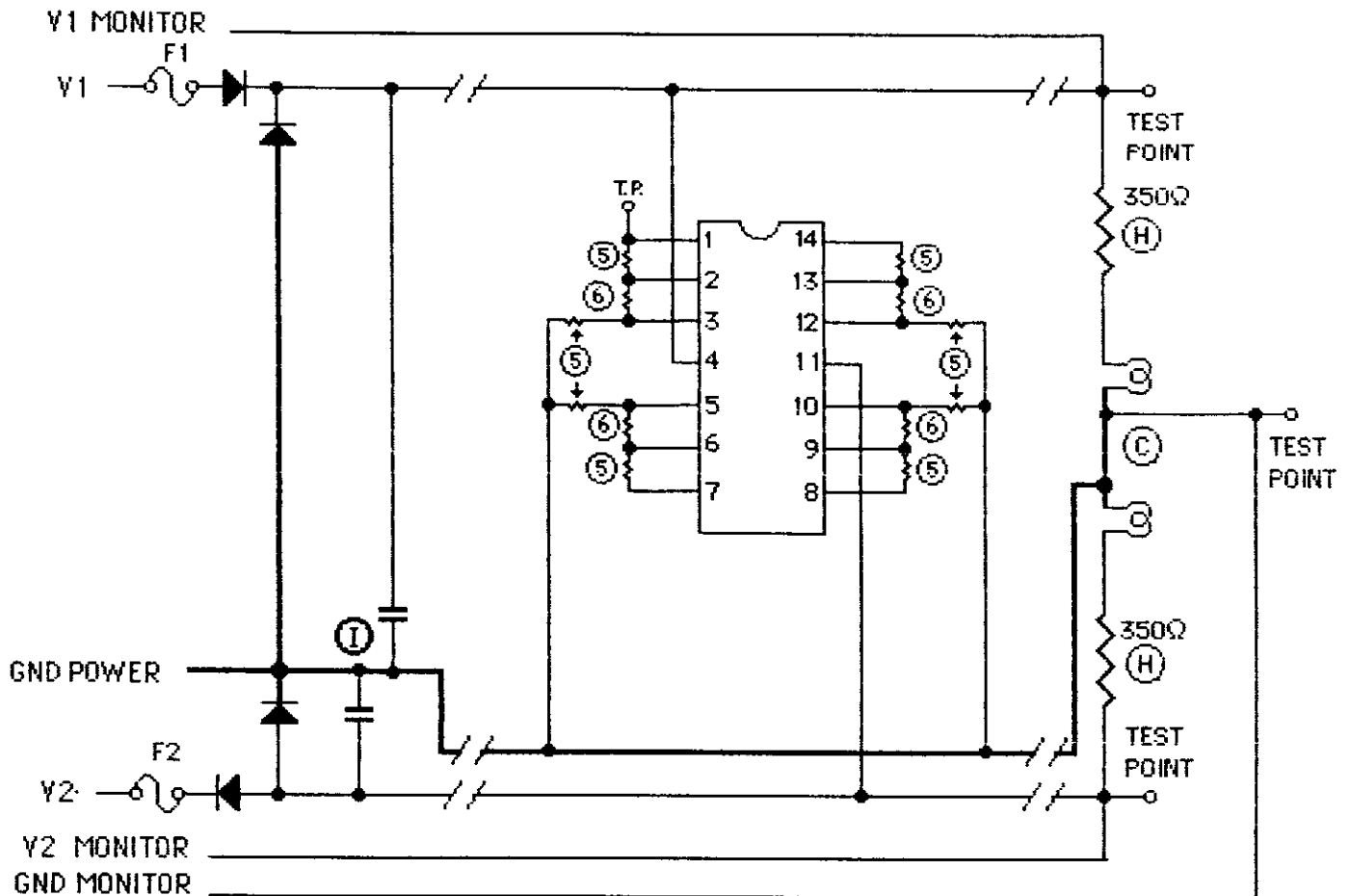


FIGURE 4

STATIC BURN-IN CIRCUIT
OPTION 1, CERAMIC DIP / 14 LEADS

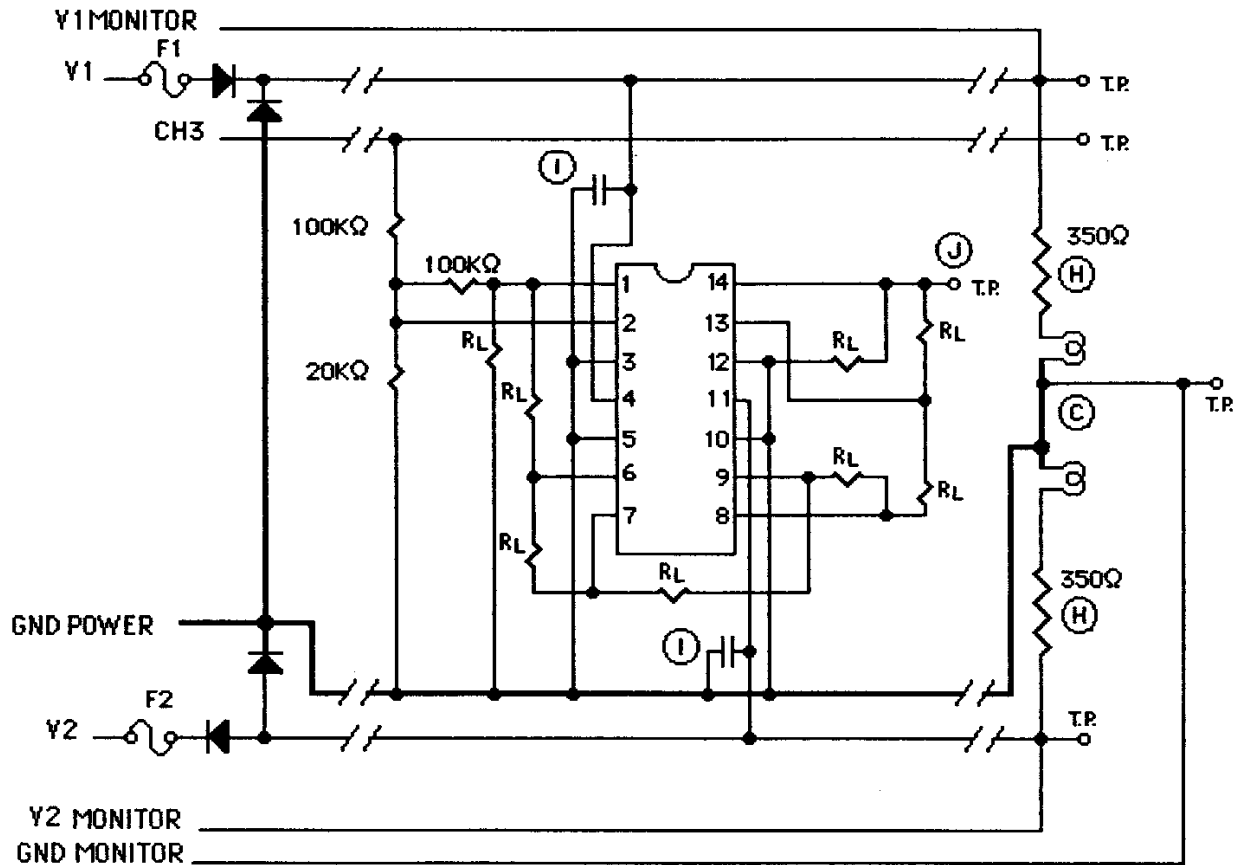


NOTES:

1. Unless otherwise specified, component tolerances shall be per military specification.
2. $T_j = 172^\circ\text{C}$ maximum.
3. $T_a = 150^\circ\text{C}$.
4. Burn-in Voltages: $V_1 = +20\text{V}$ to $+22\text{V}$
 $V_2 = -20\text{V}$ to -22V
5. Resistors to be 1/2 watt, $49.9\text{K}\Omega$ per specification.
6. Resistors to be 1/2 watt, 100Ω per specification.

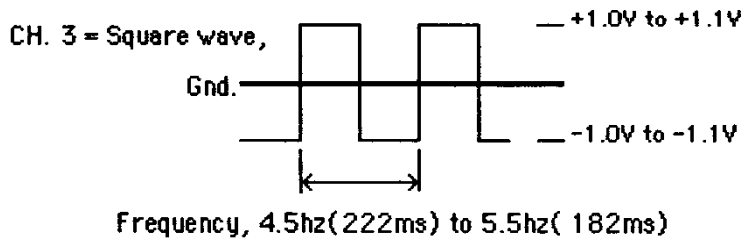
FIGURE 5

**DYNAMIC BURN-IN CIRCUIT
OPTION 1, CERAMIC DIP / 14 LEADS**



NOTES:

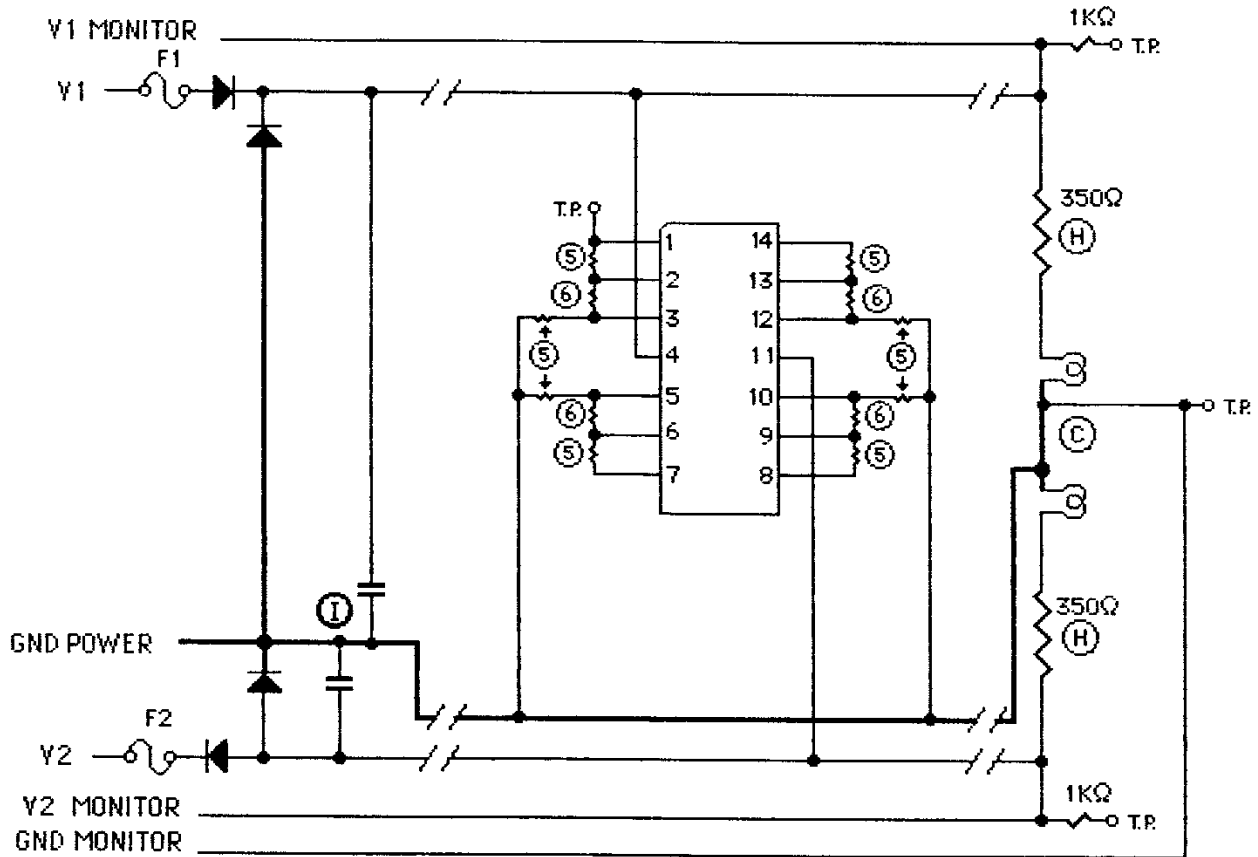
1. Unless otherwise specified, component tolerances shall be per military specification.
2. $T_j = +152^\circ\text{C}$ maximum
3. $T_a = +125^\circ\text{C}$.
4. Burn-in Voltages: $V_1 = +20\text{V}$ to $+22\text{V}$
 $V_2 = -20\text{V}$ to -22V



5. $R_L = 715$

FIGURE 6

STATIC BURN-IN CIRCUIT
OPTION 2, FLATPACK, GLASS SEAL / 14 LEADS

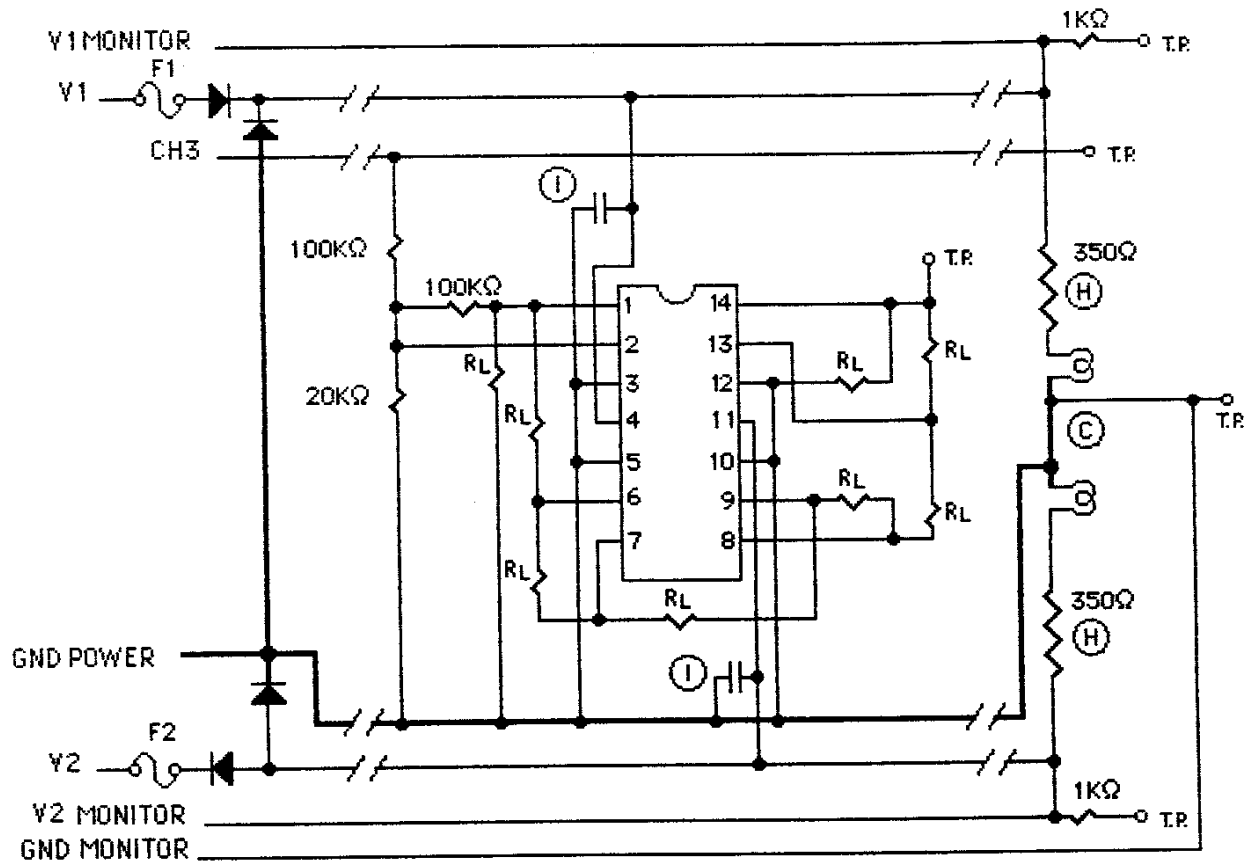


NOTES:

1. Unless otherwise specified, component tolerances shall be per military specification.
2. $T_j = 171\text{ }^\circ\text{C}$ maximum.
3. $T_a = 150\text{ }^\circ\text{C}$.
4. Burn-in Voltages: $V_1 = +20\text{V to } +22\text{V}$
 $V_2 = -20\text{V to } -22\text{V}$
5. Resistors to be 1/2 watt, 49.9KΩ per specification.
6. Resistors to be 1/2 watt, 100Ω per specification.

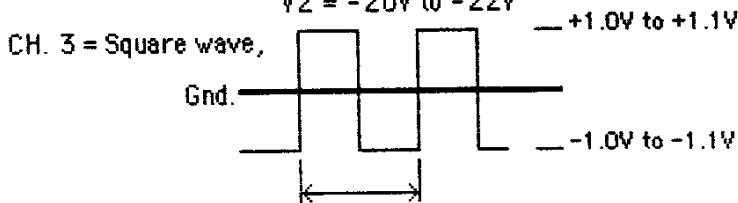
FIGURE 7

DYNAMIC BURN-IN CIRCUIT
OPTION 2, FLATPACK, GLASS SEAL / 14 LEADS



NOTES:

1. Unless otherwise specified, component tolerances shall be per military specification.
2. $T_j = 166^\circ\text{C}$ maximum.
3. $T_a = 125^\circ\text{C}$.
4. Burn-in voltages: $V_1 = +20\text{V to } +22\text{V}$
 $V_2 = -20\text{V to } -22\text{V}$



Frequency, 4.5hz(222ms) to 5.5hz(182ms)

5. $R_L = 715\Omega$

FIGURE 8

TOTAL DOSE BIAS CIRCUIT

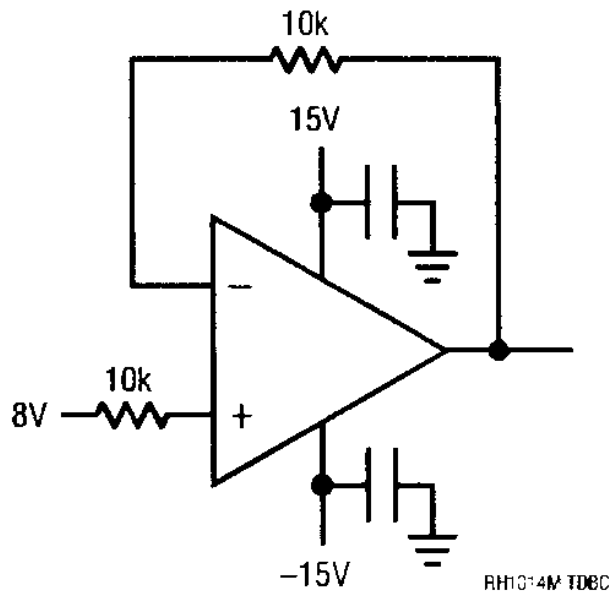


FIGURE 9

TABLE I: ELECTRICAL CHARACTERISTICS (PRE-IRRADIATION)

 $V_S = \pm 15V$, $V_{CM} = 0V$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	NOTES	$T_A = 25^\circ C$		SUB-GROUP	$-55^\circ C \leq T_A \leq 125^\circ C$			UNITS
				MIN	TYP		MAX	MIN	TYP	
V_{OS}	Input Offset Voltage				300	1		550	2,3	μV
			2		450	1		750	3	μV
		$V_{CM} = 0.1V$, $T_A = 125^\circ C$	2					750	2	μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Tempco of Offset Voltage		1				2.5		$\mu V/^\circ C$	
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term V_{OS} Stability			0.5					$\mu V/Mo$	
I_{OS}	Input Offset Current				10	1		20	2,3	nA
			2		10	1		20	2,3	nA
I_B	Input Bias Current				30	1		45	2,3	nA
			2		50	1		120	2,3	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz		0.55						μV_{p-p}
	Input Noise Voltage	$f_0 = 10Hz$		24						nV/\sqrt{Hz}
	Density	$f_0 = 1000Hz$		22						nV/\sqrt{Hz}
i_n	Input Noise Current Density	$f_0 = 10Hz$		0.07						pA/\sqrt{Hz}
R_{IN}	Input Resistance	Differential	1	70						$M\Omega$
		Common Mode		4						$G\Omega$
A_{VOL}	Large-Signal Voltage Gain	$V_O = \pm 10V$, $R_L \geq 2k$		1.2		4	0.25		5,6	$V/\mu V$
		$V_O = \pm 10V$, $R_L \geq 600\Omega$		0.5		4				$V/\mu V$
		$V_O = 5mV$ to $4V$, $R_L = 500\Omega$	2	1						$V/\mu V$
	Input Voltage Range		1	13.5						V
			1	-15.0						V
			1,2	3.5						V
			1,2	0						V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = 13.5V$, $-15V$		97		1				dB
		$V_{CM} = 13V$, $-14.9V$					94		2,3	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2V$ to $\pm 18V$		100		1	97		2,3	dB
	Channel Separation	$V_O = \pm 10V$, $R_L = 2k$		120		1				dB
V_{OUT}	Output Voltage Swing	$R_L \geq 2k$		± 12.5		4	± 11.5		5,6	V
		Output Low, No Load	2		25	4				mV
		Output Low, 600Ω to GND	2		10	4		18	5,6	mV
		Output Low, $I_{SINK} = 1mA$	2		350	4				mV
		Output High, No Load	2		4.0	4				V
		Output High, 600Ω to GND	2		3.4	4		3.1	5,6	V
SR	Slew Rate			0.2		4			$V/\mu s$	
I_S	Supply Current	Per Amplifier			0.55	1		0.70	2,3	mA
			2		0.50	1		0.65	2,3	mA

See Applicable notes on next page.

TABLE II: ELECTRICAL CHARACTERISTICS (POST-IRRADIATION)

$V_S = \pm 15V$, $V_{CM} = 0V$, $T_A = 25^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	NOTES	10KRAD(Si)		20KRAD(Si)		50KRAD(Si)		100KRAD(Si)		200KRAD(Si)		UNITS
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OS}	Input Offset Voltage			450	450	600	750	900					μV	
			2	600	600	750	900					μV		
I_{OS}	Input Offset Current			10	10	15	20	25					nA	
			2	10	10	15	20					nA		
I_B	Input Bias Current			60	75	100	175	250					nA	
			2	80	100	125	200					nA		
	Input Voltage Range		1	13.5	13.5	13.5	13.5	13.5					V	
			1	-15.0	-15.0	-15.0	-15.0	-15.0					V	
			2	3.5	3.5	3.5	3.5						V	
			2	0	0	0	0						V	
CMRR	Common-Mode Rejection Ratio	$V_{CM} = 13V, -15V$		97	97	94	90	86					dB	
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 18V$		100	98	94	86	80					dB	
A_{VOL}	Large-Signal Voltage Gain	$R_L = 10k, V_O = \pm 10V$		500	200	100	50	25					V/mV	
V_{OUT}	Maximum Output Voltage Swing	$R_L = 10k$		± 12.5	± 12.5	± 12.5	± 12.5	± 12.5					V	
			2	25	30	40	50					mV		
			2	10	10	10	10					mV		
			2	0.6	0.8	1.0	1.6					V		
			2	4.0	4.0	4.0	4.0					V		
			2	3.4	3.2	3.0	2.8					V		
SR	Slew Rate	$R_L = 10k$		0.13	0.12	0.11	0.07	0.01					V/ μs	
I_S	Supply Current	Per Amplifier		0.55	0.55	0.55	0.55	0.55					mA	
			2	0.50	0.50	0.50	0.50					mA		

Note 1: Guaranteed by design, characterization, or correlation to other tested parameters.

Note 2: Specification applies for $V_S^+ = 5V$, $V_S^- = 0V$, $V_{CM} = 0V$, $V_{OUT} = 1.4V$.

TABLE III: POST BURN-IN ENDPOINTS AND DELTA LIMIT REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $V_{CM} = 0\text{V}$ unless otherwise noted

PARAMETER	ENDPOINT LIMIT		DELTA		UNITS
	MIN	MAX	MIN	MAX	
V_{OS}	-300	300	-200	200	μV
$+I_B$	-30	+30	-4	4	nA
$-I_B$	-30	+30	-4	4	nA

TABLE IV: ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUP
Final Electrical Test Requirements (Method 5004)	1* 2,3,4,5,6
Group A Test Requirements (Method 5005)	1,2,3,4,5,6
Group B and D for Class S End Point Electrical Parameters (Method 5005)	1,2,3

* PDA applies to subgroup 1. See PDA Test Notes.

PDA Test Notes

The PDA is specified as 5% based on failures from group A, subgroup 1, tests after cooldown as the final electrical test in accordance with method 5004 of MIL-STD-883. The verified failures of group A, subgroup 1, after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent for the lot.

Linear Technology Corporation reserves the right to test to tighter limits than those given.