REVISION RECORD		
REV	DESCRIPTION	DATE
0	INITIAL RELEASE	06/12/96
A	PARAGRAPH 3.8 NOW REFLECTS THE CORRECT FIGURES FOR BURN-IN CIRCUITS FOR EACH PERTINENT PACKAGE. DELETION OF PARAGRAPHS 3.12.1 AND 3.12.2, AND INCORPORATION OF PARAGRAPH 3.12.1 INTO PARAGRAPH 3.12, PAGE 4. CHANGED BURN-IN CIRCUIT FOR FLATPACK. BURN-IN CIRCUIT NOW REFLECTS A CIRCUIT THAT IS USED FOR BOTH STATIC AND DYNAMIC. REMAINING FIGURES WILL BE RENUMBERED. WILL NOT CHANGE. PARAGRAPH 4.5.2 MOVED FROM PAGE 5 TO PAGE 4. ENTIRE SPECIFICATION IS RENUMBERED. ENTIRE SPECIFICATION REV'D.	09/05/96
B	• PAGE 2, ADDED PARAGRAPHS 3.2.1, 3.2.2, AND 3.2.3. • PAGE 2, PARAGRAPH 3.3.b: ADDED "(SEE PARAGRAPH 3.2)". • PAGE 3, ADDED PARAGRAPHS 3.8.1, 3.8.2, AND 3.8.3. • PAGE 4, PARAGRAPH 4.4.2, GROUP B INSPECTION WAS REDEFINED. • PAGE 5, PARAGRAPH 4.4.3, GROUP D INSPECTION WAS REDEFINED. PARAGRAPH 4.5.1, SOURCE INSPECTION WAS REDEFINED. • PAGES 6, 7, 8, FIGURES 1, 2, 3 CASE OUTLINES: ADDED θ_{ja} AND θ_{jc} . • PAGE 9, REDREW FIGURES 5 AND 6 TERMINAL CONNECTIONS. • UPDATED ENTIRE SPEC TO REVISION B.	11/25/97
C	• PAGE 17, CHANGED VOS MIN DELTA LIMIT FROM –60 µV to –200 µV, AND CHANGED VOS MAX DELTA LIMIT FROM 60 µV TO 200 µV.	12/18/97
D	• ADDED A SECOND PAGE FOR REVISION RECORD. UPDATED ENTIRE SPEC TO NEXT REVISION DUE TO THE ADDITIONAL PAGE. • PAGE 3, PARAGRAPH 3.2.3, CHANGED PACKAGE TYPE TO 10 LEAD FLATPACK GLASS SEAL. • PAGE 4, PARAGRAPH 3.8.3, CHANGED OPTION 3 TO FLATPACK GLASS SEAL, AND PARAGRAPH 3.10.3, CHANGED LEAD MATERIAL AND FINISH TO KOVAR WITH HOT SOLDER DIP ON ALL PACKAGE OPTIONS. • PAGE 5, AMENDED PARAGRAPHS 4.1 AND 4.1.1 TAKING EXCEPTION TO ANALYSIS OF CATASTROPHIC FAILURES. • PAGE 9, FIGURE 3, CHANGED PACKAGE TYPE TO FLATPACK GLASS SEAL. • PAGE 10, FIGURE 6, CHANGED PACKAGE TYPE TO FLATPACK GLASS SEAL. • PAGE 14, FIGURE 10, CHANGED PACKAGE TYPE TO FLATPACK GLASS SEAL.	03/20/98
E	• PAGE 7,8,9, FIGURE 1,2,3, CHANGED θ_{JA} AND θ_{JC}.	09/28/99

REVISION RECORD AND DESCRIPTION CONTINUED ON NEXT PAGE.

CAUTION: ELECTROSTATIC DISCHARGE SENSITIVE PART

REVISION	PAGE NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
INDEX	REVISION	**N**	**N**	**N**	**N**	**N**	**N**	**N**	**N**	**N**	**N**	**N**	**N**	**N**	**N**	**N**	**N**	**N**
REVISION	PAGE NO.	18	19	20	21	22												
INDEX	REVISION	**N**	**N**	**N**	**N**	**N**												

				ANALOG DEVICES INC. **MILPITAS, CALIFORNIA**
	ORIG			
	DSGN			TITLE:
	ENGR			**MICROCIRCUIT, LINEAR,** **RH1013M, DUAL PRECISION** **OPERATIONAL AMPLIFIER**
	MFG			
	CM			
	QA			SIZE:
	PROG			**64155** / **05-08-5013** / **N**
APPLICATION	FUNCT	SIGNOFFS	DATE	CONTRACT:

FOR OFFICIAL USE ONLY

REVISION RECORD		
REV	DESCRIPTION	DATE
F	• PAGE 3, PARAGRAPHS 3.2.1, 3.2.2, 3.2.3 HAD FIGURES 1, 2, AND 3 REMOVED. • PAGE 4, PARAGRAPH 3.7, CHANGED VERBIAGE FROM "SPECIFIED IN TABLE III" TO "AND AS SPECIFIED IN TABLE III HEREIN", LINE 2. PARAGRAPH 3.9, ADDED "HEREIN" AFTER "TABLE II", LINE 2. • PAGE 5, PARAGRAPH 4.3, ADDED "HEREIN" AFTER "TABLE III", LINE 2. PARAGRAPH 4.4.1, ADDED "HEREIN" AFTER "TABLE III", LINE 2. • PAGE 6, PARAGRAPH 4.4.2.2, CHANGED VERBIAGE IN LINE 1 FROM "ALL FOOTNOTES OF TABLE 11A OF MIL-STD-883" TO "ALL FOOTNOTES PERTAINING TO TABLE IIA IN MIL-STD-883". PARAGRAPH 4.4.3.2, CHANGED VERBIAGE IN LINE 1 FROM "ALL FOOTNOTES OF TABLE IV OF MIL-STD-883" TO "ALL FOOTNOTES PERTAINING TO TABLE IV IN MIL-STD-883'.	11/18/99
G	• PAGE 9, CHANGED THETA JA TO θJA=170°C/W AND THETA JC TO θJC=40°C/W FROM θJA=225°C/W AND θJC=18°C/W PER PACKAGE ENGINEER.	08/30/00
H	• PAGE 3: PARAGRAPH 3.2.1 ADDED "OPTION 1", PARAGRAPH 3.2.2, ADDED "OPTION 2", PARAGRAPH 3.2.3, ADDED "OPTION 3". • PAGE 4: PARAGRAPH 3.6, TABLE IA CHANGED TO TABLE II. PARAGRAPH 3.7, TABLE III CHANGED TO TABLE IV. PARAGRAPH 3.9, TABLE II CHANGED TO TABLE III. PARAGRAPH 3.10.3, ADDED "DEVICE OPTIONS 1, 2, AND 3" TO LINE 1. PARAGRAPH 3.11.1 WAS CHANGED FROM "…dosage rate of approximately 20 Rads per second" TO "…dosage rate of less than or equal to 10 Rads per second". • PAGE 5: PARAGRAPHS 4.1 THROUGH 4.4.2.1 CHANGES WERE DONE TO CLARIFY GROUP SAMPLING. PARAGRAPH 4.4.3 CHANGE WAS DONE TO CLARIFY GROUP SAMPLING. • PAGE 6: PARAGRAPHS 4.6.2 THROUGH 4.6.4 WERE RE-WRITTEN. THESE DATA PROVIDED, AND DATA AVAILABLE. PARAGRAPH 4.6.10 NOTE, ADDED FURTHER EXPLANATION OF MINIMUM DELIVERED DATA. • PAGES 7 THROUGH 15, ALL FIGURE TITLES CHANGED TO HAVE DEVICE OPTIONS AND PACKAGE TYPES AT TOP OF PAGE, AND HAVE ALL FIGURES AT BOTTOM OF PAGE. • PAGE 8: LEAD SHOULDER DIAMETER MAX NOW 0.065 INCHES (WAS 0.068). • PAGE 9: CASE OUTLINE UPDATED TO MIL-STD-1835. • PAGE 10: MOVED FIGURES TO BETTER FIT THE PAGE. • PAGE 17: TABLE IA HAS BECOME TABLE II. • PAGE 18: TABLE II HAS BECOME TABLE III. TABLE III HAS BECOME TABLE IV.	04/08/03
J	• PAGE 9: CASE OUTLINE DRAWING CHANGED PIN 1 NOTCH MOVED TO INSIDE LEAD LOCATION.	5/19/03
K	• PAGE 4: CHANGED INITIAL RATE OF RADS TO 240 RADS/SEC.	03/15/05
L	• PAGE 5, CHANGED IN BOTH PARAGRAPHS 4.2, 4.3 IN CONJUNCTION TO 3.3 CHANGED TO 3.4 AND PARAGRAPH 4.3 CHANGED 3.1.1 TO 3.1 AND 3.2.1 TO 3.1.1 • PAGE 4, PARAGRAPH 3.10.3 CHANGED OPTION 2 & ADDED OPTION 3 AS ALLOY 42. PARAGRAPH 3.11.1 CHANGED VERBIAGE.	04/23/08

REVISION RECORD		
REV	DESCRIPTION	DATE
M	Replace burnin circuit in figure 7, 8 & 9 to reflect changes to burn-in ambient temperature and addition of thermal shutdown temperature	12/01/17
N	**Removed Source Inspection (4.5.1)** **Changed LTC footer to Analog Devices Inc.** **Add OBS to Option 2 – RH1013MJ8 (Ceramic Dip, 8 Leads) (OBS)**	**01/15/19**

1.0 SCOPE:

1.1 This specification defines the performance and test requirements for a microcircuit processed to a space level manufacturing flow.

2.0 APPLICABLE DOCUMENTS:

2.1 Government Specifications and Standards: the following documents listed in the Department of Defense Index of Specifications and Standards, of the issue in effect on the date of solicitation, form a part of this specification to the extent specified herein.

SPECIFICATIONS:

MIL-PRF-38535	Integrated Circuits (Microcircuits) Manufacturing, General Specification for
MIL-STD-883	Test Method and Procedures for Microcircuits
MIL-STD-1835	Microcircuits Case Outlines

2.2 Order of Precedence: In the event of a conflict between the documents referenced herein and the contents of this specification, the order of precedence shall be this specification, MIL-PRF-38535 and other referenced specifications.

3.0 REQUIREMENTS:

3.1 General Description: This specification details the requirements for the RH1013M DUAL PRECISION OPERATIONAL AMPLIFIER, processed to space level manufacturing flow.

3.2 Part Number:

3.2.1 Option 1 – RH1013MH (TO5 Metal Can, 8 Leads)

3.2.2 Option 2 – RH1013MJ8 (Ceramic Dip, 8 Leads) (OBS)

3.2.3 Option 3 – RH1013MW (Glass Sealed Flatpack, 10 Leads)

3.3 Part Marking Includes:

a. LTC Logo

b. LTC Part Number (See Paragraph 3.2)

c. Date Code

d. Serial Number

e. ESD Identifier per MIL-PRF-38535, Appendix A

3.4 The Absolute Maximum Ratings:

Supply Voltage (Pin 8 to Pin 4)	±22V
Differential Input Voltage	±30V
Input Voltage	Equal to Positive Supply Voltage
	5V Below Negative Supply Voltage
Output Short Circuit Duration 1/	INDEFINITE
Operating Temperature Range	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 sec)	+300°C

1/ Parameter is guaranteed by design, characterization, or correlation to other tested parameters.

3.5 Electrostatic discharge sensitivity, ESDS, shall be Class 1.

3.6 Electrical Performance Characteristics: The electrical performance characteristics shall be as specified in Table I and **Table II.**

3.7 Electrical Test Requirements: Screening requirements shall be in accordance with 4.1 herein, MIL-STD-883, Method 5004, and as specified in **Table IV** herein.

3.8 Burn-In Requirement:

3.8.1 Option 1 (TO5): Static Burn-In, Figure 7; Dynamic Burn-In, Figure 8

3.8.2 Option 2 (Ceramic Dip): Static/Dynamic Burn-In, Figure 9

3.8.3 Option 3 (Glass Sealed Flatpack) : Static/Dynamic Burn-In, Figure 10

3.9 Delta Limit Requirement: Delta limit parameters are specified in **Table III** herein, are calculated after each burn-in, and the delta rejects are included in the PDA calculation.

3.10 Design, Construction, and Physical Dimensions: Detail design, construction, physical dimensions, and electrical requirements shall be specified herein.

3.10.1 Mechanical / Packaging Requirements: Case outlines and dimensions are in accordance with Figure 1, Figure 2, and Figure 3.

3.10.2 Terminal Connections: The terminal connections shall be as specified in Figure 4, Figure 5, and Figure 6.

3.10.3 Lead Material and Finish: The lead material and finish for Device Options 1, shall be Kovar and options 2, 3 are Alloy 42. The lead finishes shall be hot solder dip (Finish letter A) in accordance with MIL-PRF-38535.

3.11 Radiation Hardness Assurance (RHA):

3.11.1 The manufacturer shall perform a lot sample test as an internal process monitor for total dose radiation tolerance. The sample test is performed with MIL-STD-883 TM1019 Condition A as a guideline.

3.11.2 For guaranteed radiation performance to MIL-STD-883, Method 1019, total dose irradiation, the manufacturer will provide certified RAD testing and report through an independent test laboratory when required as a customer purchase order line item.

3.11.3 Total dose bias circuit is specified in Figure 11.

3.12 Wafer Lot Acceptance: Wafer lot acceptance shall be in accordance with MIL-PRF-38535, Appendix A, except for the following: Topside glassivation thickness shall be a minimum of 4KÅ.

3.13 Wafer Lot Acceptance Report: SEM is performed per MIL-STD-883, Method 2018 and copies of SEM photographs shall be supplied with the Wafer Lot Acceptance Report as part of a Space Data Pack when specified as a customer purchase order line item.

4.0 VERIFICATION (QUALITY ASSURANCE PROVISIONS)

4.1 Quality Assurance Provisions: Quality Assurance provisions shall be in accordance with MIL-PRF-38535. Linear Technology is a QML certified company and all Rad Hard candidates are assembled on qualified Class S manufacturing lines.

4.2 Sampling and Inspection: Sampling and Inspection shall be in accordance with MIL-STD-883, Method 5005 with QML allowed and TRB approved deviations in conjunction with paragraphs 3.1.1, 3.2.1, and 3.4 of the test method.

4.3 Screening: Screening requirements shall be in accordance with MIL-STD-883, Method 5004 with QML allowed and TRB approved deviations in conjunction with paragraphs 3.1, 3.1.1 and 3.4 of the test method. Electrical testing shall be as specified in Table IV herein.

4.3.1 Analysis of catastrophic (open/short) failures from burn-in will be conducted only when a lot fails the burn-in or re-burn-in PDA requirements.

4.4 Quality Conformance Inspection: Quality conformance inspection shall be in accordance with 4.2 and 4.3 herein and as follows:

4.4.1 Group A Inspection: Group A inspection shall be performed in accordance with 4.1 herein, per MIL-STD-883, Method 5005, and specified in Table IV herein.

4.4.2 Group B Inspection: When purchased, a full Group B is performed on an inspection lot. As a minimum, Subgroup B2 (Resistance to Solvents / Mark Permanency) and Subgroup B3 (Solderability) are performed prior to the first shipment from any inspection lot and Attributes provided when a Full Space Data Pack is ordered. Subgroup B5 (Operating Life) is performed on each wafer lot. This subgroup may or may not be from devices built in the same package style as the current inspection lot. Attributes and variables data for this subgroup will be provided upon request at no charge.

4.4.2.1

Group B, Subgroup 2c = 10%	Group B, Subgroup 5 = *5% (*per wafer or inspection lot
Group B, Subgroup 3 = 10%	whichever is the larger quantity)
Group B, Subgroup 4 = 5%	Group B, Subgroup 6 = 15%

4.4.2.2 All footnotes pertaining to Table IIa in MIL-STD-883, Method 5005 apply. The quantity (accept number) of all other subgroups are per MIL-STD-883, Method 5005, Table IIa.

4.4.3 Group D Inspection: When purchased, a full Group D is performed on an inspection lot. As a minimum, periodic full Group D sampling is performed on each package family for each assembly location every 26 weeks. A generic Group D Summary is provided when a full Space Data Pack is ordered.

4.4.3.1 Group D, Subgroups 3, 4 and 5 = 15% each (Sample Size Series).

4.4.3.2 All footnotes pertaining to Table IV in MIL-STD-883, Method 5005 apply. The quantity (accept number) or sample number and accept number of all other subgroups are per MIL-STD-883, Method 5005, Table IV.

4.5 Source Inspection:

4.5.1 The procuring activity has the right to perform source inspection at the supplier's facility prior to shipment for each lot of deliverables when specified as a customer purchase order line item. This may include wafer lot acceptance and final data review.

4.6 Deliverable Data: Deliverable data that will ship with devices when a Space Data Pack is ordered:

4.6.1 Lot Serial Number Sheets identifying all devices accepted through final inspection by serial number.

4.6.2 100% attributes (completed lot specific traveler; includes Group A Summary)

4.6.3 Burn-In Variables Data and Deltas (if applicable)

4.6.4 Group B2, B3, and B5 Attributes (Variables data, if performed on lot shipping)

4.6.5 Generic Group D data (4.4.3 herein)

4.6.6 SEM photographs (3.13 herein)

4.6.7 Wafer Lot Acceptance Report (3.13 herein)

4.6.8 X-Ray Negatives and Radiographic Report

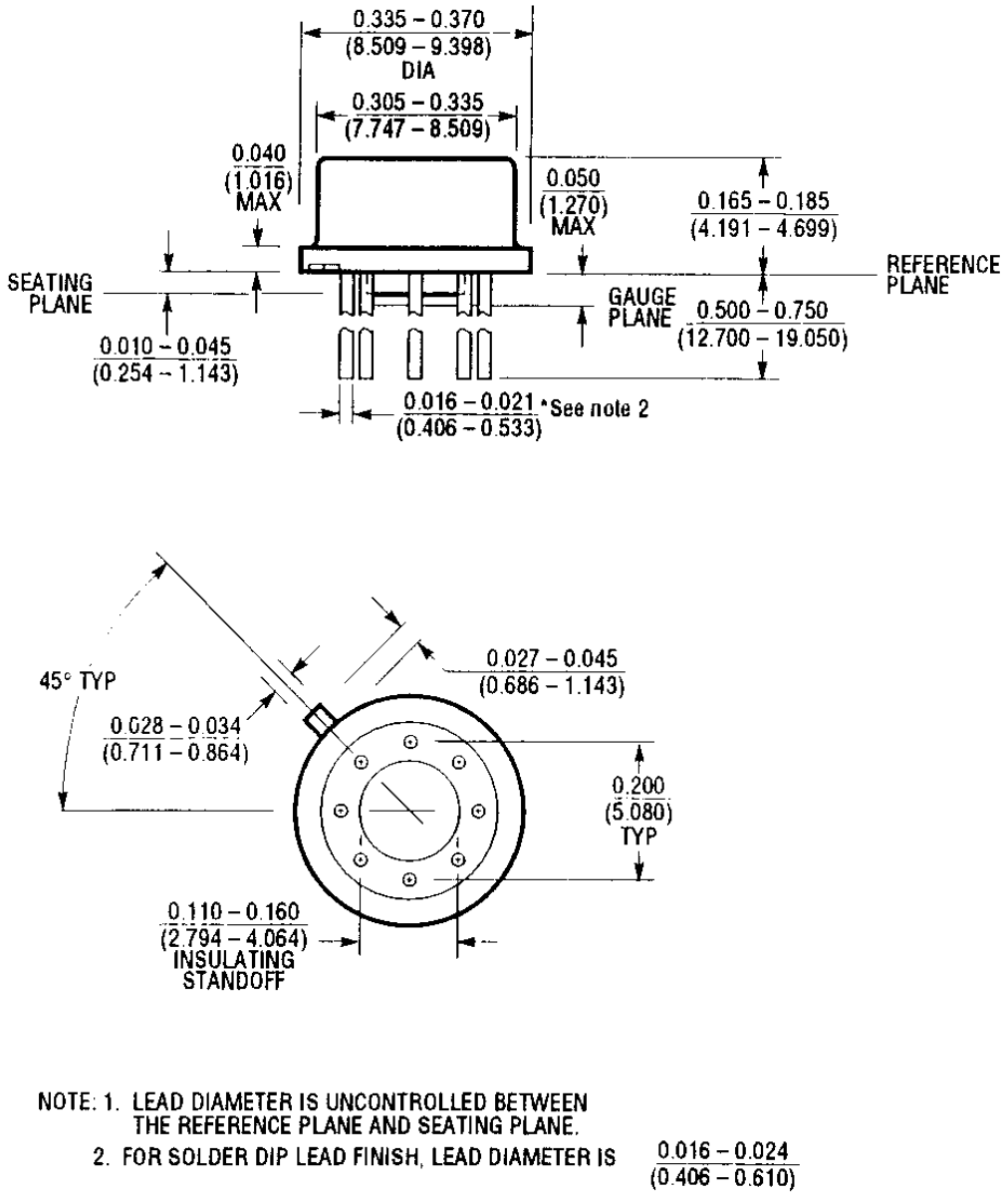
4.6.9 A copy of outside test laboratory radiation report if ordered

4.6.10 Certificate of Conformance certifying that the devices meet all the requirements of this specification and have successfully completed the mandatory tests and inspections herein.

Note: Items 4.6.1 and 4.6.10 will be delivered as a minimum, with each shipment. This is noted on the Purchase Order Review Form as "No Charge Data".

5.0 Packaging Requirements: Packaging shall be in accordance with Appendix A of MIL-PRF-38535. All devices shall be packaged in conductive material or packaged in anti-static material with an external conductive field shielding barrier.

DEVICE OPTION # 1
(H) TO5 / 8 LEADS CASE OUTLINE

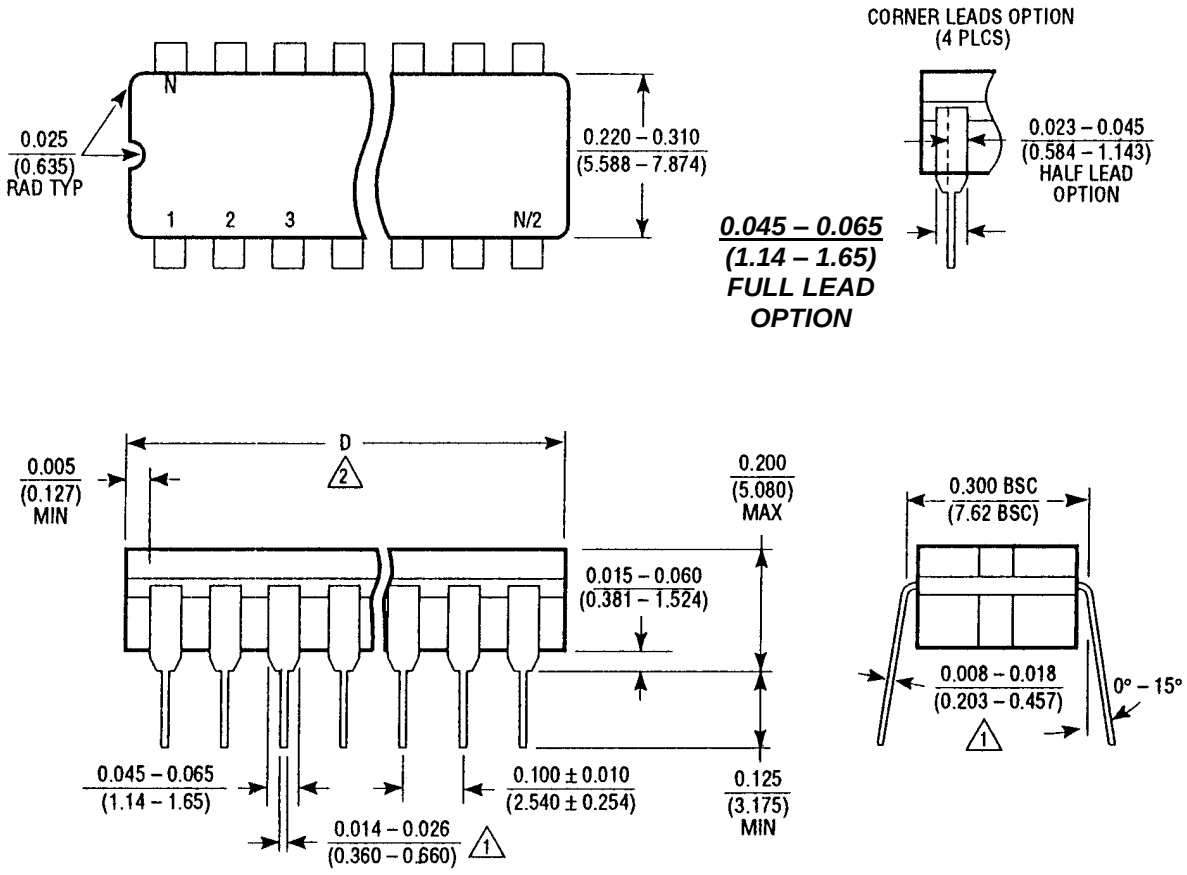


NOTE: 1. LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND SEATING PLANE.
2. FOR SOLDER DIP LEAD FINISH, LEAD DIAMETER IS 0.016 – 0.024 (0.406 – 0.610)

θ_{ja} = +150°C/W
θ_{jc} = +40°C/W

FIGURE 1

DEVICE OPTION # 2
(J8) CERAMIC DIP / 8 LEADS CASE OUTLINE

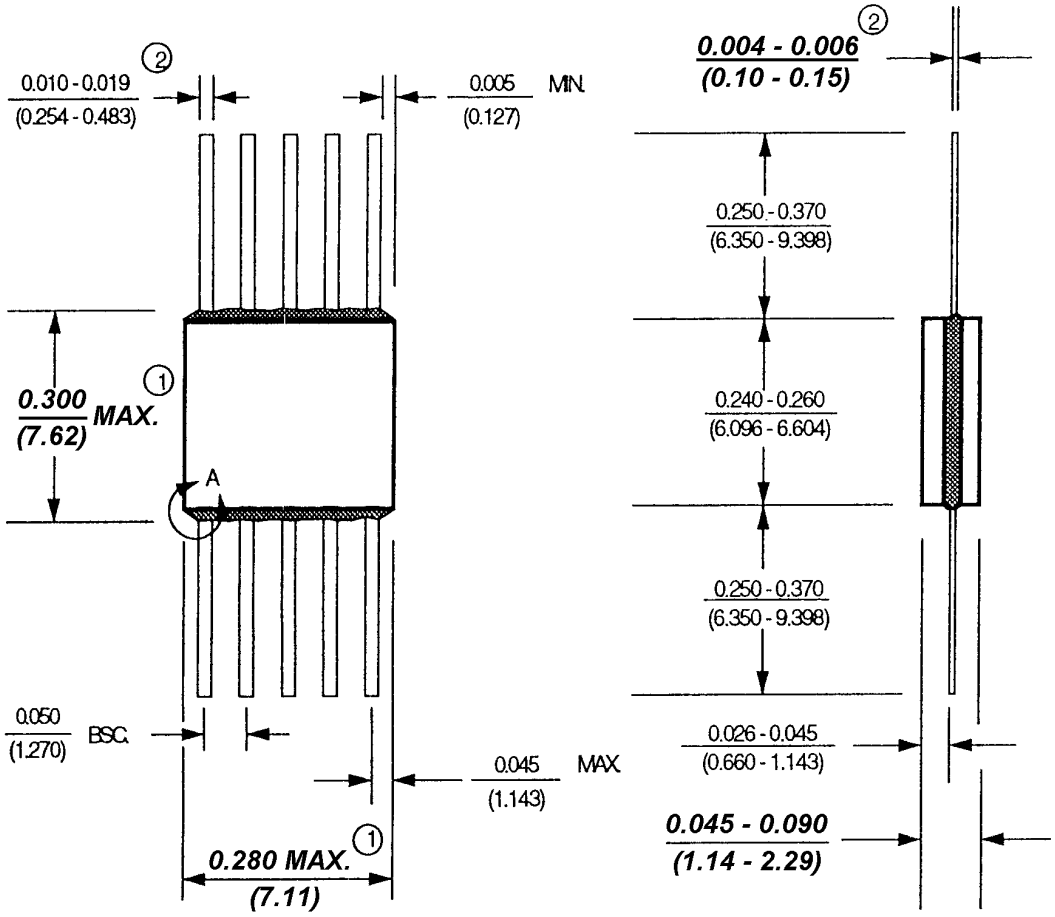


NOTE: 1. LEAD DIMENSIONS APPLY TO SOLDER DIP OR TIN PLATE LEADS.
2. 8 LEAD D MAX = .405 (10.287)

θ_{ja} = +110°C/W
θ_{jc} = +30°C/W

FIGURE 2

DEVICE OPTION # 3
(W10) GLASS SEALED FLATPACK / 10LEADS CASE OUTLINE



NOTE: 1. THIS DIMENSION ALLOWS FOR OFF-CENTER LID, MENISCUS AND GLASS OVER RUN.

NOTE: 2. INCREASE DIMENSION BY 0.003 INCH WHEN LEAD FINISH IS APPLIED (SOLDER DIPPED).

θ_{ja} = +170°C/W
θ_{jc} = +40°C/W

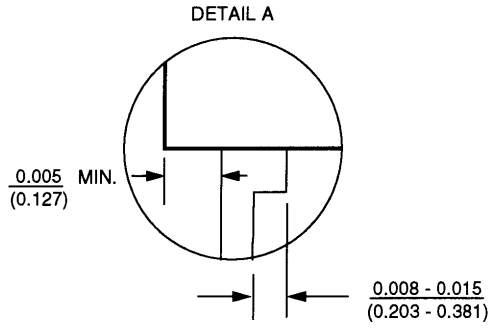


FIGURE 3

TERMINAL CONNECTIONS

DEVICE OPTION #1, TO5 8 LEAD METAL CAN

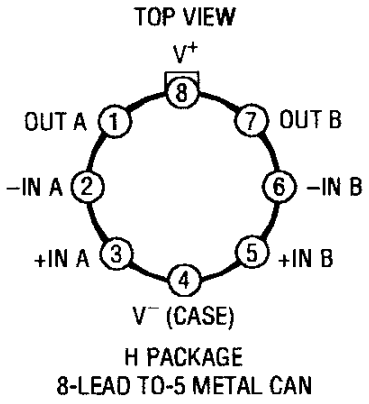


FIGURE 4

DEVICE OPTION #2, 8 LEAD CERAMIC DIP

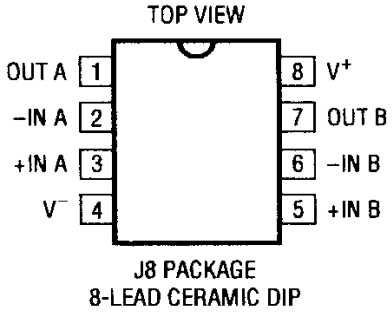


FIGURE 5

DEVICE OPTION #3, GLASS SEALED 10 LEAD FLATPACK

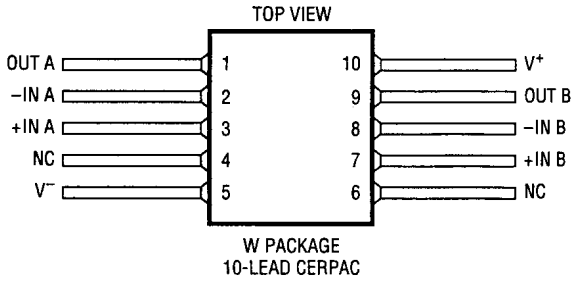


FIGURE 6

STATIC BURN-IN CIRCUIT
OPTION 1, TO5 METAL CAN / 8 LEADS

		OVEN OPTIONS			
BOARD STYLE: LTC	YES	LEGACY OVEN	YES	MCC OVEN	YES
AVI-TECH	NO	OPTIMUM OVEN	YES	OUTSIDE OVEN	YES

RIDER CARD ASSEMBLY: N/A

PROBE: 04-06-9252

	HARDWARE #	REV.	QUANTITY BOARDS	MAX SKTS PER BOARD
BOARD:	04-06-0035	A	1	80
EDGE CARD:	N/A			
ROW CARD:	N/A			

	MIN °C	MAX °C
AMBIENT TEMP:	125°C	133°C
JUNCTION TEMP:	137°C	141°C
AMBIENT TEMP:	150°C	158°C
JUNCTION TEMP:	162°C	166°C
THERMAL SHUTDOWN:	N/A	

POWER SEQUENCE						DEVICE		EMPTY BOARD		
ON	OFF	SUPPLY	MIN V	MAX V	FUSE AMPS	STARTUP CURRENT	STEADY STATE CURRENT	PER ROW CARD	PER EDGE CARD	DEDICATED BOARD PER SKT
		V1	+20.0V	+22.0V	2Amp	2mA/SKT	2mA/SKT	N/A	N/A	0mA/SKT + 50mA
		V2	-20.0V	-22.0V	2Amp	1.4mA/SKT	1.4mA/SKT	N/A	N/A	0mA/SKT + 50mA
		V3								
		V4								
		V5								

TEST POINTS

T.P.#	PIN NAME	VALUE
1	OUTA	GND
2	OUTB	GND

PWR/MON OPTIONS	
YES	V1/V4
	V2/GND

SPECIAL NOTES:
- Do not connect V4 PWR.

CLOCKS ON VS DC	MIN V	MAX V	FREQ	DUTY CYCLE	VECTOR?

Figure 7 continue on next page

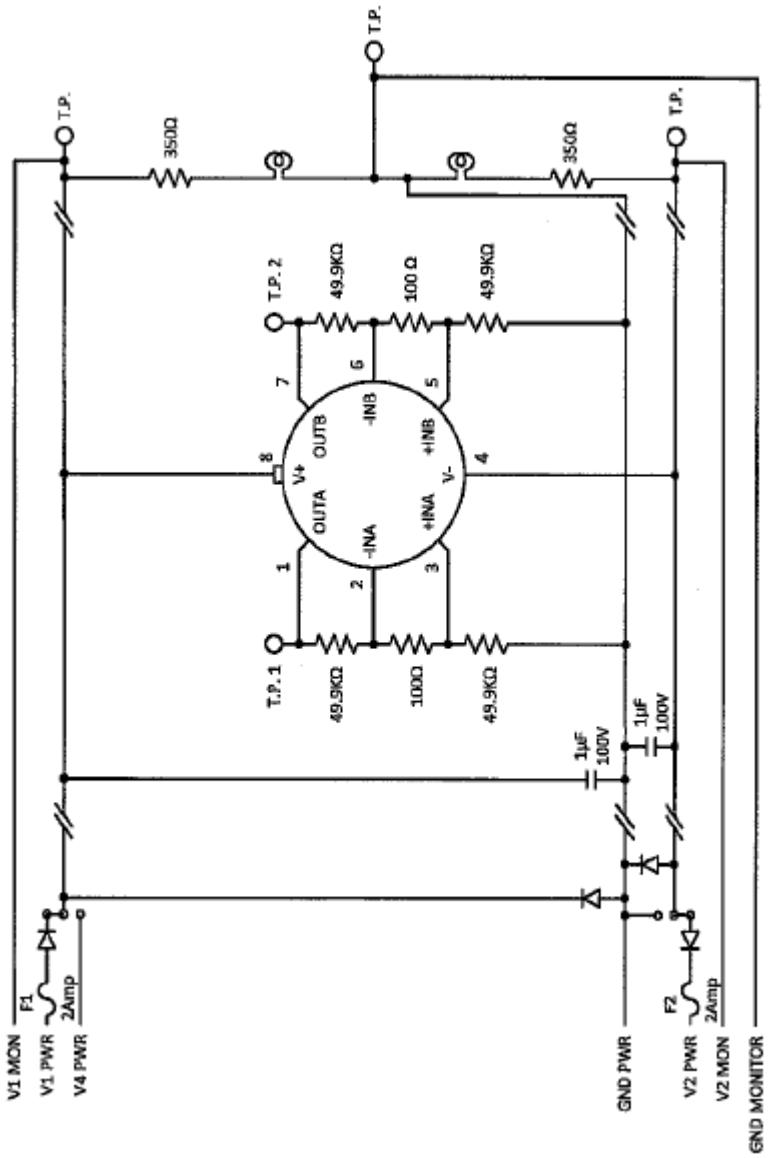
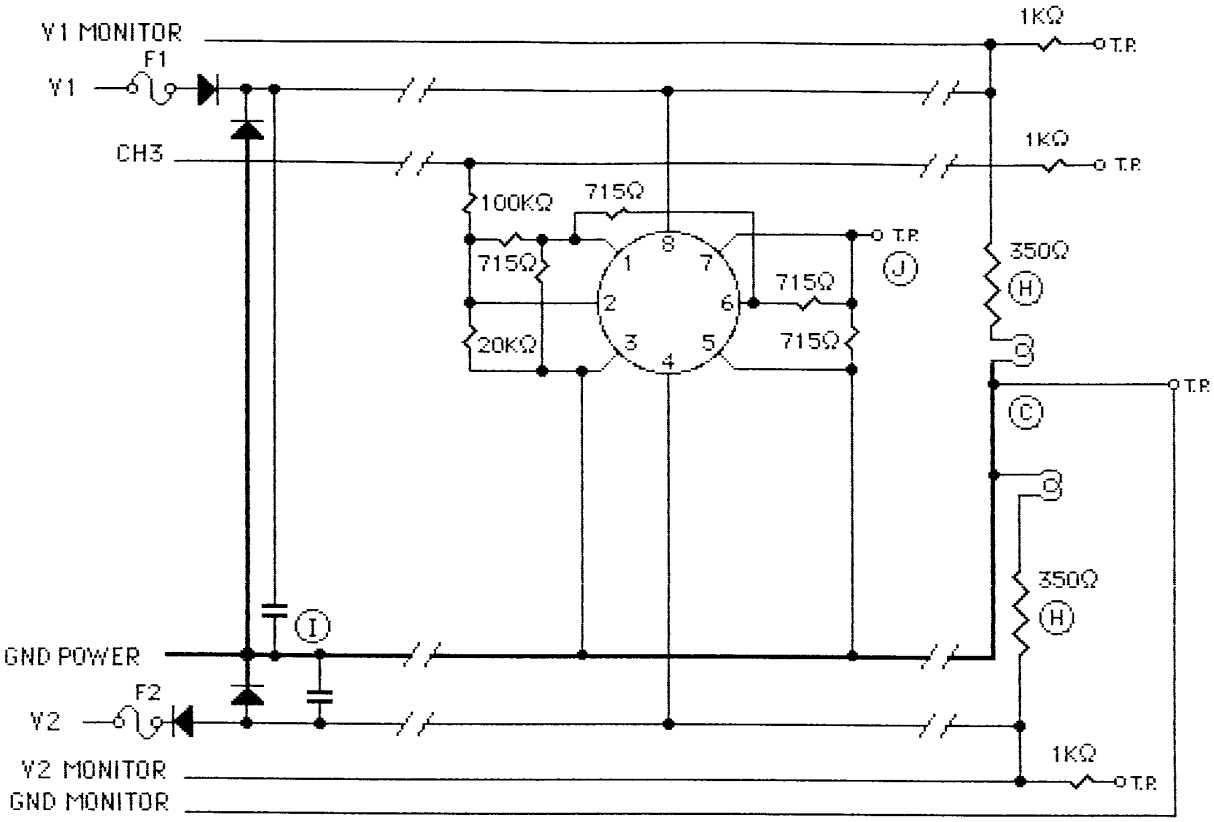

T.P.
T.P.
T.P.
350Ω
350Ω
T.P. 2
49.9KΩ
100 Ω
49.9KΩ
T.P. 1
49.9KΩ
100Ω
49.9KΩ
1µF 100V
1µF 100V
OUTB
-INB
+INB
V+
V-
OUTA
-INA
+INA
F1 2Amp
F2 2Amp
V1 MON
V1 PWR
V4 PWR
GND PWR
V2 PWR
V2 MON
GND MONITOR

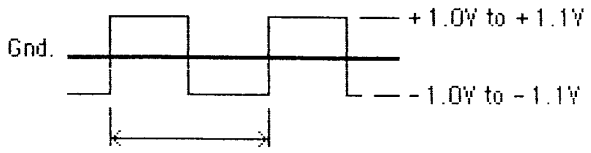
FIGURE 7

DYNAMIC BURN-IN CIRCUIT
OPTION 1, TO5 METAL CAN / 8 LEADS



NOTES:

1. Unless otherwise specified, component tolerances shall be per military specification.
2. Tj = 146°C maximum.
3. Ta = 125°C.
4. Burn-in Voltages: V1 = +20V to +22V
   V2 = -20V to -22V
5. CH3 = Square wave,



Frequency, 4.5Hz (222mS) to 5.5Hz (182mS)

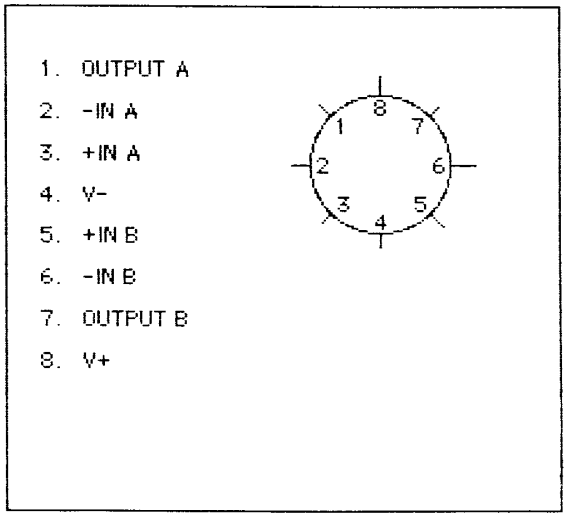


FIGURE 8

STATIC/DYNAMIC BURN-IN CIRCUIT
OPTION 2, CERDIP / 8 LEADS

		OVEN OPTIONS			
BOARD STYLE: LTC	YES	LEGACY OVEN	YES	MCC OVEN	YES
AVI-TECH	NO	OPTIMUM OVEN	YES	OUTSIDE OVEN	YES

RIDER CARD ASSEMBLY: N/A

PROBE: 04-06-9121

	HARDWARE #	REV.	QUANTITY BOARDS	MAX SKTS PER BOARD
BOARD:	04-06-00383	C	1	192
EDGE CARD:	N/A			
ROW CARD:	N/A			

	MIN °C	MAX °C
AMBIENT TEMP:	125°C	133°C
JUNCTION TEMP:	128°C	137°C
AMBIENT TEMP:	150°C	158°C
JUNCTION TEMP:	153°C	162°C
THERMAL SHUTDOWN:	N/A	

POWER SEQUENCE						DEVICE		EMPTY BOARD		
ON	OFF	SUPPLY	MIN V	MAX V	FUSE AMPS	STARTUP CURRENT	STEADY STATE CURRENT	PER ROW CARD	PER EDGE CARD	DEDICATED BOARD PER SKT
		V1	+20.0V	+22.0V	2Amp	2mA/SKT	2mA/SKT	N/A	N/A	0mA/SKT + 50mA
		V2	-20.0V	-22.0V	2Amp	1.4mA/SKT	1.4mA/SKT	N/A	N/A	0mA/SKT + 50mA
		V3								
		V4								
		V5								

TEST POINTS

T.P.#	PIN NAME	VALUE
1	OUTA	GND
2	OUTB	GND

PWR/MON OPTIONS: NO / /

SPECIAL NOTES:

1. BOARD TO BE USED FOR BOTH STATIC AND DYNAMIC BURN-IN. ENSURE THAT CHANNEL THREE IS PRESENT FOR DYNAMIC BURN-IN. ENSURE THAT CHANNEL THREE IS NOT PRESENT FOR STATIC BURN-IN.

CHANNELS	CLOCKS ON VS DC	MIN V	MAX V	FREQ	DUTY CYCLE	VECTOR?
CH3	AFTER	-1.0V to -1.1V	+1V to +1.1V	4.5 Hz to 5.5 Hz	50%	N/A

Figure 9 continue on next page

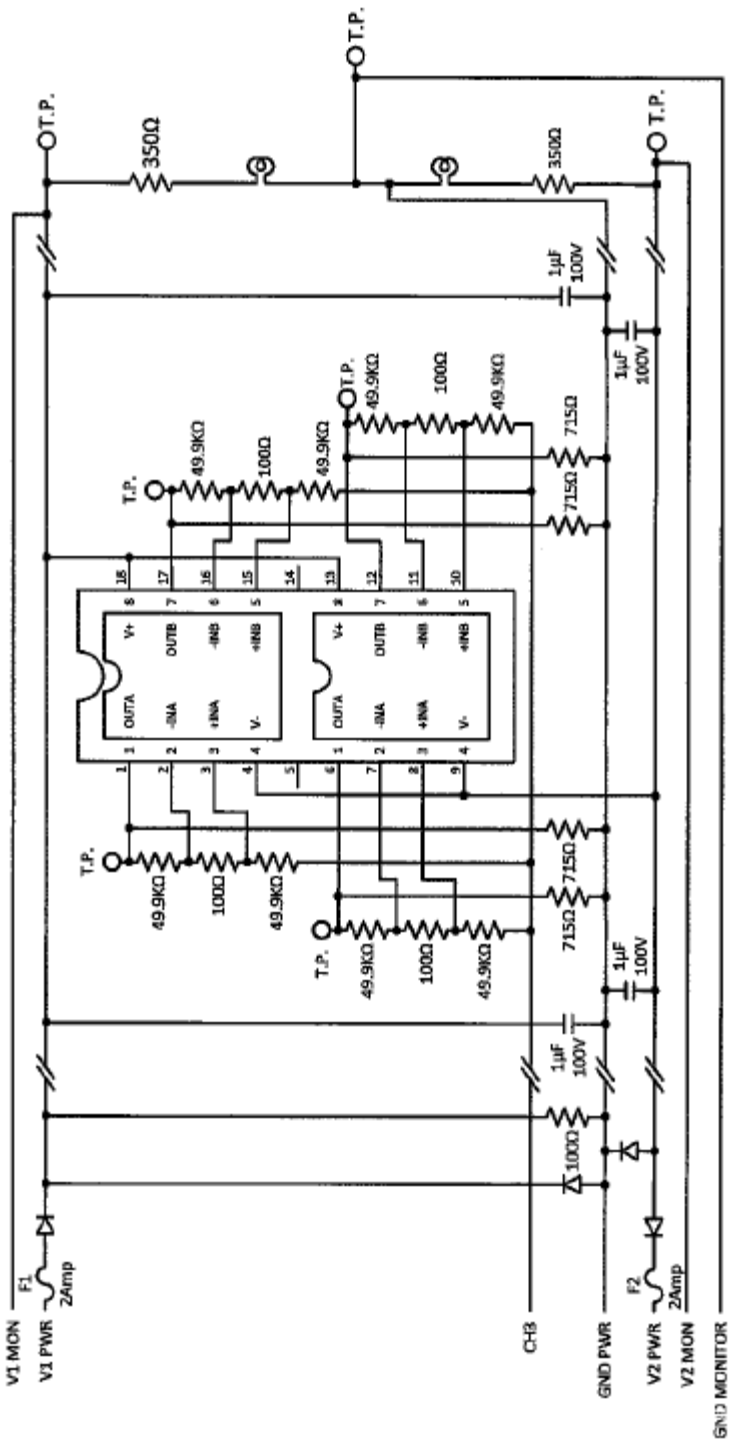

T.P.
350Ω
1µF 100V
49.9KΩ
100Ω
715Ω
V+
OUTB
-INB
+INB
OUTA
-INA
+INA
V-
F1 2Amp
F2 2Amp
V1 MON
V1 PWR
CHS
GND PWR
V2 PWR
V2 MON
GND MONITOR

FIGURE 9

STATIC/DYNAMIC BURN-IN CIRCUIT
OPTION 3, FLATPACK GLASS SEAL

OVEN OPTIONS

BOARD STYLE: LTC	YES	LEGACY OVEN	YES	MCC OVEN	YES
AVI-TECH	NO	OPTIMUM OVEN	YES	OUTSIDE OVEN	YES

RIDER CARD ASSEMBLY: N/A

PROBE: 04-06-9185

	HARDWARE #	REV.	QUANTITY BOARDS	MAX SKTS PER BOARD
BOARD:	04-06-0391	A	1	80
EDGE CARD:	N/A			
ROW CARD:	N/A			

	MIN °C	MAX °C
AMBIENT TEMP:	125°C	133°C
JUNCTION TEMP:	130°C	143°C
AMBIENT TEMP:	150°C	158°C
JUNCTION TEMP:	155°C	168°C
THERMAL SHUTDOWN:	N/A	

POWER SEQUENCE						DEVICE		EMPTY BOARD		
ON	OFF	SUPPLY	MIN V	MAX V	FUSE AMPS	STARTUP CURRENT	STEADY STATE CURRENT	PER ROW CARD	PER EDGE CARD	DEDICATED BOARD PER SKT
		V1	+20.0V	+22.0V	2Amp	2mA/SKT	2mA/SKT	N/A	N/A	0mA/SKT + 50mA
		V2	-20.0V	-22.0V	2Amp	1.4mA/SKT	1.4mA/SKT	N/A	N/A	0mA/SKT + 50mA
		V3								
		V4								
		V5								

TEST POINTS

T.P.#	PIN NAME	VALUE
1	OUTA	GND
2	OUTB	GND

PWR/MON OPTIONS

NO / /

SPECIAL NOTES:

1. BOARD TO BE USED FOR BOTH STATIC AND DYNAMIC BURN-IN. ENSURE THAT CHANNEL THREE IS PRESENT FOR DYNAMIC BURN-IN. ENSURE THAT CHANNEL THREE IS NOT PRESENT FOR STATIC BURN-IN.

CHANNELS	CLOCKS ON VS DC	MIN V	MAX V	FREQ	DUTY CYCLE	VECTOR?
CH3	AFTER	-1.0V to -1.1V	+1.0V to +1.1V	4.5 Hz to 5.5 Hz	50%	N/A

Figure 10 continue on next page

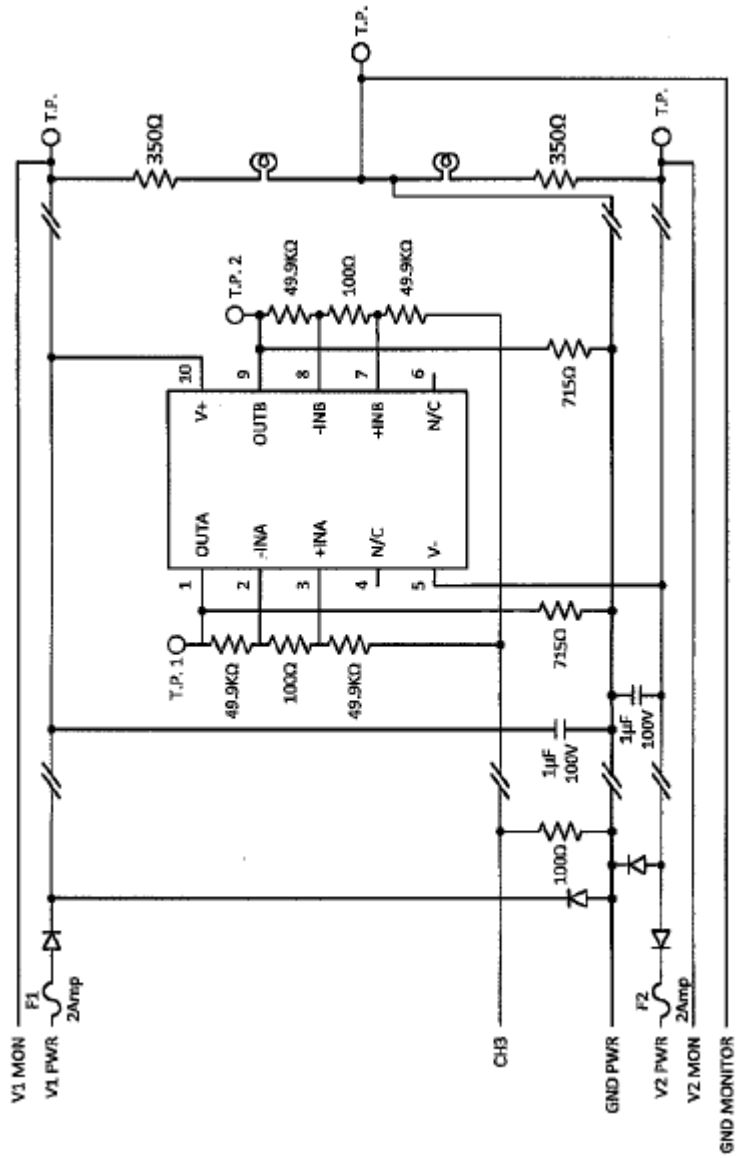

T.P.
350Ω
350Ω
T.P.
T.P.
T.P. 2
49.9KΩ
100Ω
49.9KΩ
715Ω
10
9
8
7
6
V+
OUTB
-INB
+INB
N/C
OUTA
-INA
+INA
N/C
V-
1
2
3
4
5
T.P. 1
49.9KΩ
100Ω
49.9KΩ
715Ω
1µF 100V
1µF 100V
100Ω
F1
2Amp
F2
2Amp
V1 MON
V1 PWR
CH3
GND PWR
V2 PWR
V2 MON
GND MONITOR

FIGURE 10

TOTAL DOSE BIAS CIRCUIT

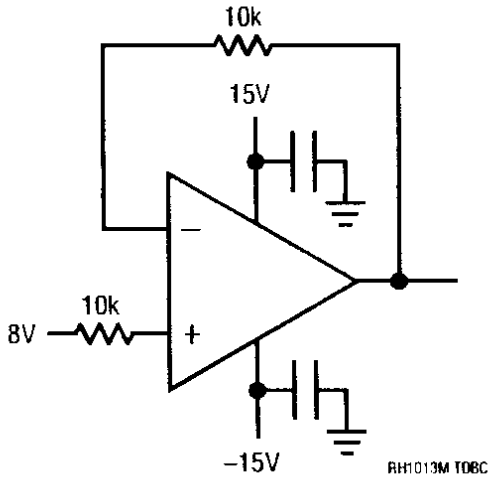


FIGURE 11

TABLE I: ELECTRICAL CHARACTERISTICS (PRE-IRRADIATION)

$V_S = \pm 15V$, $V_{CM} = 0V$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	NOTES	$T_A = 25°C$ MIN	TYP	MAX	SUB-GROUP	$-55°C \le T_A \le 125°C$ MIN	TYP	MAX	SUB-GROUP	UNITS
V_{OS}	Input Offset Voltage					300	1			550	2,3	µV
			2			450	1			750	3	µV
		$V_{CM} = 0.1V$								750	2	µV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Tempco of Offset Voltage		1							2.5		µV/°C
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term V_{OS} Stability				0.5							µV/Mo
I_{OS}	Input Offset Current					10	1			20	2,3	nA
			2			10	1			20	2,3	nA
I_B	Input Bias Current					30	1			45	2,3	nA
			2			50	1			120	2,3	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz			0.55							μV_{P-P}
	Input Noise Voltage Density	$f_O = 10Hz$			24							$nV/\sqrt{Hz}$
		$f_O = 1000Hz$			22							$nV/\sqrt{Hz}$
i_n	Input Noise Current Density	$f_O = 10Hz$			0.07							$pA/\sqrt{Hz}$
R_{IN}	Input Resistance	Differential	1	70								MΩ
		Common Mode			4							GΩ
A_{VOL}	Large-Signal Voltage Gain	$V_O = \pm 10V$, $R_L \ge 2k$		1.2			4	0.25			5,6	V/µV
		$V_O = \pm 10V$, $R_L \ge 600\Omega$		0.5			4					V/µV
		$V_O = 5mV$ to $4V$, $R_L = 500\Omega$	2		1							V/µV
	Input Voltage Range		1	13.5								V
			1	−15.0								V
			1,2	3.5								V
			1,2	0								V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = 13.5V, -15V$		97			1					dB
		$V_{CM} = 13V, -14.9V$						94			2,3	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2V$ to $\pm 18V$		100			1	97			2,3	dB
	Channel Separation	$V_O = \pm 10V$, $R_L = 2k$		120			1					dB
V_{OUT}	Output Voltage Swing	$R_L \ge 2k$		±12.5			4	±11.5			5,6	V
		Output Low, No Load	2			25	4					mV
		Output Low, 600Ω to GND	2			10	4			18	5,6	mV
		Output Low, $I_{SINK} = 1mA$	2			350	4					mV
		Output High, No Load	2	4.0			4					V
		Output High, 600Ω to GND	2	3.4			4	3.1			5,6	V
SR	Slew Rate			0.2			4					V/µs
I_S	Supply Current	Per Amplifier				0.55	1			0.70	2,3	mA
			2			0.50	1			0.65	2,3	mA

Note: Table I electrical characteristics notes are on the next page following Table II .

TABLE II: ELECTRICAL CHARACTERISTICS (POST-IRRADIATION) NOTE

V_S = ±15V, V_{CM} = 0V, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	NOTES	10KRAD(Si) MIN	10KRAD(Si) MAX	20KRAD(Si) MIN	20KRAD(Si) MAX	50KRAD(Si) MIN	50KRAD(Si) MAX	100KRAD(Si) MIN	100KRAD(Si) MAX	200KRAD(Si) MIN	200KRAD(Si) MAX	UNITS
V_{OS}	Input Ofset Voltage				450		450		600		750		900	µV
			2		600		600		750		900			µV
I_{OS}	Input Offset Current				10		10		15		20		25	nA
			2		10		10		15		20			nA
I_B	Input Bias Current				60		75		100		175		250	nA
			2		80		100		125		200			nA
	Input Voltage Range		1	13.5		13.5		13.5		13.5		13.5		V
			1	−15.0		−15.0		−15.0		−15.0		−15.0		V
			2	3.5		3.5		3.5		3.5				V
			2	0		0		0		0				V
CMRR	Common-Mode Rejection Ratio	V_{CM} = 13V, −15V		97		97		94		90		86		dB
PSRR	Power Supply Rejection Ratio	V_S = ±10V to ±18V		100		98		94		86		80		dB
A_{VOL}	Large-Signal Voltage Gain	R_L ≥ 10k, V_O = ±10V		500		200		100		50		25		V/mV
V_{OUT}	Maximum Output Voltage	R_L ≥ 10k		±12.5		±12.5		±12.5		±12.5		±12.5		V
	Swing	Output Low, No Load	2		25		30		40		50			mV
		Output Low, 600Ω to GND	2		10		10		10		10			mV
		Output Low, I_{SINK} = 1mA	2		0.6		0.8		1.0		1.6			V
		Output High, No Load	2	4.0		4.0		4.0		4.0				V
		Output High, 600Ω to GND	2	3.4		3.2		3.0		2.8				V
SR	Slew Rate	R_L ≥ 10k		0.13		0.12		0.11		0.07		0.01		V/µs
I_S	Supply Current	Per Amplifier			0.55		0.55		0.55		0.55		0.55	mA
			2		0.50		0.50		0.50		0.50			mA

Note 1: Guaranteed by design, characterization, or correlation to other tested parameters..

Note 2: Specification applies for V_S^+ = 5V, V_S^- = 0V, V_{CM} = 0V, V_{OUT} = 1.4V.

TABLE III: POST BURN-IN ENDPOINTS AND DELTA LIMIT REQUIREMENTS

T_A = 25°C, V_S = ±15V, V_{CM} = 0V unless otherwise noted

	ENDPOINT LIMIT		DELTA		
PARAMETER	MIN	MAX	MIN	MAX	UNITS
V_{OS}	-300	300	-200	200	µV
$+I_B$	-30	0	-3	3	nA
$-I_B$	-30	0	-3	3	nA

TABLE IV: ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUP
FINAL ELECTRICAL TEST REQUIREMENTS (METHOD 5004)	1*, 2, 3, 4, 5, 6
GROUP A TEST REQUIREMENTS (METHOD 5005)	1, 2, 3, 4, 5, 6
GROUP B AND D FOR CLASS S ENDPOINT ELECTRICAL PARAMETERS (METHOD 5005)	1, 2, 3

*PDA APPLIES TO SUBGROUP 1.

PDA TEST NOTE: The PDA is specified as 5% based on failures from Group A, Subgroup 1, tests after cooldown as the final electrical test in accordance with method 5004 of MIL-STD-883. The verified failures of Group A, Subgroup 1 and delta rejects after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent for the lot