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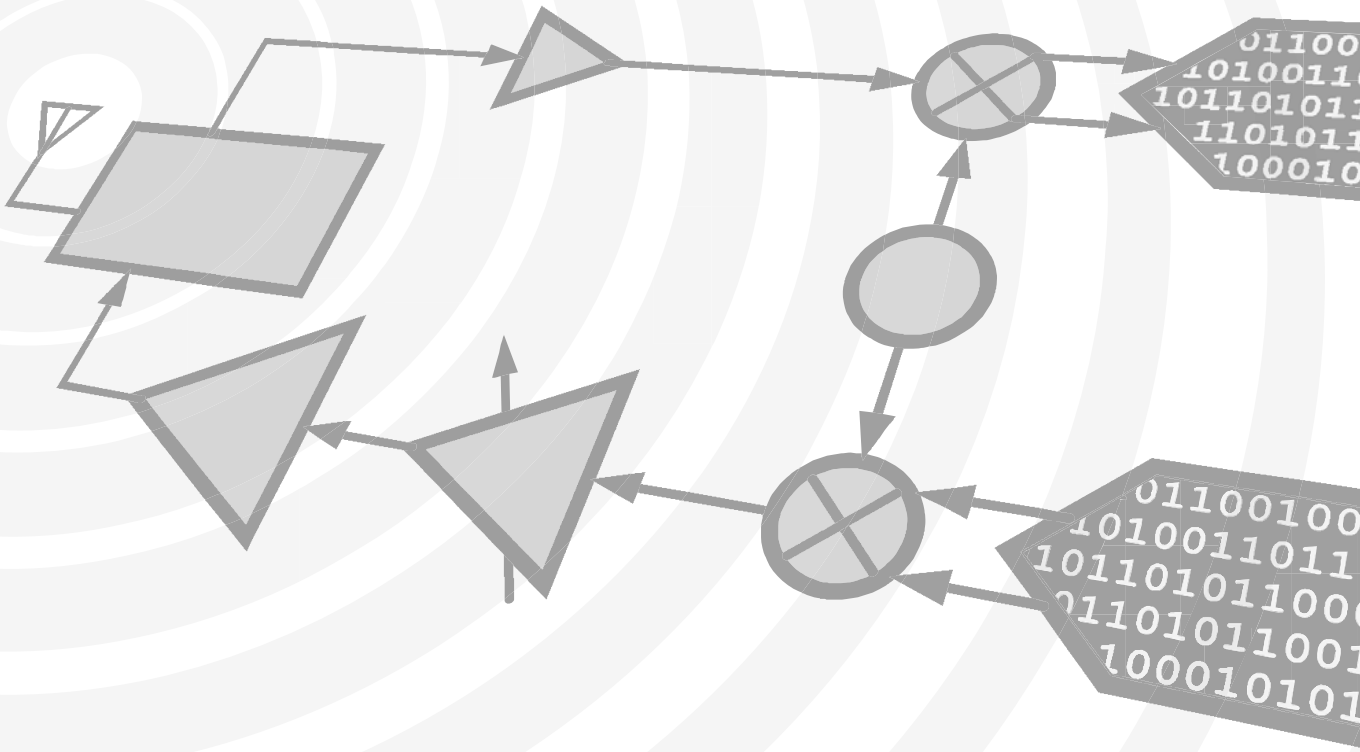

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HMCAD1511 ADC's Digital Gain Feature Enables Optimal Balancing of SNR and Distortion Performance

Purpose

This note describes how Hittite's 8-bit analog-to-digital converter family HMCAD1510/11/12/13 helps ease the challenges of pre-ADC signal conditioning and the SNR-versus-distortion tradeoff with its features of full-scale range adjustment and programmable digital gain.

Introduction

The HMCAD1511 family of 8-bit, low-power ADCs offer excellent SNR and SNDR (also known as SiNAD) performance while consuming very little power. They also cover a range of sample rates from 250 MS/s to 1.0 GS/s at 4, 2 or 1-channel per device selectable configurations. There are also two features built into these devices that may not be appreciated at first glance: user-selectable full-scale range and programmable digital gain of up to 32x. The digital gain can come very handy in the design of the analog front-end signal chain as it allows the designer the flexibility of using lower analog signal amplitude for optimal cascaded performance through the entire chain. This digital gain is distinct from the full-scale range adjustment of the analog input that these devices also provide. With the fine-tuning of the full-scale range the system designer can better utilize these 8-bit ADCs' precious codes.

The Problem of Filling the ADC's Input

It is a well understood challenge in any modern signal path design where an ADC is employed for purposes of digital signal processing: how to fill the ADC's input "full-scale" or span without clipping or overloading the ADC under extreme conditions. In most practical, robust designs you end up wasting a good number of the ADC's codes because as all the tolerances of the signal chain's components are accounted for, you end up staying well away from the full-scale points of the ADC's input. This means that, essentially, you don't use all the ADC bits you pay for. Note that this applies regardless of the use of AGC – which helps tremendously with the large variations in the input signal strength. But in the end analysis the basic problem still remains due to tolerances and the lack of very precise and repeatable configuration of the analog components in the front-end.

The HMCAD1511 family helps the system designer in this area by allowing adjustment of the ADC's full-scale range. The full-scale range (or span) of this family of ADCs is normally 2.0Vpp measured differentially; but it can be adjusted by up to +9.7% or -10% in steps of 0.3%. Register 0x55 provides the 6 bits of control for this purpose. Although this does not entirely alleviate the task of filling the ADC's

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full-scale, it helps the design process as you first design the front-end signal chain as precisely as the components would allow, and then better match the ADC's full-scale range to signal swing you're actually getting at the ADC's input in the final stages of the design. It is also helpful that this is a digital adjustment performed through the device configuration firmware.

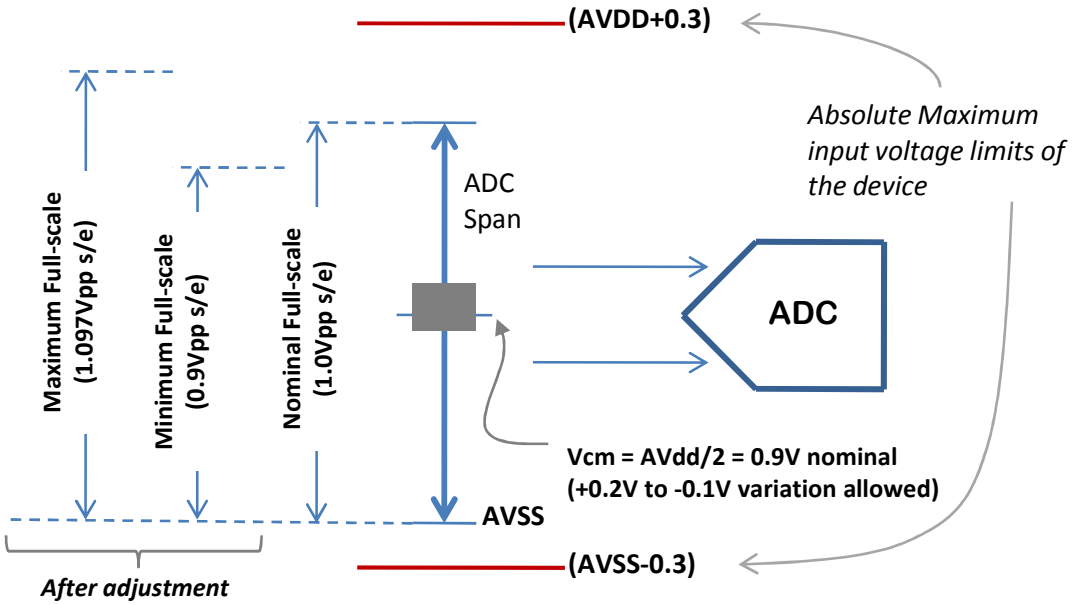

Figure 1: ADC Full-Scale Adjustment

How Much Signal Amplitude is Enough?

In most practical, high-speed signal processing systems, the receive signal enters the system at very weak strength and needs to be amplified significantly before it can be presented to the ADC for conversion to digital values. Normally, one would amplify the signal enough to utilize most of the ADC's span (full-scale) – as explained in the previous section. But a more accurate answer is that you amplify the signal enough to achieve your system SNR requirements. Now, assuming that during the system architecture phase one has selected an ADC that has just enough SNR for the system's requirements, both approaches lead to the same point. For example, if you have selected the HMCAD1511, an 8-bit converter with typical SNR in the 49dB range, and your system specifications require almost that amount of SNR, then you must design the front-end signal chain to present a signal to the ADC that is close to 1dB below full-scale (-1.0 dBFS) at its highest as that is the signal level at which the ADC achieves 49dB SNR. (Dynamic parameters in most ADC datasheets are specified at signal level of -1.0 dBFS).

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As the signal level drops below full-scale, the SNR (signal-to-noise ratio) performance of the ADC drops directly as the signal level is lower but the noise floor of the ADC remains approximately the same. This effect is shown in Figure 2 for an ideal 8-bit ADC.

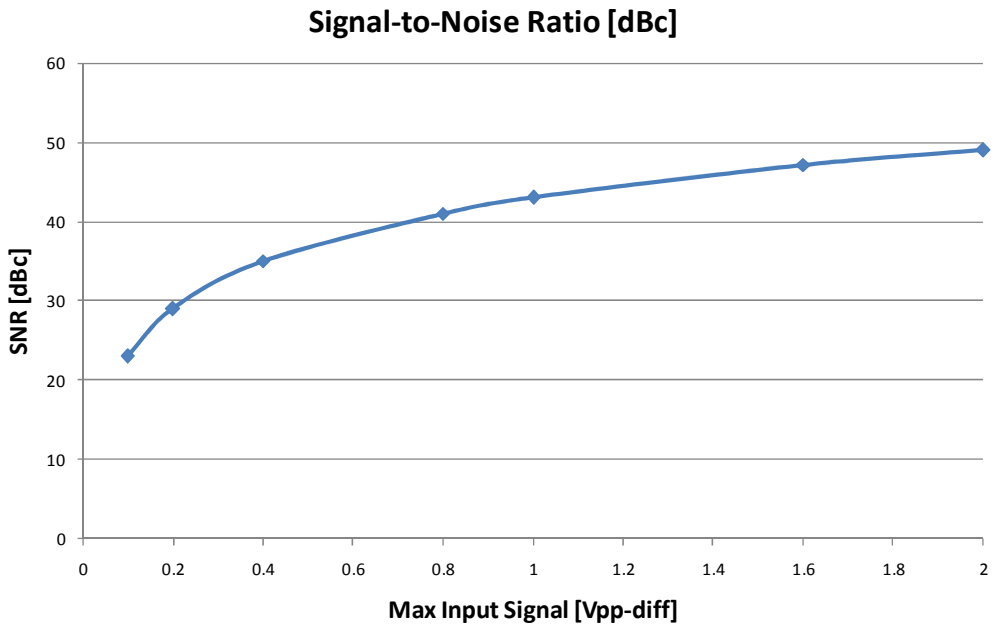

Figure 2: SNR degradation with lower signal levels for an ideal 8-bit ADC

As Figure 2 illustrates, there is a direct (dB-for-dB) loss in SNR in an ideal ADC as the input signal is lowered below the full-scale value. So if you want to utilize most of the ADC's SNR capability, you must amplify your maximum signal to a level close to the full-scale of the ADC. This is not only difficult to achieve, as explained in the previous section, it is also not the best region of the signal chain's operation from the standpoint of distortion – which we have ignored thus far in this discussion.

Not only the ADC, but most components in the signal chain leading up to the ADC, such as the DVGA or the driver amplifier just before the ADC, show higher distortion effects as the input signal gets closer to the full-scale. Figure 3 illustrates this effect with lab measurements of a Hittite ADC. It should be noted that the SNR and SNDR (Signal-to-Noise plus Distortion Ratio) are shown in units of dBFS in this plot. This is done to remove the gross effect of the signal level reduction – which has been illustrated in Figure 2.

[Note: The SNDR metric is mathematically interchangeable with ENOB (effective number of bits)].

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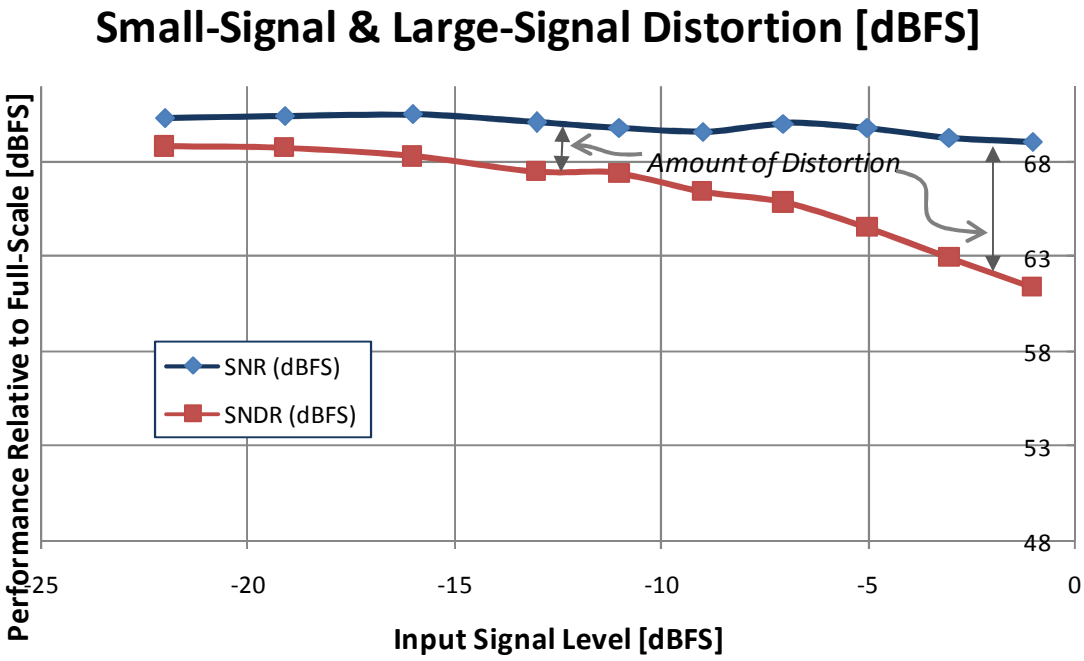

Figure 3: Distortion in an ADC worsens with larger input signal levels

Figure 4 shows the second harmonic distortion of a high-speed, wideband amplifier that is commonly used as a high-speed ADC driver. Here again, the distortion component gets markedly worse as the amplifier's output voltage amplitude is raised.

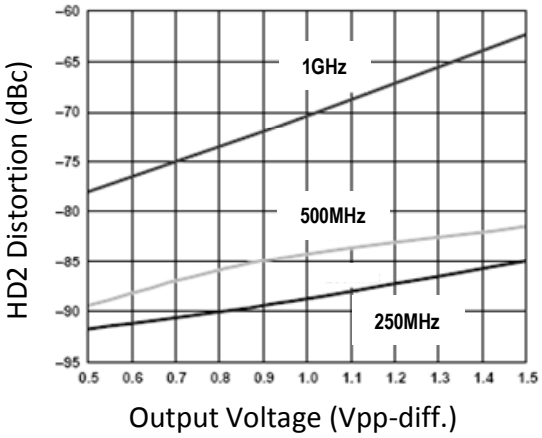

Figure 4: Amplifier distortion as a function of its output voltage amplitude

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Thus, there is a tradeoff the system engineer must face – trying to find a balance between sufficient SNR and tolerable distortion for the particular system's needs. This is where the HMCAD1511 family of ADCs brings a significant advantage with its digital gain feature. This feature is based on the fact that the HMCAD1511, though it is an 8-bit converter, has more resolution available in its core circuitry. This means that although the SNR available to the user is limited by the quantization noise floor of an 8-bit converter, the actual noise floor deep within the ADC's core is significantly lower than that.

The digital gain feature of these devices allows the system designer to take advantage of this fact by allowing him to operate at lower signal levels at the input of the ADC and then "gaining up the output signal" close to the full-scale *without a loss in the signal-to-noise ratio.* Figure 5 illustrates how the digital gain feature allows you to maintain the SNR close to the -1.0 dBFS specification of the HMCAD1511 as compared to the case of a typical 8-bit ADC, without the benefit of the digital gain feature, where the SNR degrades as the input signal level is lowered.

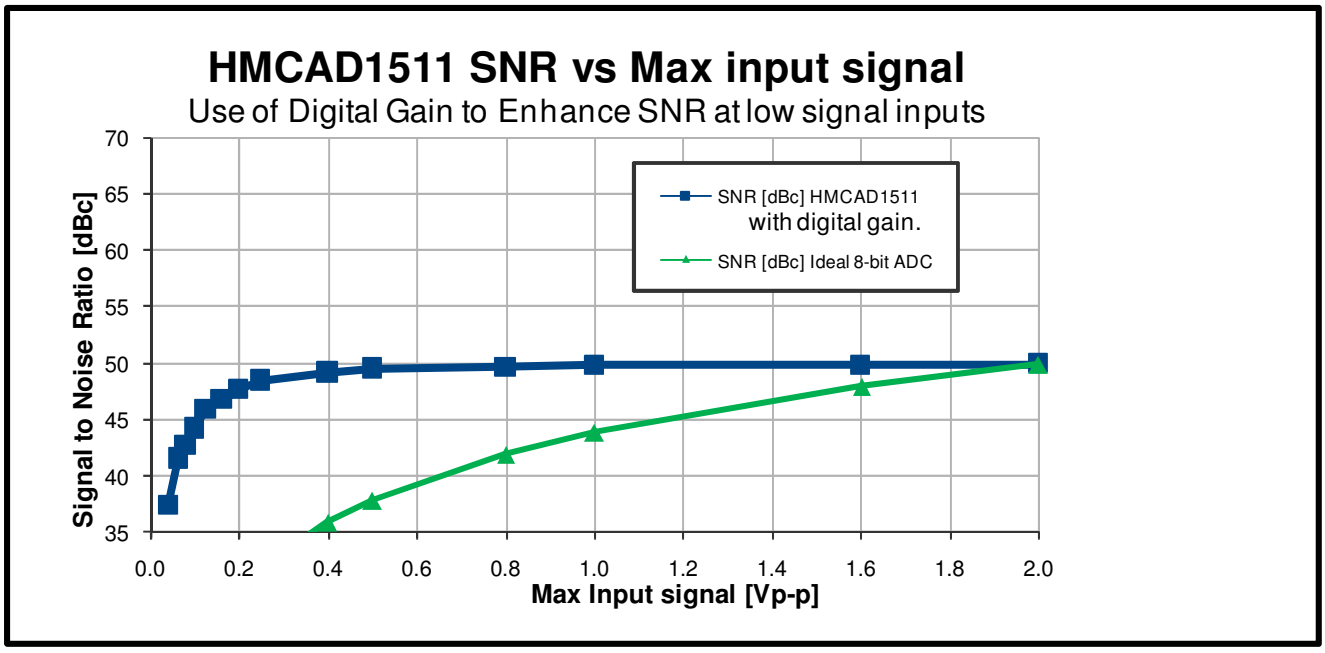

Figure 5: SNR performance of the HMCAD1511 with and without the use of Digital Gain

The digital gain of the HMCAD1511 is set to 1x by default upon power-up. The user can set it to higher values in registers 0x2A and 0x2B. Two different types of adjustments are allowed: x-gain (1x, 1.25x, 2x, 2.5x, 4x, 5x, 8x, 10x, …32x); or dB-gain (0dB through 12dB in steps of 1dB). Separate digital gain settings are provided for each ADC input. Lab testing has shown that gain settings up to 8x (corresponding to 0.25Vpp-diff. input full-scale) show minimal loss in SNR (as evident in Figure 5). SNR

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in dBc starts to degrade rapidly beyond digital gain of 10x, so the user is advised to keep the digital gain setting at 10x or less. In actual practice, considering the distortion performance of the amplifiers, DVGAs, and the ADC itself, one should not have to go to an input signal full-scale of less than 0.5Vpp-diff. – which corresponds to a digital gain setting of 4x.

As an example, one may design the signal chain front-end with a maximum signal at the ADC input of up to 0.5Vpp-differential (or -12dBFS) and thus obtain notably better distortion performance from the front-end circuitry as well from the HMCAD1511. In this case the digital gain in the ADC would be set to 4x or 12dB and the ADC's digital output will exhibit SNR that is specified in the datasheet for input signal levels of -1.0dBFS – i.e., about 49dBc. It should be noted that in such a case the ADC's digital output will over-range at 0.5Vpp-differential input signal level.

Another Use of the Digital Gain

One may think of the digital gain feature as performing the same function after the ADC as the DVGA (digital variable gain amplifier) device does in front of the ADC. Since the digital gain of the HMCAD1511/13 ADC can be changed by the user through the SPI interface 'on-the-fly', much as one controls the gain of a DVGA, same gain control can be accomplished post-ADC in the digital domain and a discrete DVGA device may not be necessary at all. This is certainly possible, but it should be noted that the SPI interface would introduce some additional time delay to the gain control loop. At the same time, the mere fact that the gain adjustment is being made *after* the ADC means that the gain control loop actually has to react more quickly in order to keep the ADC's digital output from saturating. (The signal chain front-end design has to assure regardless that the ADC's analog inputs are not overloaded beyond the nominal 2.0Vpp differential level. So this techniques has no effect on that aspect of signal-chain design). The user should also be cautioned that the digital gain adjustments take effect immediately and could even cause transitional 'code spikes' in the digital data that may be problematic for the digital signal processing circuitry.

For these reasons this technique would make sense in only those applications where gain control requirements are not very demanding.

Conclusion

The HMCAD1511/12/13 family has been shown to offer a significant benefit to the system designer with its digital gain feature. With this feature, owing to the HMCAD1511 family's greater internal resolution, a much better balance can be achieved between receive channel SNR and distortion – something not possible with other 8-bit analog-to-digital converters.

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