

SELECTING PRESCALERS For PLL SYNTHESIZERS

Selecting Prescalers For PLL Synthesizers

Prescalers are frequency dividers used in RF and microwave frequency translation and signal generation. They are commonly employed in phase-locked loops (PLLs) and frequency synthesizers to match the frequency of a high-frequency source to that of a reference oscillator. By understanding how to bias and operate prescalers, they can be effectively designed into a wide range of high-frequency applications.

The modulus or divide ratio is a fundamental prescaler parameter. Fixed modulus prescalers having a modulus equal to an integer power of 2 (i.e. 2, 4, 8...) allow the highest input-frequency handling capability compared to other integer division ratios. For example, a new line of monolithic-microwave-integrated-circuit (MMIC) prescalers from Hittite Microwave Corp. (Chelmsford, MA) feature high input-frequency capabilities to 13 GHz. The prescalers, which are available in chip form or in low-cost plastic packages, are fabricated with a low-noise InGaP GaAs heterojunction-bipolar-transistor (HBT) process.

A simplified block diagram of one of these MMIC prescalers is shown in Fig. 1. In addition to the fixed digital frequency divider network, which is implemented using flip flops, the prescaler includes amplifiers on the input and output sides. These amplifiers are configured with complementary pairs to allow either single-ended or differential-mode operation at the input and output ports. The die form of the prescalers includes three control terminals for the following functions: input disable, DC power down, and RF output power level select.

The small size of the chip prescalers makes them useful for compact multichip module (MCM) packaging configurations. On the other hand, the chip form requires more critical die attach and wire-bonding assembly processes, while the plastic package devices are compatible with conventional high-speed automatic surface-mount-technology (SMT)

assembly equipment. Add to this the ruggedness of the plastic package MMIC prescaler, and it becomes the configuration of choice for use in many types of microwave assemblies intended for low-cost, high-volume applications. The HBT prescalers are designed for use with a single +5 VDC $\pm 5\%$ supply. The +5 VDC supply should be well conditioned to minimize degradation of phase noise, and free from over-voltage transients that could damage the prescaler.

The +5 VDC prescalers include an internal monolithic 15 pF power-supply decoupling capacitor. However, a pair of external decoupling capacitors connected between the Vcc terminal and ground is highly recommended. To bypass lower frequencies, one capacitor should be relatively high in capacitance. For example, a 1-to-10- μ F tantalum chip or multilayer ceramic capacitor is recommended. The second capacitor should be relatively low in capacitance (such as 300 pF) to effectively bypass high frequency components and to minimize prescaler input-to-output coupling.

The two decoupling capacitors, especially the lower capacitance one, should be placed as close as possible to the Vcc connection on the prescaler. The connection from the ground electrode of the capacitors to the circuit ground plane should be kept short. For chip prescalers, a single-layer 300-pF capacitor is recommended. The ground side of the single-layer capacitor should be attached to the carrier using conductive epoxy, or AuSn eutectic solder, then make the connection to at least one of the Vcc pads on the chip using one or more wire bonds.

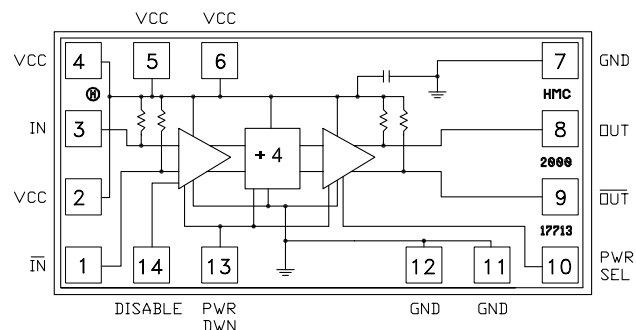


FIGURE 1. This block diagram shows the control terminals for a high-frequency MMIC prescaler.

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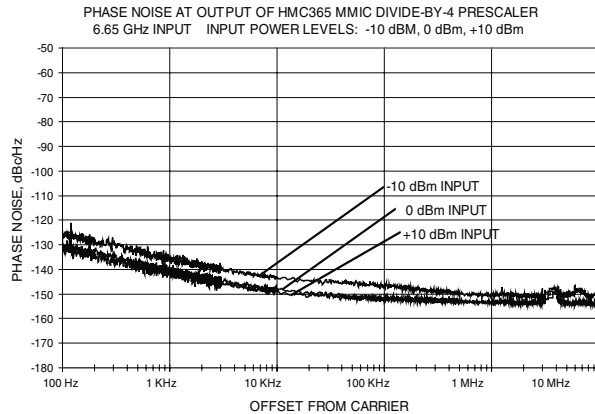


FIGURE 2. The phase noise for a divide-by-four prescaler was measured for three different input power levels.

For normal prescaler operation, the Power Down control terminal, present only on the bare die form devices and not on the plastic package parts, must be grounded. Applying +5 VDC to this pin will place the entire device into a power-down standby mode in which the DC current consumption is reduced to a few milliamps. The DC Power Down terminal can be controlled electronically with the output of a CMOS logic gate operating with a +5 VDC supply, or by connecting it to an open collector logic device with a 1 K ohm pull-up resistor tied to the +5 VDC supply. The nominal source current required from the +5 VDC control signal to this input is less than 1 mA.

The nominal AC input impedance for each of the two differential prescaler inputs is a resistive 50 ohms referenced to ground. Although these are differential input ports, the prescaler can also be operated as an unbalanced (single-ended) device.

Both prescaler input lines must be DC blocked from external circuitry. In the prescaler's internal circuitry, these inputs are DC coupled, with precisely controlled DC operating levels. Any external DC connection to the input lines can disturb these critical DC operating levels and degrade or disable operation of the device. If the input signal lines are already DC blocked by other circuitry at the source of the prescaler input signal, then DC blocking capacitors at the prescaler input can be omitted. This may be the case when the input lines are fed by microstrip coupled-line filters, highpass filters, or from other circuitry that effectively provides a DC block.

The capacitance and style of the DC blocking capacitors should be properly selected to not cause significant attenuation of the input signal. There are several standard guidelines to follow:

1. Select a capacitance value which, for the lowest frequency at which the prescaler will be operated, presents a value of reactance which is small relative to 50 ohms, say 3 ohms or less. For example, if 10 GHz is the minimum input frequency, at least 5 pF DC blocking capacitance should be used. For a minimum input frequency of 1 GHz, at least 50 pF capacitance should be used.
2. From the vendor's data for the capacitor, check that its self-resonant frequency (SRF) is higher than the highest input frequency at which the prescaler will be operated. For DC blocking, it may be acceptable to operate at or somewhat above the series SRF of a capacitor. To avoid potential problems, however, this practice should be avoided.
3. For best performance, select a capacitor style specified by the manufacturer for operation at microwave frequencies.

For single-ended input operation, either of the prescaler's two input terminals (IN or IN Complement) may be used. The input line selected must be DC blocked in the same manner as described for differential-mode input connections. The prescaler will operate with the unused input terminal left open-circuited, but this is not recommended. Instead, for single-ended input operation, the unused input terminal should be AC grounded by connecting it through a DC blocking capacitor to ground to improve input sensitivity. The capacitor can be the same type used for the DC block on the active RF input line.

A prescaler's data sheet will provide a recommended operating window for input power. Typically, a device will operate over a greater than 25 dB range of input power levels. However, towards the specified upper frequency range of the device, the window is reduced in range to about 10 dB. For differential-mode input operation, the input power range in the data sheet refers to total power from the two input lines, not the power on each line.

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At the lower end of the recommended input power operating window, the prescaler's output phase noise will begin to degrade. As an example, the output phase noise of a model HMC365 divide-by-four prescaler from Hittite Microwave Corp. was characterized for three different single-ended input-power levels at 6.65 GHz (Fig. 2). The output phase noise first decreases for increasing input power level. Then, above an input power level of 0 dBm, the improvement in phase noise flattens out. Thus, for phase-noise critical applications, it is better to operate this particular prescaler at input power levels of 0 dBm or above, although input power levels above the recommended maximum should be avoided. As the input power increases beyond the rated maximum level, spurious signals will begin to appear at the prescaler's output port. As the input power is further increased, at some level the device will become overstressed, and device degradation may result.

When possible, differential prescaler connections should always be made. To use only one side of an available differential input pair is effectively throwing away one-half of the input signal power, and input power level may be at a premium. In addition, the differential mode of operation on the input side may provide some rejection of common-mode noise present on the input lines.

A MMIC prescaler offers a substantial amount of gain at its input and output ports. For conditions of no RF input signal, or inadequate RF input signal level, the prescaler may go into a low-level uncontrolled oscillation. The general cause of this is feedback from device output to input in the presence of

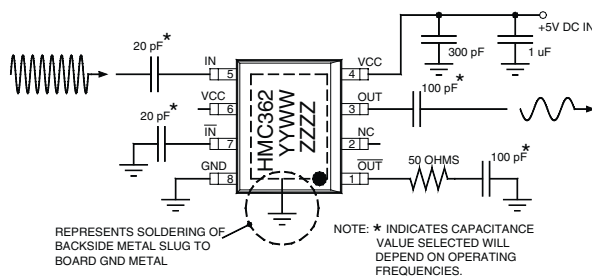


FIGURE 3a. The external connections for this plastic-packaged prescaler are configured for single-ended operation.

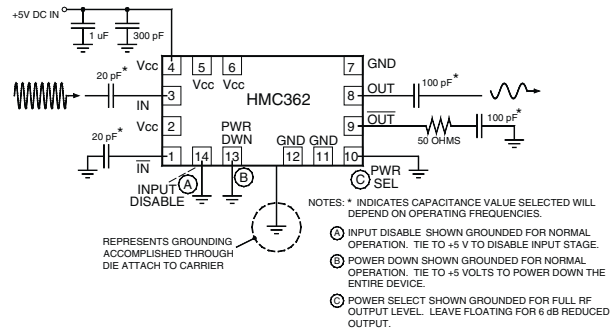


FIGURE 3b. The chip version of the prescaler is also configured for a single-ended operation.

the high device gain. Prescaler self-oscillation can be avoided by providing an input signal of sufficient amplitude (as specified on a product data sheet).

For applications where an input signal is not continuously present, self-oscillation can be suppressed by active control of the Input Disable function (available on the chip prescalers only). For normal operation, the Input Disable pin must be grounded. (On plastic-packaged prescalers, the Input Disable pin is permanently grounded internally.) When +5 VDC is applied to the chip Input Disable pin, the output port of the prescaler's input amplifier is forced to a predetermined logic state, effectively placing the prescaler into a hold state, with one complementary output set at high and one set at low.

For high-speed operation, the Input Disable pin can be driven by the output of a CMOS logic gate, or by connecting it to an open collector output of a logic device with a 10 K ohm pull-up resistor tied to the +5 VDC supply. The nominal source current required from the +5 VDC control signal to drive the Input Disable is less than 0.1 mA.

The output lines of the MMIC prescalers are also configured as a differential pair. The nominal RF output impedance of each output line is 50 ohms. Single-ended loads can be driven by simply using only one of the two output terminals. Being a digital device, the prescaler's output signal levels are independent of the input power level, as long as the prescaler is used within its specified input signal range. There are some output power variations as a function of frequency, however, as noted on each product data sheet (as specified for single-ended

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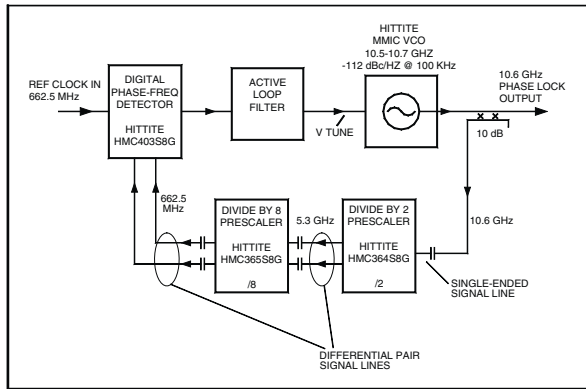


FIGURE 4. This phase-locked 10.6-GHz oscillator was developed as a reference clock for SONET applications.

outputs). When properly configured to drive a differential load, the prescaler can deliver double the single-ended output power.

As with the input lines, the prescaler's output signal lines must be DC blocked. The same guidelines for selecting the input DC blocking capacitors can be applied to the choice of output DC blocking capacitors. However, the frequency at the output is lower than at the input, and consequently the resulting minimum required capacitance value will be higher, by a factor equal to the division ratio.

For single-ended operation, there are two options for the unused output terminal. It can be left in an open-circuit condition, which is not recommended. Or a 50 ohms DC-blocked RF termination can be provided for this output terminal by connecting it to a 50 ohms resistor in series with a DC blocking capacitor, one side of which is grounded. The second approach helps reduce reverse signal leakage, which is the appearance of the lower-frequency prescaler output signals (essentially spurious signals) at the prescaler's higher-frequency input ports.

In some cases, this spurious distortion could propagate backward through a design and degrade signals in circuitry prior to the prescaler input terminals. Reverse leakage is normally characterized on a product data sheet as a function of frequency for the two conditions of the unused output port: terminated and unter-

minated. With the output of the prescaler operated in differential mode into a load with 50 ohms impedance per leg, the two output terminals are effectively terminated and a minimum reverse-leakage condition is achieved.

High-speed logic devices that are designed to work with differential input signals can be used with the prescaler in differential output mode. The Output Power Select control terminal allows selection between two prescaler output-level operating modes. Direct DC grounding of the Output Power Select terminal provides full RF output power, while leaving the Output Power Select terminal in an open-circuit condition results in a reduced output power mode, with about 6 dB reduction in output level compared to the full-level mode. In the reduced RF output power mode, the DC current drawn by the prescaler drops by about 20 mA. The reduced-output mode can be useful in those applications where DC power consumption is critical. The Output Power Select line is generally not directly controllable by standard logic gate outputs. Normally, this line will be hard wired to ground for full-power operation, or left open-circuited for reduced output power operation.

The packaged prescalers are supplied in an eight-lead SOIC surface-mount housing (Fig. 3a). An exposed rectangular copper alloy slug on the bottom side of the package is plated with tin-lead

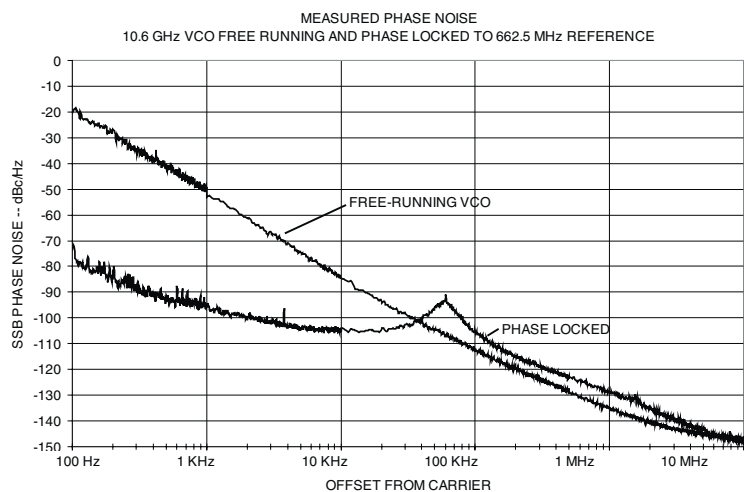


FIGURE 5. The measured phase noise of 10.6 GHz PLL oscillator is compared with the phase noise of the free-running (unlocked) 10.6-GHz VCO.

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(Sn/Pb) solder. The metal slug provides a good RF ground and is the primary heat transfer interface for the MMIC.

Improper connection from the metal ground slug to a printed circuit board can result in reduced bandwidth performance as well as device overheating. The metal slug on the package must be soldered to a rectangular metal pad on the circuit board. The pad must be both a good RF ground, and a good heatsink. The size of the rectangular metal pad should be about the same size as the exposed metal slug on the package. For good heatsinking, the ground pad on the circuit board should include plated metal via holes extending to another large area of grounded metal on the board, such as a ground plane.

Soldering of this ground slug of the plastic package to the circuit board is best accomplished using solder paste and a solder reflow process. Because the exposed surface of the metal slug is coated with Sn/Pb solder, electrically conductive epoxy (which is not compatible with Sn/Pb solder) must not be used for the attachment. A soldering iron is not suitable for this attachment process because the surfaces to be bonded are not exposed for contact with the soldering iron. For prototype work, a hotplate may be used to achieve solder reflow, but a controlled reflow oven process is preferred.

The eight metal leads of the plastic package are also solder coated, so these leads must also be bonded to the circuit board traces with solder (but not with conducting epoxy). The lead labeled GND is connected internally to a grounded metal pad on the prescaler chip. This lead should be soldered to a grounded metal pad on the circuit board.

The back side of the die, and the bonding pads on the top side of the die, are gold metallized. The 4-mil-thick chips feature 1 mil of backside metal. The bonding pads on the top side of the chip are 4x4 mil squares. The die may be attached to a metal carrier using either AuSn eutectic solder or electrically conductive epoxy. Several bonding pads on the prescaler chip (identified as GND) are ground pads that are connected within the chip directly to the backside grounded metal on the device. With the die attached with AuSn eutectic solder or electrically conductive

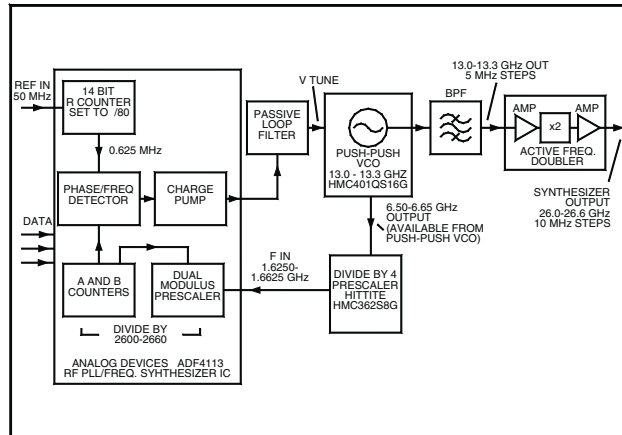


FIGURE 6. This 26.0-to-26.6-GHz frequency synthesizer was constructed with a divide-by-four prescaler and a commercial fractional-N synthesizer IC.

epoxy directly to a circuit carrier, it is not necessary to run bond wires to these pads. The pads can be used as bonding points for grounding other circuit elements if necessary.

The phase noise characteristics of a prescaler should be well understood when the device is used in phase-noise-critical applications. There are three basic processes to keep in mind:

1. Theoretical analysis of a divide-by-N frequency divider shows that the output signal phase noise, expressed on a per hertz basis and referenced at the same frequency delta from the carrier, is reduced by $20\log_{10}(N)$ dB, compared to the phase noise of the input signal. (Recall that for a times N frequency multiplier, the phase noise is increased by the same $20\log_{10}(N)$ dB factor.)
2. Due to thermal noise, 1/f noise processes, etc., there will always be some degradation of the output signal phase noise from the prescaler relative to the theoretical value. As seen in Fig. 2, the phase noise added by a prescaler to a synthesizer is small and usually negligible.
3. Noise on the DC power supply line can be a significant source of phase noise degradation. Good device decoupling should always be used, along with proper power line filtering, shielding, and grounding for the PCB layout.

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Examples of plastic-packaged and chip prescalers with connections configured for single-ended input and output operation are shown in Figs.3a and 3b, respectively. For the chip, the three control terminals (Input Disable, Power Down, and Output Power Select) are configured for full-output-power operation.

Hittite Microwave Corporation offers evaluation boards, primarily for the plastic-packaged prescalers, although they can also be configured for chip prescalers. The fully assembled boards, which are set up for 50 ohm single-ended input operation, include the prescaler, DC blocking capacitors, decoupling capacitors, and SMA input and output connectors. A user need only apply an RF signal and DC power, and RF output signals are available at SMA connectors.

As an example of the type of design possible with these prescalers, a 10.6 GHz phase-locked oscillator for a frequency reference requirement in a Synchronous Optical Network (SONET) OC-192 (10 Gb/s) optical communications system was constructed (Fig. 4). It is based on two Hittite prescalers: a divide-by-2 unit followed by a divide-by-8 unit. The 10.6 GHz VCO in this circuit is a proprietary design, although other tunable sources, such as

a hybrid circuit varactor-tuned dielectric resonator oscillator (DRO) assembly, can be substituted. The HMC403S8G digital phase-frequency detector is a standard Hittite MMIC, developed for high-frequency, low-phase-noise applications. Each of the three MMICs is housed in a surface-mount plastic package. Figure 5 compares the phase noise of the free-running VCO and the PLL.

Figure 6 shows a block diagram for a microwave frequency synthesizer designed and fabricated using a plastic-packaged model HMC362S8G divide-by-4 MMIC prescaler, along with a commercial fractional-N synthesizer IC from Analog Devices (Norwood, MA). The phase noise of the synthesizer was measured (Fig. 7) with a 3048A test set from Agilent Technologies (Santa Rosa, CA). The prescaler delivers an output signal which is sufficiently low in frequency for the synthesizer IC to process. In this circuit, at the point before the active frequency doubler, the circuit is essentially a 13.0-to-13.3 GHz frequency synthesizer with 5 MHz frequency steps. The addition of the x2 active multiplier turns it into a 26.0-to-26.6 GHz synthesizer with 10 MHz steps. The measured phase noise at 26 GHz is suitable for systems employing 16-state quadrature-amplitude modulation (16QAM).

The VCO in this synthesizer is the company's model HMC401QS16G MMIC. The push-push source generates an internal signal that is one-half the output frequency. An integrated active doubler delivers the desired frequency range. Active multipliers in this frequency range are also available in hybrid form from a variety of manufacturers.

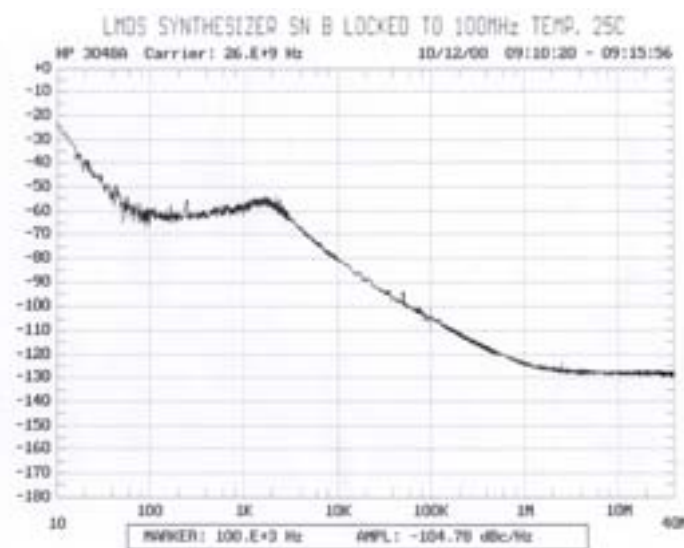


FIGURE 7. The measured phase noise of the 26.0-to-26.6-GHz frequency synthesizer is shown for offset frequencies from 10 Hz to 40 MHz.

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