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Adaptive Response Cycle Optimization for A²B Plug-and-Play Node Discovery

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Introduction

The A²B® bus protocol supports daisy-chained audio networks in automotive, industrial, and consumer applications. Dynamic network applications require a Plug-and-Play (PnP) method of discovery that detects each node and configures it automatically on the bus. Reliable PnP discovery requires each node in the chain to be assigned a Response Cycle (RESPCYCS) register value matched to the physical cable length — a parameter unknown at design time. This note describes an adaptive, sweep-based algorithm that discovers and tunes RESPCYCS for each node in sequence without prior topology knowledge, and the staged software architecture used to implement and validate it.

In this document and the procedures outlined in it, it is assumed that the application hardware conforms to the reference design as detailed in the *AD2437 Automotive Audio Bus (A²B®) System Specification Manual*[2] or our evaluation hardware. This example uses the RJ45 connector implementation and EVAL-AD2437A1MZ for the main node and EVAL-AD2437B1MZ for subordinate nodes.

Background

An A²B network consists of one main node and up to 16 subordinate nodes connected in a daisy-chain topology over a single twisted-pair cable. In the network discovery phase, the main node initiates discovery by issuing a DISCVRY command with a candidate RESPCYCS value. If a subordinate node is present and the RESPCYCS value is sufficient to cover the cable propagation delay, the subordinate node locks its PLL and the main node receives a DSCDONE interrupt. If RESPCYCS is not sufficient, no response is received and a timeout occurs.

The value in the RESPCYCS register defines the relative time from the start of a synchronization control frame (SCF) to the moment the last subordinate node responds with a synchronization response frame (SRF). It indicates when earlier nodes can expect the response from the last subordinate node. If the last node does not respond, the previous node that is next to the presumed last node does respond.

In a fixed installation with known cable lengths, the value in the RESPCYCS register can be calculated analytically. When a dynamic system is required and nodes are actively added and removed, the discovery process needs to be plug-and-play. In the scenario where cable lengths vary, connections are field-swapped, and topology is unknown the value must be determined empirically at runtime for each link in the chain.

A²B transceivers have a built-in auto calibration mechanism that can lock onto the SRF with a window of -4 and +15-bit times. This covers a wide range of cable lengths but has some limitations when adding new nodes to the system. It only adjusts during discovery and when the response cycle register is written to. The asymmetry of the window also favors cables that are shorter than expected. For systems with one or two subordinate nodes, setting the response cycles for a 4m cable length is sufficient, but for systems

with more subordinate nodes, the SRF will start to fall outside of this window, and upstream nodes will drop when trying to discover new nodes to the network.

Staged Discovery Algorithm

The algorithm discovers nodes one at a time in a staged loop. For each stage N, the upstream node (N−1) is placed in switch mode 1 to comply with two-step discovery. Refer to the *AD2437 Automotive Audio Bus (A^2B®) System Specification Manual[2]*. The node is also put in switch bypass mode.

Starting with a response cycle setting that correlates to the longest supported cable length, 9 counts below the upstream node's operational RESPCYC value, the DISCVRY register is written to. If a DSCDONE interrupt is not received, a new value must be attempted. To prevent an upstream node from dropping, first the system must be stabilized. SWCTL.0 = 0 is written to the current end node, stopping the discovery process. To reset the auto calibration of upstream nodes, all response cycle registers to every node currently discovered are incremented and then decremented. A health check is completed on all nodes to verify that they are still active on the network by reading the VENDOR register.

This process is repeated by increasing the response cycle value by one and writing to DISCVRY.

If a DSCDONE interrupt is received, the upstream node B port is turned off and then on again with switch bypass mode disabled, and another discovery attempt is made with the previous value incremented by 1. This is an empirical adjustment based on test data. The new node is configured and ENDDSC is written to the main node.

The difference between the response cycle setting of the previous node minus the value of the newly discovered node is referred to as the delta (Δ) .

$$\Delta = \text{RESPCYCS}_{\text{upstream}} - \text{RESPCYCS}_{\text{tuned}}$$

The delta represents the additional response cycles consumed by the new cable segment. A larger delta indicates a longer cable run.

To accommodate all upstream nodes for the additional delay added by the new node, all upstream nodes need to have their response cycle value boosted by half of the delta.

$$\text{boost} = \lfloor \Delta/2 \rfloor$$

The full margin stack for the newly discovered node is therefore:

$$\text{RESPCYCS}_{\text{operational}} = \text{RESPCYCS}_{\text{first DSCDONE}} + 1 + \lfloor \Delta/2 \rfloor$$

This process also resets the auto calibration, so when a discovery is successful, there is no need to increment and decrement the response cycle value as is done with a failed discovery attempt. A wellness check can also be completed to verify no nodes have been dropped from the system.

Discovery Process Example and Description

The following example is the discovery of a five-node system consisting of one main node and four subordinate nodes. The cable lengths used are 20 ft between main and subordinate node 0; 100 ft between subordinate nodes 0 and 1; 50 ft between subordinate nodes 1 and 2; and 20 ft between subordinate nodes 2 and 3.

Follow the steps below:

[0a] Initial Main Reset — Four soft resets clear the chip and flush any stagnant states by writing CONTROL.2 = 1. A final CONTROL write, with NEWSTRCT and MSTR bits high, enters main active mode.

This is where the transceiver must be set up for RJ45 connectors (CONTROL.4 = 1) or XLR connectors (CONTROL.4 = 0).

In this example RJ45 connectors are used.

[0001] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X91

[0002] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X94

[0003] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X94

[0004] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X94

[0005] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X94

[0006] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X91

[0007] A2BREAD <- MAIN, VENDOR(0X02), DATA=0XAD

[0b] Main Preconfigure Default — Default register initialization: Interrupt pending and mask registers are cleared; MBOX1CTL and initial RESPCYCS are written.

The initial response cycle setting is arbitrary, and the working value is primarily data dependent. Starting with a value of 0x80 leaves a good amount of room for downstream and upstream data.

[0008] A2BWRITE_BURST -> MAIN, INTPND0(0X18), DATA=[0XFF, 0XFF, 0X0F]

[0009] A2BWRITE_BURST -> MAIN, INTMSK0(0X1B), DATA=[0XFF, 0X00, 0X0F]

[0010] A2BWRITE -> MAIN, MBOX1CTL(0X96), DATA=0X02

[0011] A2BWRITE -> MAIN, INTPND2(0X1A), DATA=0X1A

[0012] A2BWRITE -> MAIN, RESPCYCS(0X0F), DATA=0X80

[0c] User Specific Settings — This is a placeholder for application-specific main node configuration of I2SGCFG, I2SCFG, PLLCTL, and SLOTFMT registers. Currently sets I2SGCFG = 0x20.

This is where the system specific settings, with respect to the serial I/O and GPIO ports, are programmed.

[0013] A2BWRITE -> MAIN, I2SGCFG(0X41), DATA=0X20

[0014] A2BWRITE_BURST -> MAIN, INTMSK0(0X1B), DATA=[0XFF, 0X00, 0X0F]

[0d] Upstream B-Port Initialization — For use with two-step discovery as recommended for RJ45 and XLR connectors, switch bypass mode must be enabled. Use a read-modify-write command to set this part of the control register to protect the other settings in the register.

Set CONTROL.3 = 1 for switch bypass mode. SWSTAT2 is read to confirm switch power state, SWCTL = 0x11 to enable the B port and begin SCFs downstream.

A 100 ms settle allows the downstream node to lock its PLL from the SCFs generated by the upstream node.

Interrupts are also cleared to make sure that any new interrupts are related to the discovery process.

[0015] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X99

[0016] A2BREAD <- MAIN, SWSTAT2(0XA5), DATA=0XA0

[0017] A2BWRITE -> MAIN, SWCTL(0X09), DATA=0X11

[0018] A2BREAD <- MAIN, INTMSK0(0X1B), DATA=0XFF

[0019] A2BWRITE -> MAIN, INTMSK0(0X1B), DATA=0XFF

[0020] A2BWRITE -> MAIN, INTPND0(0X18), DATA=0XFF

[0021] A2BWRITE -> MAIN, INTPND1(0X19), DATA=0XFF

[0022] A2BWRITE -> MAIN, INTPND2(0X1A), DATA=0XFF

[1a] Subordinate Node 0 Discovery — Because the response cycle relationship between subordinate node 0 and the main node is unique in the network, subordinate node 0 is discovered with a default value of one less than the main node. For this example, this is 0x80 - 1 = 0x7F.

There are no further tuning steps for subordinate node 0. This helps compensate for the asymmetry in the auto calibration for longer cables. If a node is connected, DSCDONE is received (INTSRC = 0x80 and INTTYPE = 0x18) immediately; the main node connection is cycled and subordinate node 0 is re-discovered with switch bypass mode disabled.

[0023] A2BWRITE -> MAIN, DISCVRY(0X13), DATA=0X7F

[0024] A2BREAD <- MAIN, INTSRC(0X16), DATA=0X80

[0025] A2BREAD <- MAIN, INTTYPE(0X17), DATA=0X18

[0026] A2BWRITE -> MAIN, SWCTL(0X09), DATA=0X10

[0027] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X92

[0028] A2BWRITE -> MAIN, SWCTL(0X09), DATA=0X11

[0029] A2BWRITE -> MAIN, INTPND0(0X18), DATA=0XFF

[0030] A2BWRITE -> MAIN, INTPND1(0X19), DATA=0XFF

[0031] A2BWRITE -> MAIN, INTPND2(0X1A), DATA=0XFF

[0032] A2BWRITE -> MAIN, DISCVRY(0X13), DATA=0X7F

[0033] A2BREAD <- MAIN, INTSRC(0X16), DATA=0X80

[0034] A2BREAD <- MAIN, INTTYPE(0X17), DATA=0X18

[1b] Subordinate Node 0 Configuration — Each new node discovered in the network is programmed with a series of writes to the main node and they go to the subordinate node through the A^{2}B link. Refer to the *AD2437 Automotive Audio Bus (A^{2}B®) Transceiver Technical Reference Manual[1]* for more details on this process.

These commands include necessary default configuration writes and custom writes that are application specific. Due to the way A^{2}B systems are managed, it is critical to complete the discovery process for each new node. Discovery of subordinate node 0 ends when ENDDSC is written (CONTROL.1 = 1) to the main node.

[0035] A2BWRITE -> SUB0, RESPCYCS(0X0F), DATA=0X7F

[0036] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X91

[0037] A2BWRITE -> MAIN, INTPND2(0X1A), DATA=0X01

[0038] A2BREAD <- SUB0, VENDOR(0X02), DATA=0XAD

[0039] A2BWRITE -> SUB0, RESPCYCS(0X0F), DATA=0X7F

[0040] A2BWRITE -> MAIN, SWCTL(0X09), DATA=0X21

[0041] A2BWRITE -> SUB0, MMRPAGE(0XE0), DATA=0X01

[0042] A2BWRITE -> SUB0, CHIP(0X100), DATA=0X02

[0043] A2BWRITE -> SUB0, MMRPAGE(0X1E0), DATA=0X00

[0044] A2BWRITE -> SUB0, MMRPAGE(0XE0), DATA=0X01

[0045] A2BWRITE -> SUB0, MMRPAGE(0X1E0), DATA=0X00

[0046] A2BWRITE -> SUB0, I2SGCFG(0X41), DATA=0X20

[0047] A2BWRITE -> SUB0, MBOX1CTL(0X96), DATA=0X02

[0048] A2BWRITE -> SUB0, INTPND0(0X18), DATA=0XFF

[0049] A2BWRITE -> SUB0, SWCTL(0X09), DATA=0X10

[0050] A2BWRITE_BURST -> SUB0, INTMSK0(0X1B), DATA=[0X00, 0X00]

[0051] A2BREAD <- MAIN, INTSRC(0X16), DATA=0X00

[0052] A2BWRITE -> MAIN, SWCTL(0X09), DATA=0X11

[0053] A2BWRITE -> MAIN, I2SGCFG(0X41), DATA=0X20

[0054] A2BWRITE_BURST -> MAIN, INTMSK0(0X1B), DATA=[0X50, 0X00, 0X09]

[0055] A2BWRITE -> MAIN, SLOTFMT(0X10), DATA=0X44

[0056] A2BWRITE -> MAIN, INTPND0(0X18), DATA=0XFF

[0057] A2BWRITE -> MAIN, INTPND1(0X19), DATA=0XFF

[0058] A2BWRITE -> MAIN, INTPND2(0X1A), DATA=0XFF

[0059] A2BWRITE -> MAIN, DATCTL(0X11), DATA=0X03

[0060] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X92

[1c] Subordinate Node 0 Boost – While the relationship between the response cycle value of the main node and subordinate node 0 is unique and is not cable length dependent, a boost is still required before adding a new node to the system. A default boost of +2 for the main and subordinate node 0 is used and is written regardless of the existence of a second subordinate node. Note that changes to response cycle registers do not take effect until NEWSTRCT is written (CONTROL.0 = 1). A system health check is done to complete the discovery process of subordinate node 0.

[0061] A2BWRITE -> MAIN, RESPCYCS(0X0F), DATA=0X82

[0062] A2BWRITE -> SUB0, RESPCYCS(0X0F), DATA=0X81

[0063] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X91

[0064] A2BREAD <- MAIN, VENDOR(0X02), DATA=0XAD

[0065] A2BREAD <- SUB0, VENDOR(0X02), DATA=0XAD

[2a] Subordinate Node 1 Pre-Discovery — Interrupts are cleared and NEWSTRCT is written. These steps may prove to be redundant with time but are being kept for now.

Subordinate node 0 is put in switch bypass mode and its B Port is activated by writing 0x11 to SWCTL.

Subordinate node 0 interrupts are cleared.

[0066] A2BWRITE_BURST -> MAIN, INTMSK0(0X1B), DATA=[0XFF, 0X00, 0X0F]

[0067] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X91

[0068] A2BWRITE -> SUB0, CONTROL(0X12), DATA=0X18

[0069] A2BREAD <- SUB0, SWSTAT2(0XA5), DATA=0X20

[0070] A2BWRITE -> SUB0, SWCTL(0X09), DATA=0X11

[0071] A2BWRITE_BURST -> SUB0, INTMSK0(0X1B), DATA=[0X80, 0X00]

[0072] A2BREAD <- SUB0, INTMSK0(0X1B), DATA=0X80

[0073] A2BWRITE -> SUB0, INTMSK0(0X1B), DATA=0X00

[0074] A2BWRITE -> SUB0, INTPND0(0X18), DATA=0XFF

[2b] System Auto Calibration Reset — The response cycles in the system were just boosted, so this step is redundant for the first iteration, but must be done at the beginning of the loop in case more discovery attempts are needed. The response

cycle register in each node is incremented and then decremented to reset the auto calibration.

[0075] A2BWRITE -> MAIN, RESPCYCS(0x0F), DATA=0x83

[0076] A2BWRITE -> SUB0, RESPCYCS(0x0F), DATA=0x82

[0077] A2BWRITE -> MAIN, CONTROL(0x12), DATA=0x91

[0078] A2BWRITE -> MAIN, RESPCYCS(0x0F), DATA=0x82

[0079] A2BWRITE -> SUB0, RESPCYCS(0x0F), DATA=0x81

[0080] A2BWRITE -> MAIN, CONTROL(0x12), DATA=0x91

[2c] Tune Subordinate Node 1 — The DISCVRY register is written to the main node using a starting delta of 9. For subordinate node 1, this value is consistently 0x81 – 9 = 0x78. In this example, the cable between subordinate node 0 and 1 is 100 ft, leading to a DSCDONE received on the first attempt.

A SWCTL cycle is performed (ENDDSC, SWCTL.0 = 0, SWCTL.0 = 1), and re-issue of DISCVRY at +1 of the previous value with switch bypass mode disabled, which engages bus power.

[0081] A2BWRITE -> MAIN, INTPND0(0x18), DATA=0xFF

[0082] A2BWRITE -> MAIN, INTPND1(0x19), DATA=0xFF

[0083] A2BWRITE -> MAIN, INTPND2(0x1A), DATA=0xFF

[0084] A2BWRITE -> MAIN, DISCVRY(0x13), DATA=0x78

[0085] A2BREAD <- MAIN, INTSRC(0x16), DATA=0x80

[0086] A2BREAD <- MAIN, INTTYPE(0x17), DATA=0x18

[0087] A2BWRITE -> MAIN, CONTROL(0x12), DATA=0x92

[0088] A2BWRITE -> SUB0, SWCTL(0x09), DATA=0x10

[0089] A2BWRITE -> SUB0, CONTROL(0x12), DATA=0x10

[0090] A2BWRITE -> SUB0, SWCTL(0x09), DATA=0x11

[0091] A2BWRITE -> MAIN, INTPND0(0x18), DATA=0xFF

[0092] A2BWRITE -> MAIN, INTPND1(0x19), DATA=0xFF

[0093] A2BWRITE -> MAIN, INTPND2(0x1A), DATA=0xFF

[0094] A2BWRITE -> MAIN, DISCVRY(0x13), DATA=0x79

[0095] A2BREAD <- MAIN, INTSRC(0x16), DATA=0x80

[0096] A2BREAD <- MAIN, INTTYPE(0x17), DATA=0x18

[2d] Subordinate Node 1 Configuration — Similarly to subordinate node 0, in this step, subordinate node 1 is configured and set up with some default settings and the custom configuration settings are written.

[0097] A2BWRITE -> SUB0, INTMSK0(0x1B), DATA=0x80

[0098] A2BWRITE -> SUB1, RESPCYCS(0x0F), DATA=0x79

[0099] A2BWRITE -> MAIN, CONTROL(0x12), DATA=0x91

[0100] A2BWRITE -> SUB0, INTMSK0(0x1B), DATA=0x80

[0101] A2BWRITE -> MAIN, INTPND2(0x1A), DATA=0x01

[0102] A2BREAD <- SUB1, VENDOR(0x02), DATA=0xAD

[0103] A2BWRITE -> SUB1, RESPCYCS(0x0F), DATA=0x79

[0104] A2BWRITE -> SUB0, SWCTL(0x09), DATA=0x21

[0105] A2BWRITE -> SUB1, MMRPAGE(0xE0), DATA=0x01

[0106] A2BWRITE -> SUB1, CHIP(0x100), DATA=0x02

[0107] A2BWRITE -> SUB1, MMRPAGE(0x1E0), DATA=0x00

[0108] A2BWRITE -> SUB1, MMRPAGE(0xE0), DATA=0x01

[0109] A2BWRITE -> SUB1, MMRPAGE(0x1E0), DATA=0x00

[0110] A2BWRITE -> SUB1, I2SGCFG(0x41), DATA=0x20

[0111] A2BWRITE -> SUB1, MBOX1CTL(0x96), DATA=0x02

[0112] A2BWRITE -> SUB1, INTPND0(0x18), DATA=0xFF

[0113] A2BWRITE -> SUB1, SWCTL(0x09), DATA=0x10

[0114] A2BWRITE_BURST -> SUB1, INTMSK0(0x1B), DATA=[0x00, 0x00]

[0115] A2BREAD <- MAIN, INTSRC(0x16), DATA=0x40

[0116] A2BREAD <- MAIN, INTTYPE(0x17), DATA=0x06

[0117] A2BWRITE -> MAIN, INTPND0(0x18), DATA=0xFF

[0118] A2BWRITE -> MAIN, INTPND1(0x19), DATA=0xFF

[0119] A2BWRITE -> MAIN, INTPND2(0x1A), DATA=0xFF

[0120] A2BWRITE -> SUB0, SWCTL(0x09), DATA=0x11

[0121] A2BWRITE -> MAIN, I2SGCFG(0x41), DATA=0x20

[0122] A2BWRITE_BURST -> MAIN, INTMSK0(0x1B), DATA=[0x50, 0x00, 0x09]

[0123] A2BWRITE -> MAIN, SLOTFMT(0x10), DATA=0x44

[0124] A2BWRITE -> MAIN, INTPND0(0x18), DATA=0xFF

[0125] A2BWRITE -> MAIN, INTPND1(0x19), DATA=0xFF

[0126] A2BWRITE -> MAIN, INTPND2(0x1A), DATA=0xFF

[0127] A2BWRITE -> MAIN, DATCTL(0x11), DATA=0x03

[0128] A2BWRITE -> MAIN, CONTROL(0x12), DATA=0x92

[2e] Subordinate Node 1 Boost — As with subordinate node 0, the boost and health check is at the end of the configuration.

With the subordinate node 1 boost, the final delta is 8 so the boost value is 4.

[0129] A2BWRITE -> MAIN, RESPCYCS(0x0F), DATA=0x86

[0130] A2BWRITE -> SUB0, RESPCYCS(0x0F), DATA=0x85

[0131] A2BWRITE -> SUB1, RESPCYCS(0x0F), DATA=0x7D

[0132] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X91

[0133] A2BREAD <- MAIN, VENDOR(0X02), DATA=0XAD

[0134] A2BREAD <- SUB0, VENDOR(0X02), DATA=0XAD

[0135] A2BREAD <- SUB1, VENDOR(0X02), DATA=0XAD

[3a] Subordinate Node 2 Pre-Discovery — The pre-discovery sequence prepares subordinate node 1 as the upstream node for discovering subordinate node 2. Before the next tuning loop begins, interrupts are cleared, NEWSTRCT is written, subordinate node 1 is placed in switch bypass mode, the B port is enabled, and pending interrupts are cleared on the discovered upstream nodes.

[0136] A2BWRITE_BURST -> MAIN, INTMSK0(0X1B), DATA=[0XFF, 0X00, 0X0F]

[0137] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X91

[0138] A2BWRITE -> SUB1, CONTROL(0X12), DATA=0X18

[0139] A2BREAD <- SUB1, SWSTAT2(0XA5), DATA=0X20

[0140] A2BWRITE -> SUB1, SWCTL(0X09), DATA=0X11

[0141] A2BWRITE_BURST -> SUB1, INTMSK0(0X1B), DATA=[0X80, 0X00]

[0142] A2BREAD <- SUB0, INTMSK0(0X1B), DATA=0X80

[0143] A2BWRITE -> SUB0, INTMSK0(0X1B), DATA=0X00

[0144] A2BWRITE -> SUB0, INTPND0(0X18), DATA=0XFF

[0145] A2BREAD <- SUB1, INTMSK0(0X1B), DATA=0X80

[0146] A2BWRITE -> SUB1, INTMSK0(0X1B), DATA=0X00

[0147] A2BWRITE -> SUB1, INTPND0(0X18), DATA=0XFF

[3b] Auto Calibration Reset — Before attempting discovery of subordinate node 2, the RESPCYCS value or each discover node is incremented and then restored. This forces the auto calibration mechanism to re-center before the next DISCVRY attempt.

[0148] A2BWRITE -> MAIN, RESPCYCS(0X0F), DATA=0X87

[0149] A2BWRITE -> SUB0, RESPCYCS(0X0F), DATA=0X86

[0150] A2BWRITE -> SUB1, RESPCYCS(0X0F), DATA=0X7E

[0151] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X91

[0152] A2BWRITE -> MAIN, RESPCYCS(0X0F), DATA=0X86

[0153] A2BWRITE -> SUB0, RESPCYCS(0X0F), DATA=0X85

[0154] A2BWRITE -> SUB1, RESPCYCS(0X0F), DATA=0X7D

[0155] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X91

[3c] Tune Subordinate Node 2 — The cable between subordinate nodes 1 and 2 is 50 ft. This means it takes a few iterations to find the optimal response cycle value. The algorithm begins with a delta of 9 and does not receive a DSCDONE interrupt. It toggles SWCTL and resets the auto calibration before the next attempt.

[0156] A2BWRITE -> MAIN, INTPND0(0X18), DATA=0XFF

[0157] A2BWRITE -> MAIN, INTPND1(0X19), DATA=0XFF

[0158] A2BWRITE -> MAIN, INTPND2(0X1A), DATA=0XFF

[0159] A2BWRITE -> MAIN, DISCVRY(0X13), DATA=0X74

[0160] A2BREAD <- MAIN, INTSRC(0X16), DATA=0X00

[0161] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X92

[0162] A2BWRITE -> SUB1, SWCTL(0X09), DATA=0X10

[0163] A2BWRITE -> SUB1, CONTROL(0X12), DATA=0X10

[0164] A2BWRITE -> SUB1, CONTROL(0X12), DATA=0X18

[0165] A2BWRITE -> SUB1, SWCTL(0X09), DATA=0X11

[0166] A2BREAD <- SUB0, VENDOR(0X02), DATA=0XAD

[0167] A2BREAD <- SUB1, VENDOR(0X02), DATA=0XAD

[0168] A2BWRITE -> MAIN, RESPCYCS(0X0F), DATA=0X87

[0169] A2BWRITE -> SUB0, RESPCYCS(0X0F), DATA=0X86

[0170] A2BWRITE -> SUB1, RESPCYCS(0X0F), DATA=0X7E

[0171] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X91

[0172] A2BWRITE -> MAIN, RESPCYCS(0X0F), DATA=0X86

[0173] A2BWRITE -> SUB0, RESPCYCS(0X0F), DATA=0X85

[0174] A2BWRITE -> SUB1, RESPCYCS(0X0F), DATA=0X7D

[0175] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X91

[3d] Additional Attempts to Tune Subordinate Node 2 — Like the first attempt, a discovery attempt is made without receiving a DSCDONE interrupt. The upstream B port is toggled, and the auto calibration is reset. The DISCVRY value is incremented and another attempt is made.

This cycle repeats up to 5 times until a DSCDONE interrupt is received.

[0176] A2BWRITE -> MAIN, INTPND0(0X18), DATA=0XFF

[0177] A2BWRITE -> MAIN, INTPND1(0X19), DATA=0XFF

[0178] A2BWRITE -> MAIN, INTPND2(0X1A), DATA=0XFF

[0179] A2BWRITE -> MAIN, DISCVRY(0X13), DATA=0X75

[0180] A2BREAD <- MAIN, INTSRC(0X16), DATA=0X00

[0181] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X92

[0182] A2BWRITE -> SUB1, SWCTL(0X09), DATA=0X10

[0183] A2BWRITE -> SUB1, CONTROL(0X12), DATA=0X10

[0184] A2BWRITE -> SUB1, CONTROL(0X12), DATA=0X18

[0185] A2BWRITE -> SUB1, SWCTL(0X09), DATA=0X11

[0186] A2BREAD <- SUB0, VENDOR(0X02), DATA=0XAD

[0187] A2BREAD <- SUB1, VENDOR(0X02), DATA=0XAD

[0188] A2BWRITE -> MAIN, RESPCYCS(0X0F), DATA=0X87

[0189] A2BWRITE -> SUB0, RESPCYCS(0X0F), DATA=0X86

[0190] A2BWRITE -> SUB1, RESPCYCS(0X0F), DATA=0X7E

[0191] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X91

[0192] A2BWRITE -> MAIN, RESPCYCS(0X0F), DATA=0X86

[0193] A2BWRITE -> SUB0, RESPCYCS(0X0F), DATA=0X85

[0194] A2BWRITE -> SUB1, RESPCYCS(0X0F), DATA=0X7D

[0195] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X91

[0196] A2BWRITE -> MAIN, INTPND0(0X18), DATA=0XFF

[0197] A2BWRITE -> MAIN, INTPND1(0X19), DATA=0XFF

[0198] A2BWRITE -> MAIN, INTPND2(0X1A), DATA=0XFF

[0199] A2BWRITE -> MAIN, DISCVRY(0X13), DATA=0X76

[0200] A2BREAD <- MAIN, INTSRC(0X16), DATA=0X80

[0201] A2BREAD <- MAIN, INTTYPE(0X17), DATA=0X18

[0202] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X92

[3e] Subordinate Node 2 Configuration and Boost — Once a DSCDONE is received, the upstream B port is toggled once more and the node is discovered again, with the upstream B port switch bypass mode is disabled and an increased value of DISCVRY. Before writing ENDDSC, subordinate node 2 is configured and only the required broadcast writes are needed at the main node to establish global settings to the new node. The delta between subordinate nodes 1 and 2 determines the amount of boost applied to all nodes.

[0203] A2BWRITE -> SUB1, SWCTL(0X09), DATA=0X10

[0204] A2BWRITE -> SUB1, CONTROL(0X12), DATA=0X10

[0205] A2BWRITE -> SUB1, SWCTL(0X09), DATA=0X11

[0206] A2BWRITE -> MAIN, INTPND0(0X18), DATA=0XFF

[0207] A2BWRITE -> MAIN, INTPND1(0X19), DATA=0XFF

[0208] A2BWRITE -> MAIN, INTPND2(0X1A), DATA=0XFF

[0209] A2BWRITE -> MAIN, DISCVRY(0X13), DATA=0X77

[0210] A2BREAD <- MAIN, INTSRC(0X16), DATA=0X80

[0211] A2BREAD <- MAIN, INTTYPE(0X17), DATA=0X18

[0212] A2BWRITE -> SUB0, INTMSK0(0X1B), DATA=0X80

[0213] A2BWRITE -> SUB1, INTMSK0(0X1B), DATA=0X80

[0214] A2BWRITE -> SUB2, RESPCYCS(0X0F), DATA=0X77

[0215] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X91

[0216] A2BWRITE -> SUB1, INTMSK0(0X1B), DATA=0X80

[0217] A2BWRITE -> MAIN, INTPND2(0X1A), DATA=0X01

[0218] A2BREAD <- SUB2, VENDOR(0X02), DATA=0XAD

[0219] A2BWRITE -> SUB2, RESPCYCS(0X0F), DATA=0X77

[0220] A2BWRITE -> SUB1, SWCTL(0X09), DATA=0X21

[0221] A2BWRITE -> SUB2, MMRPAGE(0XE0), DATA=0X01

[0222] A2BWRITE -> SUB2, CHIP(0X100), DATA=0X02

[0223] A2BWRITE -> SUB2, MMRPAGE(0X1E0), DATA=0X00

[0224] A2BWRITE -> SUB2, MMRPAGE(0XE0), DATA=0X01

[0225] A2BWRITE -> SUB2, MMRPAGE(0X1E0), DATA=0X00

[0226] A2BWRITE -> SUB2, I2SGCFG(0X41), DATA=0X20

[0227] A2BWRITE -> SUB2, MBOX1CTL(0X96), DATA=0X02

[0228] A2BWRITE -> SUB2, INTPND0(0X18), DATA=0XFF

[0229] A2BWRITE -> SUB2, SWCTL(0X09), DATA=0X10

[0230] A2BWRITE_BURST -> SUB2, INTMSK0(0X1B), DATA=[0X00, 0X00]

[0231] A2BREAD <- MAIN, INTSRC(0X16), DATA=0X41

[0232] A2BREAD <- MAIN, INTTYPE(0X17), DATA=0X06

[0233] A2BWRITE -> MAIN, INTPND0(0X18), DATA=0XFF

[0234] A2BWRITE -> MAIN, INTPND1(0X19), DATA=0XFF

[0235] A2BWRITE -> MAIN, INTPND2(0X1A), DATA=0XFF

[0236] A2BWRITE -> SUB1, SWCTL(0X09), DATA=0X11

[0237] A2BWRITE -> MAIN, I2SGCFG(0X41), DATA=0X20

[0238] A2BWRITE_BURST -> MAIN, INTMSK0(0X1B), DATA=[0X50, 0X00, 0X09]

[0239] A2BWRITE -> MAIN, SLOTFMT(0X10), DATA=0X44

[0240] A2BWRITE -> MAIN, INTPND0(0X18), DATA=0XFF

[0241] A2BWRITE -> MAIN, INTPND1(0X19), DATA=0XFF

[0242] A2BWRITE -> MAIN, INTPND2(0X1A), DATA=0XFF

[0243] A2BWRITE -> MAIN, DATCTL(0X11), DATA=0X03

[0244] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X92

[0245] A2BWRITE -> MAIN, RESPCYCS(0X0F), DATA=0X89

[0246] A2BWRITE -> SUB0, RESPCYCS(0X0F), DATA=0X88

[0247] A2BWRITE -> SUB1, RESPCYCS(0X0F), DATA=0X80

[0248] A2BWRITE -> SUB2, RESPCYCS(0X0F), DATA=0X7A

[0249] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X91

[0250] A2BREAD <- MAIN, VENDOR(0X02), DATA=0XAD

[0251] A2BREAD <- SUB0, VENDOR(0X02), DATA=0XAD

[0252] A2BREAD <- SUB1, VENDOR(0X02), DATA=0XAD

[0253] A2BREAD <- SUB2, VENDOR(0X02), DATA=0XAD

[4a] Subordinate Node 3 Pre-Discovery — The process for subordinate node 3 is the same as for the other nodes. Subordinate node 2 is put into switch bypass mode, interrupts are cleared, and the auto calibration is reset on all nodes by incrementing and decrementing all response cycles in the system.

[0254] A2BWRITE_BURST -> MAIN, INTMSK0(0X1B), DATA=[0XFF, 0X00, 0X0F]

[0255] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X91

[0256] A2BWRITE -> SUB2, CONTROL(0X12), DATA=0X18

[0257] A2BREAD <- SUB2, SWSTAT2(0XA5), DATA=0X20

[0258] A2BWRITE -> SUB2, SWCTL(0X09), DATA=0X11

[0259] A2BWRITE_BURST -> SUB2, INTMSK0(0X1B), DATA=[0X80, 0X00]

[0260] A2BREAD <- SUB0, INTMSK0(0X1B), DATA=0X80

[0261] A2BWRITE -> SUB0, INTMSK0(0X1B), DATA=0X00

[0262] A2BWRITE -> SUB0, INTPND0(0X18), DATA=0XFF

[0263] A2BREAD <- SUB1, INTMSK0(0X1B), DATA=0X80

[0264] A2BWRITE -> SUB1, INTMSK0(0X1B), DATA=0X00

[0265] A2BWRITE -> SUB1, INTPND0(0X18), DATA=0XFF

[0266] A2BREAD <- SUB2, INTMSK0(0X1B), DATA=0X80

[0267] A2BWRITE -> SUB2, INTMSK0(0X1B), DATA=0X00

[0268] A2BWRITE -> SUB2, INTPND0(0X18), DATA=0XFF

[0269] A2BWRITE -> MAIN, RESPCYCS(0X0F), DATA=0X8A

[0270] A2BWRITE -> SUB0, RESPCYCS(0X0F), DATA=0X89

[0271] A2BWRITE -> SUB1, RESPCYCS(0X0F), DATA=0X81

[0272] A2BWRITE -> SUB2, RESPCYCS(0X0F), DATA=0X7B

[0273] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X91

[0274] A2BWRITE -> MAIN, RESPCYCS(0X0F), DATA=0X89

[0275] A2BWRITE -> SUB0, RESPCYCS(0X0F), DATA=0X88

[0276] A2BWRITE -> SUB1, RESPCYCS(0X0F), DATA=0X80

[0277] A2BWRITE -> SUB2, RESPCYCS(0X0F), DATA=0X7A

[0278] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X91

[4b] Subordinate Node 3 Tuning — The cable between subordinate nodes 2 and 3 is 20 ft, requiring more tuning attempts than previous nodes, however the process remains the same. The DISCVRY register is written and if no DSCDONE interrupt is received, the process of resetting the auto calibration and retrying discovery with an incremented value is repeated.

[0279] A2BWRITE -> MAIN, INTPND0(0X18), DATA=0XFF

[0280] A2BWRITE -> MAIN, INTPND1(0X19), DATA=0XFF

[0281] A2BWRITE -> MAIN, INTPND2(0X1A), DATA=0XFF

[0282] A2BWRITE -> MAIN, DISCVRY(0X13), DATA=0X71

[0283] A2BREAD <- MAIN, INTSRC(0X16), DATA=0X00

[0284] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X92

[0285] A2BWRITE -> SUB2, SWCTL(0X09), DATA=0X10

[0286] A2BWRITE -> SUB2, CONTROL(0X12), DATA=0X10

[0287] A2BWRITE -> SUB2, CONTROL(0X12), DATA=0X18

[0288] A2BWRITE -> SUB2, SWCTL(0X09), DATA=0X11

[0289] A2BREAD <- SUB0, VENDOR(0X02), DATA=0XAD

[0290] A2BREAD <- SUB1, VENDOR(0X02), DATA=0XAD

[0291] A2BREAD <- SUB2, VENDOR(0X02), DATA=0XAD

[0292] A2BWRITE -> MAIN, RESPCYCS(0X0F), DATA=0X8A

[0293] A2BWRITE -> SUB0, RESPCYCS(0X0F), DATA=0X89

[0294] A2BWRITE -> SUB1, RESPCYCS(0X0F), DATA=0X81

[0295] A2BWRITE -> SUB2, RESPCYCS(0X0F), DATA=0X7B

[0296] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X91

[0297] A2BWRITE -> MAIN, RESPCYCS(0X0F), DATA=0X89

[0298] A2BWRITE -> SUB0, RESPCYCS(0X0F), DATA=0X88

[0299] A2BWRITE -> SUB1, RESPCYCS(0X0F), DATA=0X80

[0300] A2BWRITE -> SUB2, RESPCYCS(0X0F), DATA=0X7A

[0301] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X91

[4c] Additional Attempts to Tune Subordinate Node 3 — A total of four attempts are made, aligning with the expected behavior.

[0302] A2BWRITE -> MAIN, INTPND0(0X18), DATA=0XFF

[0303] A2BWRITE -> MAIN, INTPND1(0X19), DATA=0XFF

[0304] A2BWRITE -> MAIN, INTPND2(0X1A), DATA=0XFF

[0305] A2BWRITE -> MAIN, DISCVRY(0X13), DATA=0X72

[0306] A2BREAD <- MAIN, INTSRC(0X16), DATA=0X00

[0307] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X92

[0308] A2BWRITE -> SUB2, SWCTL(0X09), DATA=0X10

[0309] A2BWRITE -> SUB2, CONTROL(0X12), DATA=0X10

[0310] A2BWRITE -> SUB2, CONTROL(0X12), DATA=0X18

[0311] A2BWRITE -> SUB2, SWCTL(0X09), DATA=0X11

[0312] A2BREAD <- SUB0, VENDOR(0X02), DATA=0XAD

[0313] A2BREAD <- SUB1, VENDOR(0X02), DATA=0XAD

[0314] A2BREAD <- SUB2, VENDOR(0X02), DATA=0XAD

[0315] A2BWRITE -> MAIN, RESPCYCS(0X0F), DATA=0X8A

[0316] A2BWRITE -> SUB0, RESPCYCS(0X0F), DATA=0X89

[0317] A2BWRITE -> SUB1, RESPCYCS(0X0F), DATA=0X81

[0318] A2BWRITE -> SUB2, RESPCYCS(0X0F), DATA=0X7B

[0319] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X91

[0320] A2BWRITE -> MAIN, RESPCYCS(0X0F), DATA=0X89

[0321] A2BWRITE -> SUB0, RESPCYCS(0X0F), DATA=0X88

[0322] A2BWRITE -> SUB1, RESPCYCS(0X0F), DATA=0X80

[0323] A2BWRITE -> SUB2, RESPCYCS(0X0F), DATA=0X7A

[0324] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X91

[0325] A2BWRITE -> MAIN, INTPND0(0X18), DATA=0XFF

[0326] A2BWRITE -> MAIN, INTPND1(0X19), DATA=0XFF

[0327] A2BWRITE -> MAIN, INTPND2(0X1A), DATA=0XFF

[0328] A2BWRITE -> MAIN, DISCVRY(0X13), DATA=0X73

[0329] A2BREAD <- MAIN, INTSRC(0X16), DATA=0X00

[0330] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X92

[0331] A2BWRITE -> SUB2, SWCTL(0X09), DATA=0X10

[0332] A2BWRITE -> SUB2, CONTROL(0X12), DATA=0X10

[0333] A2BWRITE -> SUB2, CONTROL(0X12), DATA=0X18

[0334] A2BWRITE -> SUB2, SWCTL(0X09), DATA=0X11

[0335] A2BREAD <- SUB0, VENDOR(0X02), DATA=0XAD

[0336] A2BREAD <- SUB1, VENDOR(0X02), DATA=0XAD

[0337] A2BREAD <- SUB2, VENDOR(0X02), DATA=0XAD

[0338] A2BWRITE -> MAIN, RESPCYCS(0X0F), DATA=0X8A

[0339] A2BWRITE -> SUB0, RESPCYCS(0X0F), DATA=0X89

[0340] A2BWRITE -> SUB1, RESPCYCS(0X0F), DATA=0X81

[0341] A2BWRITE -> SUB2, RESPCYCS(0X0F), DATA=0X7B

[0342] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X91

[0343] A2BWRITE -> MAIN, RESPCYCS(0X0F), DATA=0X89

[0344] A2BWRITE -> SUB0, RESPCYCS(0X0F), DATA=0X88

[0345] A2BWRITE -> SUB1, RESPCYCS(0X0F), DATA=0X80

[0346] A2BWRITE -> SUB2, RESPCYCS(0X0F), DATA=0X7A

[0347] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X91

[0348] A2BWRITE -> MAIN, INTPND0(0X18), DATA=0XFF

[0349] A2BWRITE -> MAIN, INTPND1(0X19), DATA=0XFF

[0350] A2BWRITE -> MAIN, INTPND2(0X1A), DATA=0XFF

[0351] A2BWRITE -> MAIN, DISCVRY(0X13), DATA=0X74

[0352] A2BREAD <- MAIN, INTSRC(0X16), DATA=0X80

[0353] A2BREAD <- MAIN, INTTYPE(0X17), DATA=0X18

[0354] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X92

[4d] Subordinate Node 3 Configuration — After the DSCDONE interrupt is received, the node is rediscovered with bus power enabled. The value for DISCVRY is one higher than the value that was used for the first DSCDONE.

[0355] A2BWRITE -> SUB2, SWCTL(0X09), DATA=0X10

[0356] A2BWRITE -> SUB2, CONTROL(0X12), DATA=0X10

[0357] A2BWRITE -> SUB2, SWCTL(0X09), DATA=0X11

[0358] A2BWRITE -> MAIN, INTPND0(0X18), DATA=0XFF

[0359] A2BWRITE -> MAIN, INTPND1(0X19), DATA=0XFF

[0360] A2BWRITE -> MAIN, INTPND2(0X1A), DATA=0XFF

[0361] A2BWRITE -> MAIN, DISCVRY(0X13), DATA=0X75

[0362] A2BREAD <- MAIN, INTSRC(0X16), DATA=0X80

[0363] A2BREAD <- MAIN, INTTYPE(0X17), DATA=0X18

[0364] A2BWRITE -> SUB0, INTMSK0(0X1B), DATA=0X80

[0365] A2BWRITE -> SUB1, INTMSK0(0X1B), DATA=0X80

[0366] A2BWRITE -> SUB2, INTMSK0(0X1B), DATA=0X80

[0367] A2BWRITE -> SUB3, RESPCYCS(0X0F), DATA=0X75

[0368] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X91

[0369] A2BWRITE -> SUB2, INTMSK0(0X1B), DATA=0X80

[0370] A2BWRITE -> MAIN, INTPND2(0X1A), DATA=0X01

[0371] A2BREAD <- SUB3, VENDOR(0X02), DATA=0XAD

[0372] A2BWRITE -> SUB3, RESPCYCS(0X0F), DATA=0X75

[0373] A2BWRITE -> SUB2, SWCTL(0X09), DATA=0X21

[0374] A2BWRITE -> SUB3, MMRPAGE(0XE0), DATA=0X01

[0375] A2BWRITE -> SUB3, CHIP(0X100), DATA=0X02

[0376] A2BWRITE -> SUB3, MMRPAGE(0X1E0), DATA=0X00

[0377] A2BWRITE -> SUB3, MMRPAGE(0XE0), DATA=0X01

[0378] A2BWRITE -> SUB3, MMRPAGE(0X1E0), DATA=0X00

[0379] A2BWRITE -> SUB3, I2SGCFG(0X41), DATA=0X20

[0380] A2BWRITE -> SUB3, MBOX1CTL(0X96), DATA=0X02

[0381] A2BWRITE -> SUB3, INTPND0(0X18), DATA=0XFF

[0382] A2BWRITE -> SUB3, SWCTL(0X09), DATA=0X10

[0383] A2BWRITE_BURST -> SUB3, INTMSK0(0X1B), DATA=[0X00, 0X00]

[0384] A2BREAD <- MAIN, INTSRC(0X16), DATA=0X42

[0385] A2BREAD <- MAIN, INTTYPE(0X17), DATA=0X06

[0386] A2BWRITE -> MAIN, INTPND0(0X18), DATA=0XFF

[0387] A2BWRITE -> MAIN, INTPND1(0X19), DATA=0XFF

[0388] A2BWRITE -> MAIN, INTPND2(0X1A), DATA=0XFF

[0389] A2BWRITE -> SUB2, SWCTL(0X09), DATA=0X11

[0390] A2BWRITE -> MAIN, I2SGCFG(0X41), DATA=0X20

[0391] A2BWRITE_BURST -> MAIN, INTMSK0(0X1B), DATA=[0X50, 0X00, 0X09]

[0392] A2BWRITE -> MAIN, SLOTFMT(0X10), DATA=0X44

[0393] A2BWRITE -> MAIN, INTPND0(0X18), DATA=0XFF

[0394] A2BWRITE -> MAIN, INTPND1(0X19), DATA=0XFF

[0395] A2BWRITE -> MAIN, INTPND2(0X1A), DATA=0XFF

[0396] A2BWRITE -> MAIN, DATCTL(0X11), DATA=0X03

[0397] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X92

[4e] Subordinate Node 3 Boost — The delta between subordinate nodes 2 and 3 is 0x7A – 0x75 = 5. Since 5/2 = 2.5 and is not an integer value, the boost value is rounded down to 2. Rounding down is the conservative choice to keep the margin from drifting from the optimized value.

[0398] A2BWRITE -> MAIN, RESPCYCS(0X0F), DATA=0X8B

[0399] A2BWRITE -> SUB0, RESPCYCS(0X0F), DATA=0X8A

[0400] A2BWRITE -> SUB1, RESPCYCS(0X0F), DATA=0X82

[0401] A2BWRITE -> SUB2, RESPCYCS(0X0F), DATA=0X7C

[0402] A2BWRITE -> SUB3, RESPCYCS(0X0F), DATA=0X77

[0403] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X91

[0404] A2BREAD <- MAIN, VENDOR(0X02), DATA=0XAD

[0405] A2BREAD <- SUB0, VENDOR(0X02), DATA=0XAD

[0406] A2BREAD <- SUB1, VENDOR(0X02), DATA=0XAD

[0407] A2BREAD <- SUB2, VENDOR(0X02), DATA=0XAD

[0408] A2BREAD <- SUB3, VENDOR(0X02), DATA=0XAD

[5a] Subordinate 4 Pre-Discovery — This phase demonstrates the algorithm behavior when no additional subordinate node is connected after subordinate node 3. The pre-discovery phase is the same as previous stages: Subordinate node 3 is placed into switch bypass mode, upstream node auto calibrations are reset, and interrupts are cleared.

[0409] A2BWRITE_BURST -> MAIN, INTMSK0(0X1B), DATA=[0XFF, 0X00, 0X0F]

[0410] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X91

[0411] A2BWRITE -> SUB3, CONTROL(0X12), DATA=0X18

[0412] A2BREAD <- SUB3, SWSTAT2(0XA5), DATA=0X20

[0413] A2BWRITE -> SUB3, SWCTL(0X09), DATA=0X11

[0414] A2BWRITE_BURST -> SUB3, INTMSK0(0X1B), DATA=[0X80, 0X00]

[0415] A2BREAD <- SUB0, INTMSK0(0X1B), DATA=0X80

[0416] A2BWRITE -> SUB0, INTMSK0(0X1B), DATA=0X00

[0417] A2BWRITE -> SUB0, INTPND0(0X18), DATA=0XFF

[0418] A2BREAD <- SUB1, INTMSK0(0X1B), DATA=0X80

[0419] A2BWRITE -> SUB1, INTMSK0(0X1B), DATA=0X00

[0420] A2BWRITE -> SUB1, INTPND0(0X18), DATA=0XFF

[0421] A2BREAD <- SUB2, INTMSK0(0X1B), DATA=0X80

[0422] A2BWRITE -> SUB2, INTMSK0(0X1B), DATA=0X00

[0423] A2BWRITE -> SUB2, INTPND0(0X18), DATA=0XFF

[0424] A2BREAD <- SUB3, INTMSK0(0X1B), DATA=0X80

[0425] A2BWRITE -> SUB3, INTMSK0(0X1B), DATA=0X00

[0426] A2BWRITE -> SUB3, INTPND0(0X18), DATA=0XFF

[0427] A2BWRITE -> MAIN, RESPCYCS(0X0F), DATA=0X8C

[0428] A2BWRITE -> SUB0, RESPCYCS(0X0F), DATA=0X8B

[0429] A2BWRITE -> SUB1, RESPCYCS(0X0F), DATA=0X83

[0430] A2BWRITE -> SUB2, RESPCYCS(0X0F), DATA=0X7D

[0431] A2BWRITE -> SUB3, RESPCYCS(0X0F), DATA=0X78

[0432] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X91

[0433] A2BWRITE -> MAIN, RESPCYCS(0X0F), DATA=0X8B

[0434] A2BWRITE -> SUB0, RESPCYCS(0X0F), DATA=0X8A

[0435] A2BWRITE -> SUB1, RESPCYCS(0X0F), DATA=0X82

[0436] A2BWRITE -> SUB2, RESPCYCS(0X0F), DATA=0X7C

[0437] A2BWRITE -> SUB3, RESPCYCS(0X0F), DATA=0X77

[0438] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X91

[0439] A2BWRITE -> MAIN, INTPND0(0X18), DATA=0XFF

[0440] A2BWRITE -> MAIN, INTPND1(0X19), DATA=0XFF

[0441] A2BWRITE -> MAIN, INTPND2(0X1A), DATA=0XFF

[5b] Subordinate Node n Tuning – Use the same process as in the other steps to find the next node. DISCVRY is written and the interrupts are checked for a DSCDONE. After each attempt, the auto calibrations are reset. Six attempts are made.

This covers the range of supported cables up to 100ft.

[0442] A2BWRITE -> MAIN, DISCVRY(0X13), DATA=0X6E

[0443] A2BREAD <- MAIN, INTSRC(0X16), DATA=0X00

[0444] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X92

[0445] A2BWRITE -> SUB3, SWCTL(0X09), DATA=0X10

[0446] A2BWRITE -> SUB3, CONTROL(0X12), DATA=0X10

[0447] A2BWRITE -> SUB3, CONTROL(0X12), DATA=0X18

[0448] A2BWRITE -> SUB3, SWCTL(0X09), DATA=0X11

[0449] A2BREAD <- SUB0, VENDOR(0X02), DATA=0XAD

[0450] A2BREAD <- SUB1, VENDOR(0X02), DATA=0XAD

[0451] A2BREAD <- SUB2, VENDOR(0X02), DATA=0XAD

[0452] A2BREAD <- SUB3, VENDOR(0X02), DATA=0XAD

[0453] A2BWRITE -> MAIN, RESPCYCS(0X0F), DATA=0X8C

[0454] A2BWRITE -> SUB0, RESPCYCS(0X0F), DATA=0X8B
[0455] A2BWRITE -> SUB1, RESPCYCS(0X0F), DATA=0X83
[0456] A2BWRITE -> SUB2, RESPCYCS(0X0F), DATA=0X7D
[0457] A2BWRITE -> SUB3, RESPCYCS(0X0F), DATA=0X78
[0458] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X91
[0459] A2BWRITE -> MAIN, RESPCYCS(0X0F), DATA=0X8B
[0460] A2BWRITE -> SUB0, RESPCYCS(0X0F), DATA=0X8A
[0461] A2BWRITE -> SUB1, RESPCYCS(0X0F), DATA=0X82
[0462] A2BWRITE -> SUB2, RESPCYCS(0X0F), DATA=0X7C
[0463] A2BWRITE -> SUB3, RESPCYCS(0X0F), DATA=0X77
[0464] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X91
[0465] A2BWRITE -> MAIN, INTPND0(0X18), DATA=0XFF
[0466] A2BWRITE -> MAIN, INTPND1(0X19), DATA=0XFF
[0467] A2BWRITE -> MAIN, INTPND2(0X1A), DATA=0XFF
[0468] A2BWRITE -> MAIN, DISCVRY(0X13), DATA=0X6F
[0469] A2BREAD <- MAIN, INTSRC(0X16), DATA=0X00
[0470] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X92
[0471] A2BWRITE -> SUB3, SWCTL(0X09), DATA=0X10
[0472] A2BWRITE -> SUB3, CONTROL(0X12), DATA=0X10
[0473] A2BWRITE -> SUB3, CONTROL(0X12), DATA=0X18
[0474] A2BWRITE -> SUB3, SWCTL(0X09), DATA=0X11
[0475] A2BREAD <- SUB0, VENDOR(0X02), DATA=0XAD
[0476] A2BREAD <- SUB1, VENDOR(0X02), DATA=0XAD
[0477] A2BREAD <- SUB2, VENDOR(0X02), DATA=0XAD
[0478] A2BREAD <- SUB3, VENDOR(0X02), DATA=0XAD
[0479] A2BWRITE -> MAIN, RESPCYCS(0X0F), DATA=0X8C
[0480] A2BWRITE -> SUB0, RESPCYCS(0X0F), DATA=0X8B
[0481] A2BWRITE -> SUB1, RESPCYCS(0X0F), DATA=0X83
[0482] A2BWRITE -> SUB2, RESPCYCS(0X0F), DATA=0X7D
[0483] A2BWRITE -> SUB3, RESPCYCS(0X0F), DATA=0X78
[0484] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X91
[0485] A2BWRITE -> MAIN, RESPCYCS(0X0F), DATA=0X8B
[0486] A2BWRITE -> SUB0, RESPCYCS(0X0F), DATA=0X8A
[0487] A2BWRITE -> SUB1, RESPCYCS(0X0F), DATA=0X82
[0488] A2BWRITE -> SUB2, RESPCYCS(0X0F), DATA=0X7C
[0489] A2BWRITE -> SUB3, RESPCYCS(0X0F), DATA=0X77
[0490] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X91
[0491] A2BWRITE -> MAIN, INTPND0(0X18), DATA=0XFF
[0492] A2BWRITE -> MAIN, INTPND1(0X19), DATA=0XFF
[0493] A2BWRITE -> MAIN, INTPND2(0X1A), DATA=0XFF
[0494] A2BWRITE -> MAIN, DISCVRY(0X13), DATA=0X70
[0495] A2BREAD <- MAIN, INTSRC(0X16), DATA=0X00
[0496] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X92
[0497] A2BWRITE -> SUB3, SWCTL(0X09), DATA=0X10
[0498] A2BWRITE -> SUB3, CONTROL(0X12), DATA=0X10
[0499] A2BWRITE -> SUB3, CONTROL(0X12), DATA=0X18
[0500] A2BWRITE -> SUB3, SWCTL(0X09), DATA=0X11
[0501] A2BREAD <- SUB0, VENDOR(0X02), DATA=0XAD
[0502] A2BREAD <- SUB1, VENDOR(0X02), DATA=0XAD
[0503] A2BREAD <- SUB2, VENDOR(0X02), DATA=0XAD
[0504] A2BREAD <- SUB3, VENDOR(0X02), DATA=0XAD
[0505] A2BWRITE -> MAIN, RESPCYCS(0X0F), DATA=0X8C
[0506] A2BWRITE -> SUB0, RESPCYCS(0X0F), DATA=0X8B
[0507] A2BWRITE -> SUB1, RESPCYCS(0X0F), DATA=0X83
[0508] A2BWRITE -> SUB2, RESPCYCS(0X0F), DATA=0X7D
[0509] A2BWRITE -> SUB3, RESPCYCS(0X0F), DATA=0X78
[0510] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X91
[0511] A2BWRITE -> MAIN, RESPCYCS(0X0F), DATA=0X8B
[0512] A2BWRITE -> SUB0, RESPCYCS(0X0F), DATA=0X8A
[0513] A2BWRITE -> SUB1, RESPCYCS(0X0F), DATA=0X82
[0514] A2BWRITE -> SUB2, RESPCYCS(0X0F), DATA=0X7C
[0515] A2BWRITE -> SUB3, RESPCYCS(0X0F), DATA=0X77
[0516] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X91
[0517] A2BWRITE -> MAIN, INTPND0(0X18), DATA=0XFF
[0518] A2BWRITE -> MAIN, INTPND1(0X19), DATA=0XFF
[0519] A2BWRITE -> MAIN, INTPND2(0X1A), DATA=0XFF
[0520] A2BWRITE -> MAIN, DISCVRY(0X13), DATA=0X71
[0521] A2BREAD <- MAIN, INTSRC(0X16), DATA=0X00
[0522] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X92
[0523] A2BWRITE -> SUB3, SWCTL(0X09), DATA=0X10
[0524] A2BWRITE -> SUB3, CONTROL(0X12), DATA=0X10
[0525] A2BWRITE -> SUB3, CONTROL(0X12), DATA=0X18
[0526] A2BWRITE -> SUB3, SWCTL(0X09), DATA=0X11
[0527] A2BREAD <- SUB0, VENDOR(0X02), DATA=0XAD
[0528] A2BREAD <- SUB1, VENDOR(0X02), DATA=0XAD
[0529] A2BREAD <- SUB2, VENDOR(0X02), DATA=0XAD
[0530] A2BREAD <- SUB3, VENDOR(0X02), DATA=0XAD
[0531] A2BWRITE -> MAIN, RESPCYCS(0X0F), DATA=0X8C
[0532] A2BWRITE -> SUB0, RESPCYCS(0X0F), DATA=0X8B
[0533] A2BWRITE -> SUB1, RESPCYCS(0X0F), DATA=0X83
[0534] A2BWRITE -> SUB2, RESPCYCS(0X0F), DATA=0X7D
[0535] A2BWRITE -> SUB3, RESPCYCS(0X0F), DATA=0X78
[0536] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X91
[0537] A2BWRITE -> MAIN, RESPCYCS(0X0F), DATA=0X8B
[0538] A2BWRITE -> SUB0, RESPCYCS(0X0F), DATA=0X8A
[0539] A2BWRITE -> SUB1, RESPCYCS(0X0F), DATA=0X82

[0540] A2BWRITE -> SUB2, RESPCYCS(0X0F), DATA=0X7C

[0541] A2BWRITE -> SUB3, RESPCYCS(0X0F), DATA=0X77

[0542] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X91

[0543] A2BWRITE -> MAIN, INTPND0(0X18), DATA=0XFF

[0544] A2BWRITE -> MAIN, INTPND1(0X19), DATA=0XFF

[0545] A2BWRITE -> MAIN, INTPND2(0X1A), DATA=0XFF

[0546] A2BWRITE -> MAIN, DISCVRY(0X13), DATA=0X72

[0547] A2BREAD <- MAIN, INTSRC(0X16), DATA=0X00

[0548] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X92

[0549] A2BWRITE -> SUB3, SWCTL(0X09), DATA=0X10

[0550] A2BWRITE -> SUB3, CONTROL(0X12), DATA=0X10

[0551] A2BWRITE -> SUB3, CONTROL(0X12), DATA=0X18

[0552] A2BWRITE -> SUB3, SWCTL(0X09), DATA=0X11

[0553] A2BREAD <- SUB0, VENDOR(0X02), DATA=0XAD

[0554] A2BREAD <- SUB1, VENDOR(0X02), DATA=0XAD

[0555] A2BREAD <- SUB2, VENDOR(0X02), DATA=0XAD

[0556] A2BREAD <- SUB3, VENDOR(0X02), DATA=0XAD

[0557] A2BWRITE -> MAIN, RESPCYCS(0X0F), DATA=0X8C

[0558] A2BWRITE -> SUB0, RESPCYCS(0X0F), DATA=0X8B

[0559] A2BWRITE -> SUB1, RESPCYCS(0X0F), DATA=0X83

[0560] A2BWRITE -> SUB2, RESPCYCS(0X0F), DATA=0X7D

[0561] A2BWRITE -> SUB3, RESPCYCS(0X0F), DATA=0X78

[0562] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X91

[0563] A2BWRITE -> MAIN, RESPCYCS(0X0F), DATA=0X8B

[0564] A2BWRITE -> SUB0, RESPCYCS(0X0F), DATA=0X8A

[0565] A2BWRITE -> SUB1, RESPCYCS(0X0F), DATA=0X82

[0566] A2BWRITE -> SUB2, RESPCYCS(0X0F), DATA=0X7C

[0567] A2BWRITE -> SUB3, RESPCYCS(0X0F), DATA=0X77

[0568] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X91

[0569] A2BWRITE -> MAIN, INTPND0(0X18), DATA=0XFF

[0570] A2BWRITE -> MAIN, INTPND1(0X19), DATA=0XFF

[0571] A2BWRITE -> MAIN, INTPND2(0X1A), DATA=0XFF

[0572] A2BWRITE -> MAIN, DISCVRY(0X13), DATA=0X73

[0573] A2BREAD <- MAIN, INTSRC(0X16), DATA=0X00

[0574] A2BWRITE -> MAIN, CONTROL(0X12), DATA=0X92

[5c] Discovery Wrap Up — After six attempts, ENDDSC is written completing the discovery process. The subordinate node 3 B port is turned off, and a final health check and interrupt clear is completed.

[0575] A2BWRITE -> SUB3, SWCTL(0X09), DATA=0X10

[0576] A2BWRITE -> SUB3, CONTROL(0X12), DATA=0X10

[0577] A2BWRITE -> SUB3, CONTROL(0X12), DATA=0X18

[0578] A2BREAD <- SUB0, VENDOR(0X02), DATA=0XAD

[0579] A2BREAD <- SUB1, VENDOR(0X02), DATA=0XAD

[0580] A2BREAD <- SUB2, VENDOR(0X02), DATA=0XAD

[0581] A2BREAD <- SUB3, VENDOR(0X02), DATA=0XAD

[0582] A2BWRITE -> SUB0, INTMSK0(0X1B), DATA=0X00

[0583] A2BWRITE -> SUB1, INTMSK0(0X1B), DATA=0X00

[0584] A2BWRITE -> SUB2, INTMSK0(0X1B), DATA=0X00

[0585] A2BWRITE -> SUB3, INTMSK0(0X1B), DATA=0X00

[0586] A2BWRITE -> SUB3, SWCTL(0X09), DATA=0X10

[0587] A2BWRITE -> SUB3, INTPND0(0X18), DATA=0XFF

Key Observations

The delta scales with cable length after subordinate node 0 discovery are as follows: 0x08 for the 100 ft segment, 0x06 for 50 ft, and 0x05 for the 20 ft trailing segment.

The response cycle relationship of subordinate node 0 to the main node is unique and is not cable-length dependent in the same way as downstream links, so it is addressed separately.

Boost follows proportionally, so longer cables receive more margin (+4), and shorter cables less margin (+2 or +3). The algorithm requires no cable length input; delta and boost are derived entirely from the sweep result at each stage.

By the final stage, the main node the RESPCYCS value grows from 0x80 to 0x8B. This is an increase of 0x0B, reflecting the accumulated frame overhead of a fully operational five-node chain across 190 ft of total cable.

Verification of this procedure was done by testing a system of eight subordinate nodes and the following five cable lengths: 10 ft, 20 ft, 50 ft, 75 ft, and 100 ft. A limited number of cable combinations were tested to evaluate system stresses under different test conditions.

Table 1 shows the conditions for successful tests.

Test Name	Test Number	Subordinate Node Cable Length (ft)							
		Node 0	Node 1	Node 2	Node 3	Node 4	Node 5	Node 6	Node 7
Pure Boundaries	1	10	10	10	10	10	10	10	10
	2	100	100	100	100	100	100	100	100
	3	50	50	50	50	50	50	50	50
Single Segment Perturbation	4	100	10	10	10	10	10	10	10
	5	10	100	10	10	10	10	10	10
	6	10	10	100	10	10	10	10	10
	7	10	10	10	100	10	10	10	10
	8	10	10	10	10	100	10	10	10
	9	10	10	10	10	10	100	10	10
	10	10	10	10	10	10	10	100	10
	11	10	10	10	10	10	10	10	100
Gradient Chain	12	10	20	50	75	100	100	100	100
	13	100	100	100	75	50	20	10	10
	14	10	50	20	75	10	100	20	75
Alternating Stress	15	10	100	10	100	10	100	10	100
	16	10	10	100	10	100	10	100	10
	17	20	75	10	100	50	20	75	10
Front/Back Loaded Asymmetry	18	100	100	100	100	10	10	10	10
	19	10	10	10	10	100	100	100	100
	20	100	75	50	20	10	10	10	10
	21	10	10	10	10	20	50	75	100
Mixed Topology	22	20	100	20	50	75	10	100	50
	23	75	20	100	10	75	50	20	100

Test Name	Test Number	Subordinate Node Cable Length (ft)							
		Node 0	Node 1	Node 2	Node 3	Node 4	Node 5	Node 6	Node 7
	24	50	10	75	100	20	75	10	50
Randomized Coverage	25	20	10	50	100	75	20	100	10
	26	100	20	75	50	10	100	50	75
	27	10	75	20	100	50	75	20	10

Table 1. Successful Test Cases

The following methods were attempted but did not successfully discover all nodes:

1. A test case with a delta associated with a short cable length, for faster communication, potentially failed because of asymmetry of the auto calibration
2. Not boosting the upstream nodes failed because the additional transceiver delay was not being compensated for
3. Replying purely on the auto calibration with set deltas worked for certain cable combinations with under four nodes, it did not work for more than four nodes at various cable combinations outside the set delta
4. Tested without resetting the auto calibration resulted in several upstream node drops

For successful discovery with unknown cable lengths, the following methods are necessary:

1. Start with a high delta, associated with the longest supported cable length, and increment upward toward the shortest cable length
2. Reset the auto calibration by incrementing and decrementing all response cycles before attempting a new discovery
3. Boost upstream values by one half of the delta to compensate for the additional cable delay of the newly added node and cable to the upstream nodes

Source Code

The included zip file contains the example python code used to demonstrate this application. The code is not a complete discovery stack and does not include audio stream configuration. Configuring audio streams requires changes to response cycle settings, is based on traffic and will modify the base settings found using the methods described in this document.

References

[1] *AD2437 Automotive Audio Bus (A²B®) Transceiver Technical Reference Manual.* Rev 0.2. July 2023. Analog Devices, Inc.

[2] *AD2437 Automotive Audio Bus (A²B®) System Specification Manual.* Rev 1.0. October 2025. Analog Devices, Inc.

Document History

Revision	Description
Revision 1 – August 2026	Original Document