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# Boot Estimation for ADSP-SC835 Processors

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## Introduction

For automotive infotainment applications, a fast boot time improves *time to audio.* This EE-note provides accurate estimation of the boot time for the ADSP-SC835 SHARC-FX® processors. This information is useful for designing an application and defining the boot strategy to adopt to reduce the overall boot-up time.

The boot time in ADSP-SC835/SC839 SHARC-FX processors depends on many factors including: boot mode used, size of the loader stream, and types of blocks present within the loader stream. This EE-Note explains the impact of these factors and provides an estimate of boot time. A boot time comparison between previous products (ADSP-SC57x, ADSP-2156x, ADSP-2159x/ADSP-SC59x, ADSP-SC598) and the ADSP-SC83x families is also given to assist engineers in selecting the appropriate processor for their application boot time needs.

### Summary

Boot time estimation helps a user to construct an optimized loader stream that gives a faster boot time. This note provides calculated linear equations for boot time estimation in different boot modes (varying with boot image size). It also discusses how distinct factors affect total boot time and explains how to incorporate these factors for a more accurate estimation of boot time.

Use this note to design a multi-stage boot strategy. For example, to boot an application having a 2 MB loader stream in less than 75 ms time using the SPI Quad STR boot mode, the user can only achieve 37.5 MHz SPI clock (with 600 MHz CCLK and 300 MHz SYSCLK) at power up. The 75 ms requirement cannot be met (as shown by the calculated equation in Figure 1*: SPI Flash Normal Boot at 62.5 MHz*). In this situation, updating the CGU and boot command for 75 MHz SPI clock value solves the problem. The user has the following options:

- **Normal Boot with OTP**–Initialize the CGU and DMC and program the boot command through the OTP.
- **Normal Boot without OTP**–Initialize CGU and DMC and program the boot command using `Initcode` or a primary application using a multi-stage boot.
- **Secure Boot**–Program the CGU, DMC initialization, security keys and boot command using the OTP or a primary application using a multi-stage boot.

For situations where a multi-stage boot strategy must be adapted, one can minimize the size for the primary application using this guide to meet the total boot time requirement. Boot time estimation can be useful for a user to decide a complex multi-phase boot strategy; where they can choose the size of each boot stage to help meet their requirements and reduce the overall boot time.

### This EE-Note Describes


- Boot Time for ADSP-SC835 SHARC-FX Processors
- Boot Time Estimation
- Boot Time Nonlinearity
- Boot Benchmarking
- Factors Affecting Total Boot Time
- Secure Boot Time Enhancement
- Comparison of Boot Time Among Different Processors


### Terminology

- ECDSA–Elliptical Curve Digital Signature Algorithm
- BLp–Boot Loader plaintext, Plaintext Format
- BLx–Boot Loader without key, Keyless Format
- BLw–Boot Loader wrapped, Wrapped Format
- STR–Single transfer rate
- DTR–Dual transfer rate
- GPIO–General-purpose input/output

## Boot Time for ADSP-SC835 SHARC-FX Processors

Total boot time for ADSP-SC835/SC839 SHARC-FX processors includes the sum of processor pre-boot time and the boot time consumed loading the application (for a defined boot mode).

- Pre-boot time configures all system resources prior to executing the required boot operation.
- Application loading time depends on the nature of loader stream and the peripheral used for a particular boot mode.

Several factors affect the boot time in a processor. The size of the loader stream, presence of fill blocks, and init block inside the loader stream have the most impact on boot time. Boot time can be accurately estimated for a given loader stream by considering the impact of these factors.

## Boot Time Estimation

Assume the pre-boot requires a fixed duration under certain conditions. Engineers can separately compute the application loading time (boot time) for any loader stream using the boot ROM API. ADI has measured boot times with different sized loader streams in each boot mode. Using the data, linear equations were calculated for different boot modes supported in ADSP-SC835/SC839 SHARC-FX processors using the maximum system frequency (1 GHz SHARC-FX CCLK, Cortex-M33 400 MHz CCLK, and 500 MHz SYSCLK). It was determined that the boot time varies linearly with the size of the loader stream. Using the graphs as shown in Figure 1, linear equations are calculated in the form of $y = ax + b$ , where $\boldsymbol{x}$ is size of loader stream in KB and $\boldsymbol{y}$ is boot time in milliseconds. Using these equations, an engineer can estimate the boot time for any loader stream size.

The associated zip file[2] has the boot application code `Application_Code` folder that toggles a GPIO pin during start up to measure boot time. Similarly, the example code `BootTimeMsmt_ROMAPI` folder has code to call the ROM API boot.

## Hardware Setup Used

All measurements used the EV-SC835-SOM-EZKIT and EV-SOMCRR-EZKIT evaluation kits.

ADSP-SC835/SC839 SHARC-FX processors support normal and secure boot. Secure boot supports integrity, authentication, and confidentiality in three formats for protecting the IP and data:

- Plaintext (BLp) format
- Wrapped (BLw) format
- Keyless (BLx) format

The following sections have the derived boot time linear equations for different boot modes that support the ADSP-SC835 SHARC-FX processors.

- SPI Flash Boot
- xSPI Flash Boot
- UART Host Boot
- LP Host Boot
- Extended LP Host Boot

## SPI Flash Boot

The SPI flash boot (SYS_BMODE 1) mode supports booting from flash device using the SPI peripheral. In ADSP-SC835/SC839 SHARC-FX processors, the SPI1 instance drives the default SPI boot, which supports single, dual, and quad STR modes. Table 1 shows the different BCODEs supported for the maximum SPI clock frequency for the IS25LP512M flash device, which is present on the EV-SC835-SOM-EZKIT.

*Table 1: Supported BCODE Values for SPI Flash Boot*

| Boot Mode | Max SPI Clock (MHz) | BCODE Value |
|---|---|---|
| Single STR | 75 | 0x2 |
| Dual STR | 75 | 0x3, 0x5 |
| Quad STR | 75 z | 0x4, 0x9 |

BCODEs support the I/O modes of flash devices depending on number of dummy cycles needed for the flash. See the *SPI Master BCODE Configuration Lookup Table* in the *ADSP-SC83x/ADSP-2183x SHARC-FX Processor Hardware Reference*[1] for details.

Figure 1 through Figure 4 display calculated linear boot time equations for SPI flash boot modes at 62.5 MHz SPI clock frequency, including normal boot and secure boot with ECDSA-256 authentication.

*Figure 1: SPI Flash Normal Boot at 62.5 MHz*

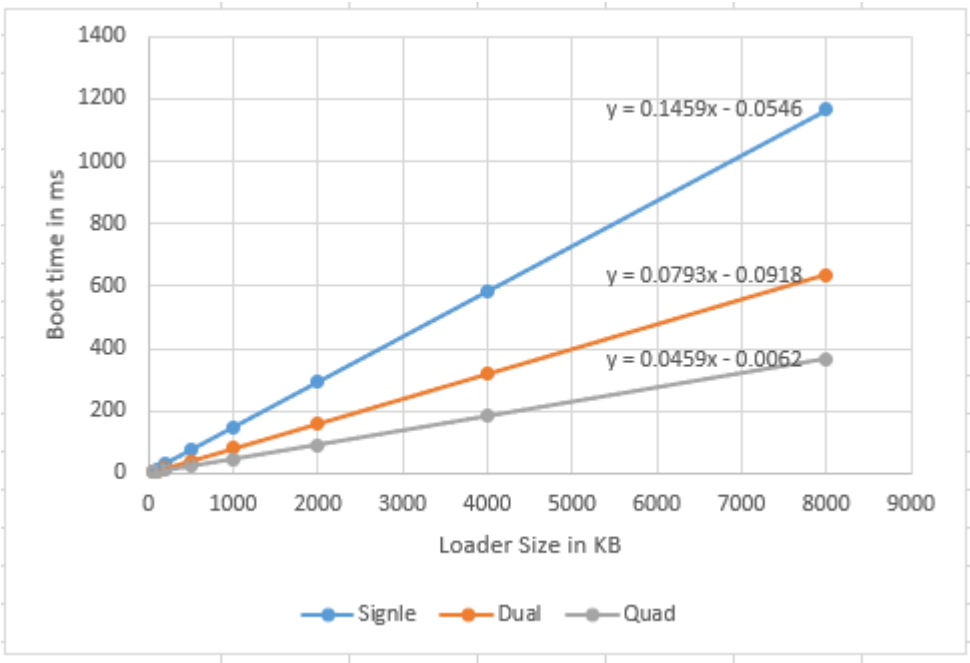



*Figure 2: SPI Flash BLP Secure Boot at 62.5 MHz*

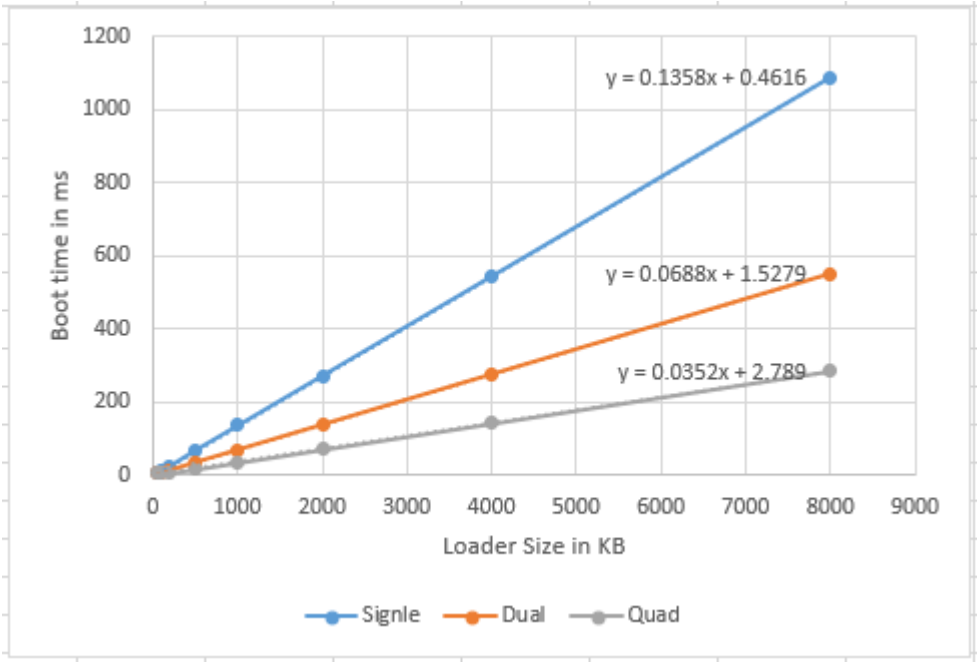


*Figure 3: SPI Flash BLx Boot at 62.5 MHz*

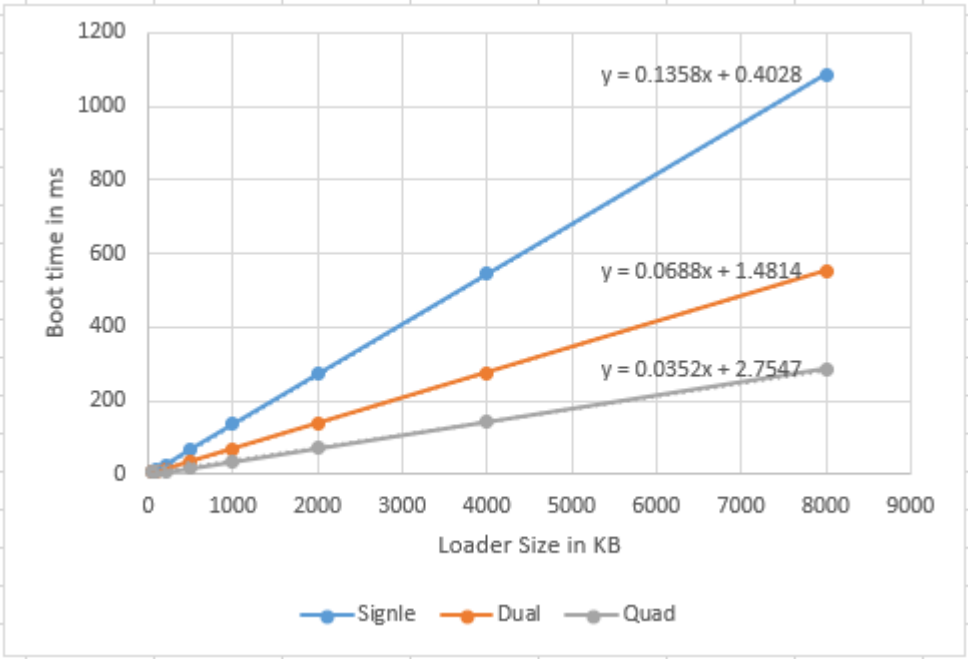
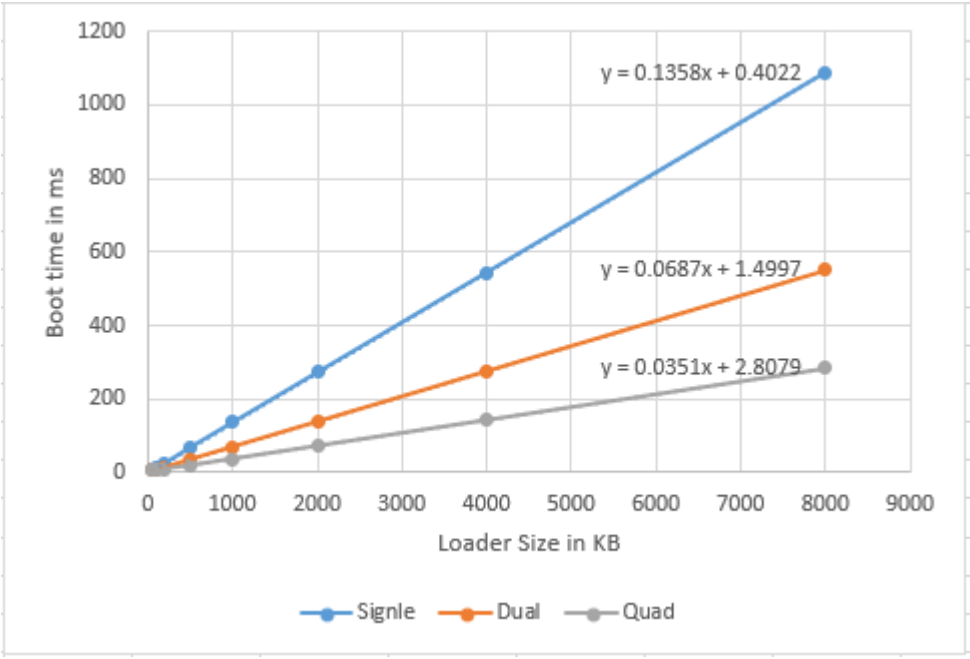



*Figure 4: SPI Flash BLw Secure Boot at 62.5 MHz*




A difference between normal and secure boot time can occur due to authentication and decryption routine actions performed by the crypto engine in secure boot,.

The numbers in Figure 1 through Figure 4 can be linearly extrapolated to a maximum 75 MHz SPI clock frequency. Table 2 shows the improved boot time estimate and measurement at the 75 MHz SPI clock frequency.

*Table 2: Boot Times for Maximum SPI Clock Frequency*

| Condition with SPI Single STR boot | Boot Time (ms) |
|---|---|
| Estimated Boot time at 62.5 MHz | 183.2 |
| Estimated Boot time after linear scaling at 75 MHz | 152.66 |
| Measured boot time at 75 MHz | 152.86 |

Expect a small error margin involving a tradeoff in CCLK and SYSCLK frequencies while attaining 75 MHz SPI CLK. Users can measure the boot time at the default 43 MHz SPI frequency for a power-on reset and estimate the boot time at 62.5 MHz or 75 MHz from linear scaling.

## xSPI Flash Boot

xSPI flash boot (SYS_BMODE 5) supports booting from hyperflash or legacy NOR flash devices using the xSPI peripheral, which includes all the bus modes from single STR to octal DTR. The xSPI flash boot supports a maximum 80 MHz xSPI clock frequency. The ADSP-SC835 family simultaneously supports two flash devices for booting, where SPI and xSPI signals reside on different port pins.

Different BCODE values in xSPI flash boot can support different frequency of operation. For example, BCODE value 6 supports the maximum xSPI clock frequency of 125 MHz. Autodetection routine in xSPI flash boot becomes more smarter in ADSP-SC835 family to detect the connected memory device (Hyperflash, Octal Flash and SPI flash with SFDP) automatically for the desired optimal settings without relying on the BCODE values for settings like dummy cycles, read commands etc.

See the xSPI Flash Boot BCODE Configuration Lookup table in the *ADSP-SC83x/ADSP-2183x SHARC-FX Processor Hardware Reference*[1] for details on BCODE definitions.

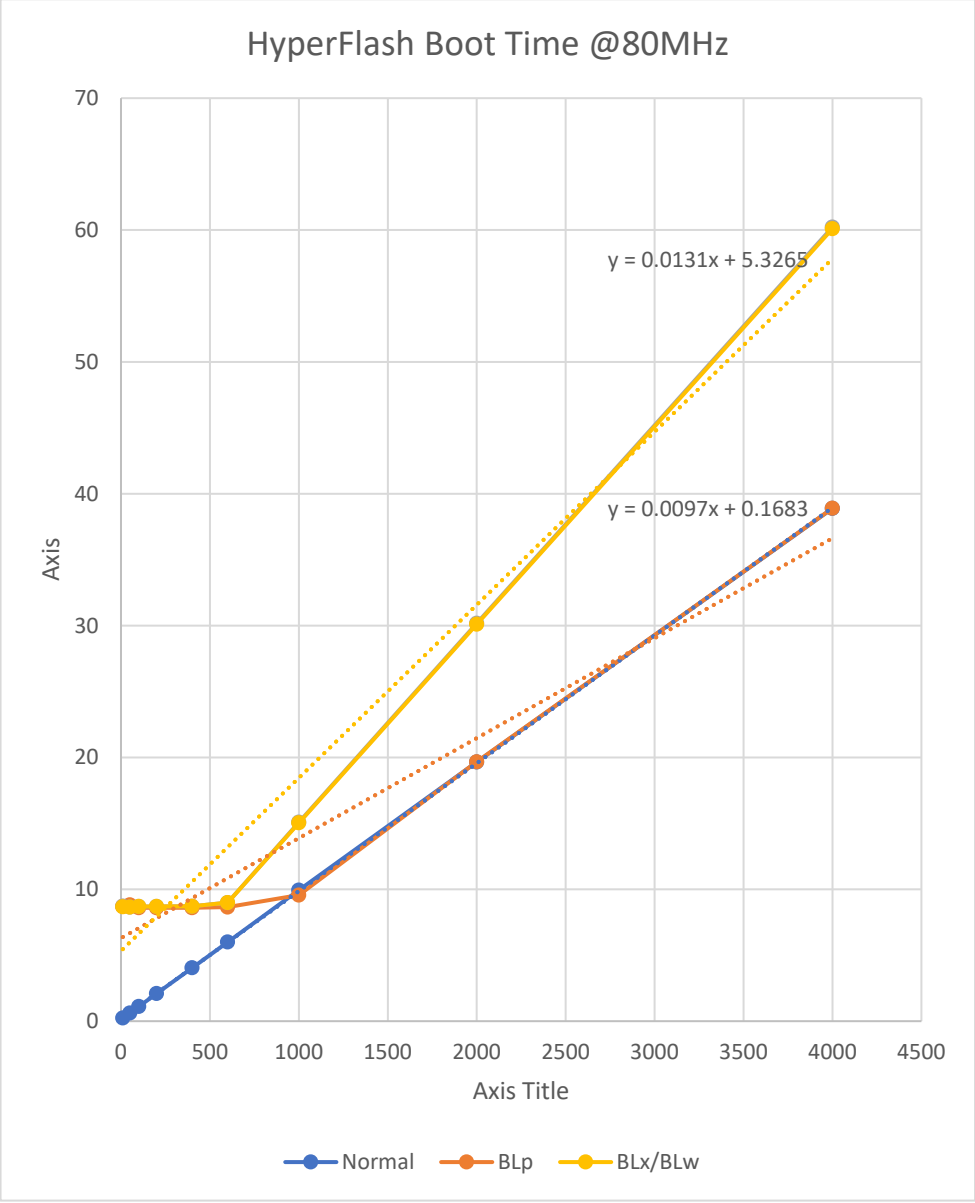
Figure 5 through Figure 7 shows the xSPI boot time captured for following devices:

1. Cypress HyperFlash (S71KL512SC0BHB003) at 80MHz of xSPI frequency
2. Macronix OctaFlash (MX66LM1G45G) at 80MHz of xSPI frequency
3. ISSI Quad Flash (IS25LP512M-RHL) at 80MHz of xSPI frequency

xSPI boot frequency in the ADSP-SC835 SHARC-FX processors is restricted to 80 MHz even though the xSPI peripheral supports up to 125 MHz frequency. The boot ROM does not support on chip xSPI PHY training by default. This can be supported through second stage boot loader, where PHY training must be done before xSPI boot

to achieve the optimal PHY DLL settings. An example will be added in a future revision of this EE Note.

*Figure 5: xSPI HyperFlash Boot Time at 100 MHz*




In xSPI boot, a considerable amount of boot time difference is observed between normal boot and secure boot (BLw/BLx). This is due to the extra time consumed in decryption operation by the crypto engine running at SYSCLK domain. It acts as a bottleneck when compared to fast xSPI Octal DTR mode in secure boot implementation. We have provision to improve this up to a good extent by increasing

the size of intermediate temporary buffer using a second stage boot loader. An example will be provided in a future revision of this application note.

*Figure 6: xSPI Quad-STR Boot Time at 80 MHz*

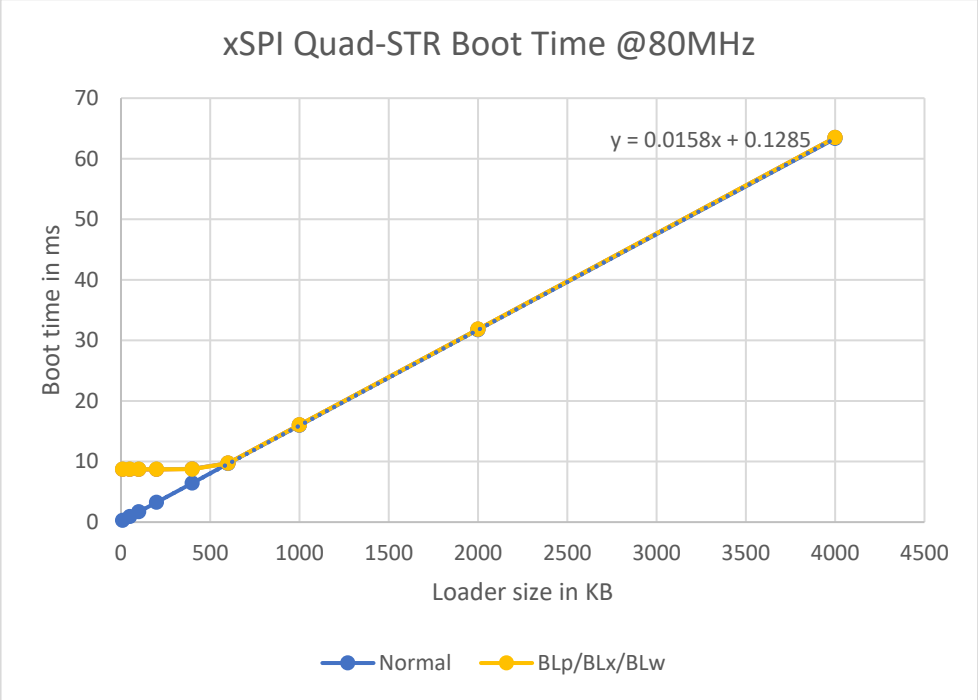
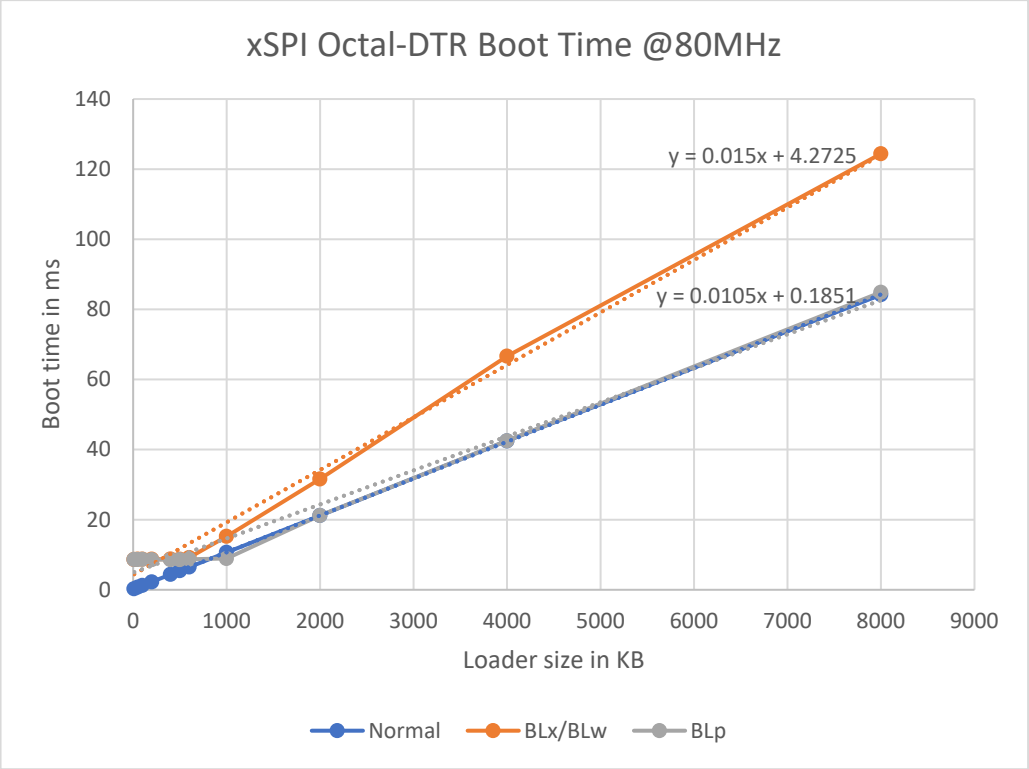


*Figure 7: xSPI Octal-DTR Boot Time at 125 MHz*




## Link Port External Host Boot

The link port boot (SYS_BMODE 4) and extended link port boot (SYS_BMODE 6) are external host boot modes in which the processor receives boot data from an external link port host through link port zero. For the link port boot mode (SYS_BMODE 4), the link port is configured as a receiver with an 8-bit SDR; the host needs to send the data in the same mode. For the extended link port boot mode (SYS_BMODE 6), the link port is configured initially as a receiver with a 2-bit SDR. Depending upon the first byte received from the host link port controller (processor), it configures itself in a new speed mode (such as 2-/4-/8-bit SDR/DDR). The host must send the data in the same mode. DMA controller performs all transfers from the link port to memory. The maximum supported operating frequency of the link port is 125 MHz, where the host boot source must drive the clock frequency. By using `Initcode` or OTP to configure the CGU for the maximum clock supported (SYSCLK 500 MHz and SCLK0 125 MHz), the host boot source drives the clock frequency. The link port receiver operates at an asynchronous frequency up to the maximum supported operating frequency.

Figure 8 provides the calculated linear boot time equation for link port normal boot at 62.5 MHz LP CLK.

*Figure 8: Link Port Normal Host Boot (SYS_BMODE 4) at 62.5 MHz (8-bit SDR)*

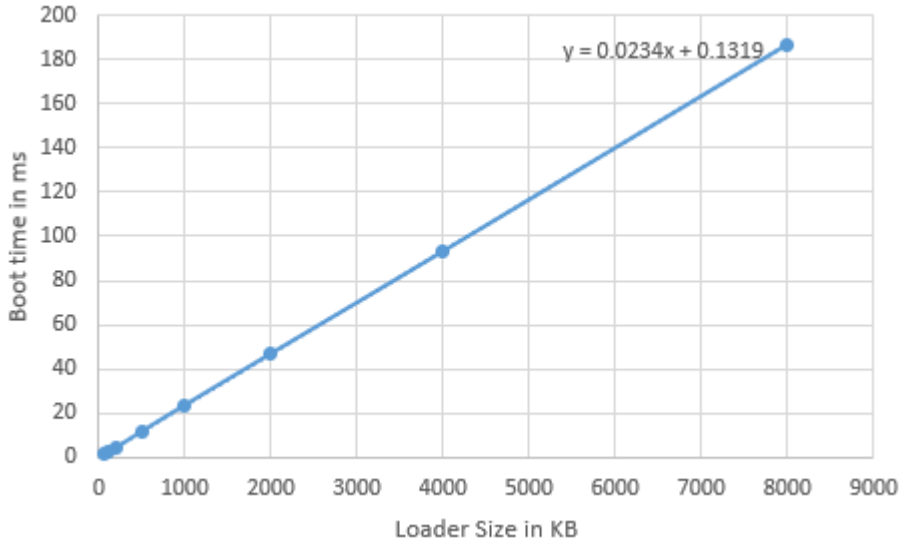
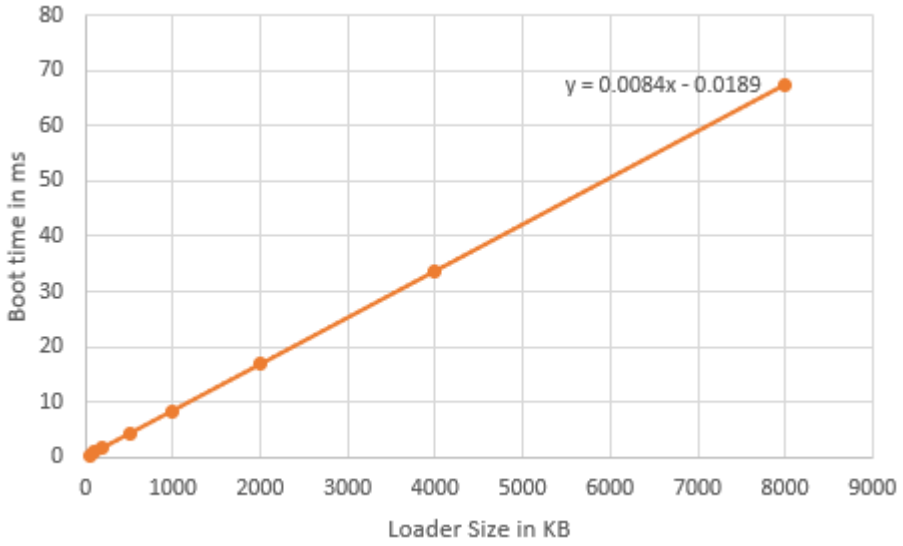



*Figure 9: Link Port Normal Host Boot (SYS_BMODE 6) at 62.5 MHz (8-bit DDR)*




Link port boot timings further improve using the125 MHz maximum clock frequency.

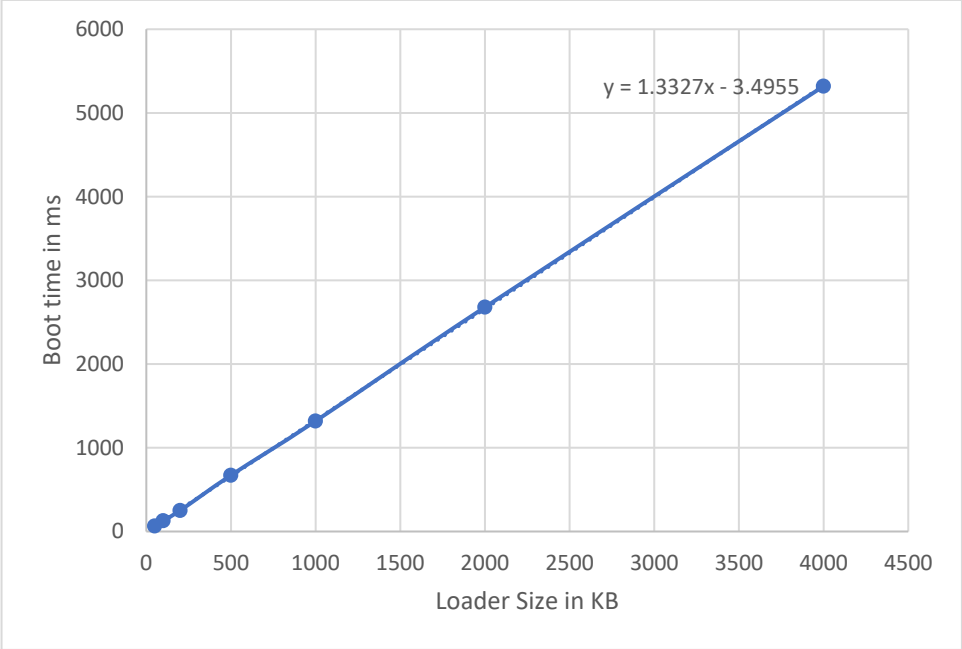
## UART External Host Boot

UART external host boot (SYS_BMODE 3) for the ADSP-SC835/SC839 SHARC-FX processors is an external host boot mode where the processor receives boot data from a UART host device connected to

the UART interface. UART0 is the default booting peripheral. The maximum UART clock supported for UART boot is 7.8 MHz. The clock can be achieved by using init code or OTP to configure the CGU for the maximum clock supported (SYSCLK 500 MHz and SCLK0 125 MHz). Because UART is a slow peripheral, the boot time for normal and secure boot modes is identical, with boot time primarily dependent on the peripheral loading time.

Figure 10 provides the calculated linear boot time equation for UART normal boot at 7.8 MHz UART CLK.

*Figure 10: UART External Host Boot at 7.8 MHz*



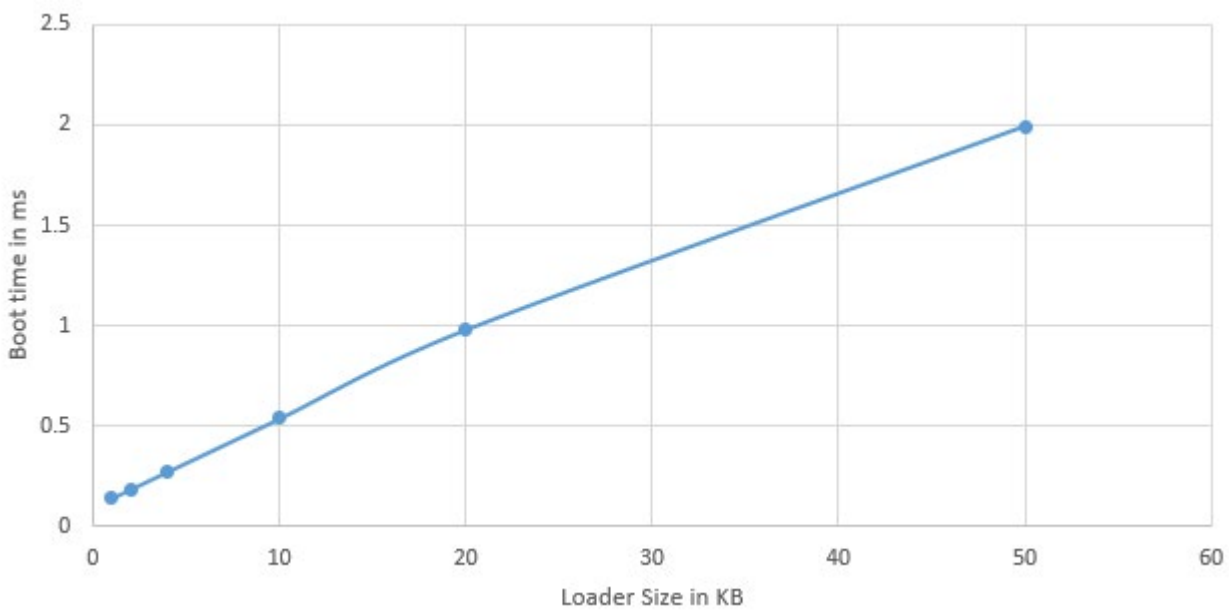

## Boot Time Nonlinearity

The figures from earlier sections provide calculated linear equations for boot time using varied sizes of loader stream. But, the linearity relationship is not consistent when the loader stream is smaller (both non-secure and secure boot). This section shows how boot time for a small loader stream follows a non-linear path in terms of non-secure boot and saturation time for a secure boot.

### Nonlinearity in Non-secure Boot Time

Figure 11 shows the boot time for SPI quad flash boot (BCODE  9) with a smaller loader stream. A size less than 20 KB is non-linear. Estimating the boot time using linear equations calculated in earlier sections is not accurate. ADI advises users to test the exact boot time for loader streams smaller than 20 KB.

*Figure11: SPI Quad Boot Time Nonlinearity at 62.5 MHz (CCLK= 1 GHz and SPI CLK=62.5 MHz)*




Nonlinearity in non-secure boot time is not affected by the boot ROM, but, rather is due to the smaller measured sample size for the smaller (KB) loader stream.

### Nonlinearity in Secure Boot Time

The pre-calculated SHA hash digest in the secure header starts the authentication process in parallel with the booting process, while loading the full image for processing hash and decryption. In large boot images, secure boot time is independent of the authentication routine. For smaller boot images, where loading time is less than the authentication routine completion time, secure boot time reaches a saturation point. Because of the parallel activity, the authentication routine determines the saturation point.

Figure 12 shows that the saturation level for SPI BLw secure quad (BCODE 9) boot (CCLK=1 GHz, SYSCLK=500 MHz, and SPI CLK=62.5 MHz) starts at the 200 KB stream size. The boot time saturates at approximately 9 milliseconds. The linear equation for computing the boot time of a BLw secure boot supports a loader stream size larger than 200 KB.

*Figure 12: SPI Secure Quad Non-linear Boot Time Saturation*

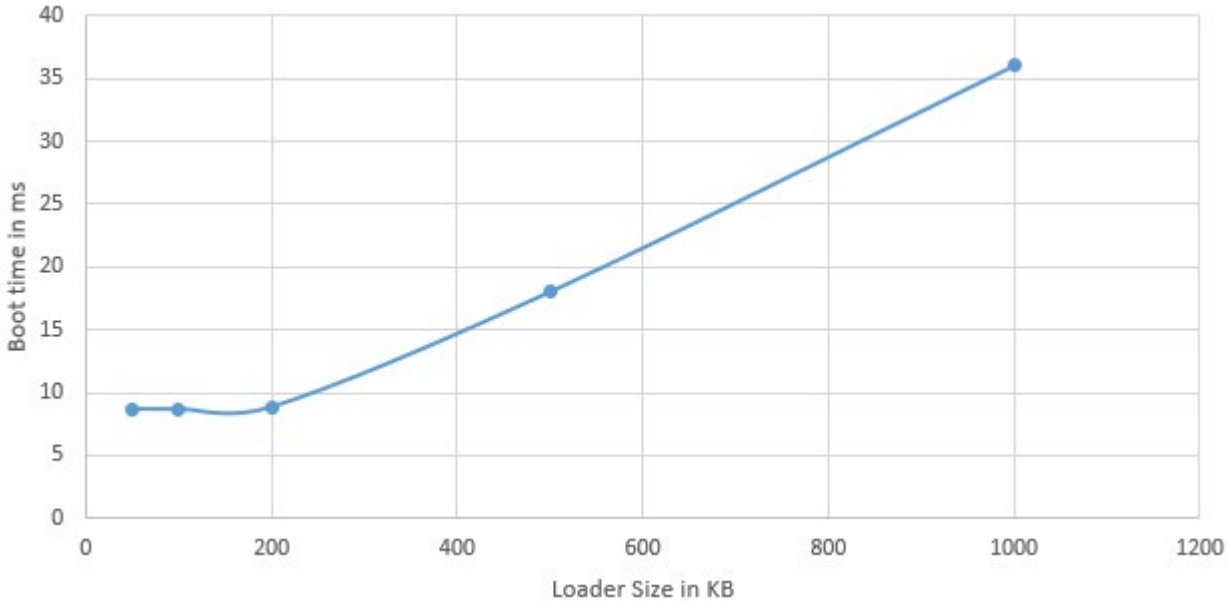



Table 3 shows the approximate saturation points for different secure boot using ECDSA-256 authentication in all the flash boot modes, with a maximum frequency (CCLK=1 GHz, SYSCLK=500 MHz, and SPI/xSPI CLK=62.5 MHz). Boot time is below saturation or approximately 9 ms.

*Table 3: Non-linear Saturation Point for Different Flash Secure Boot Modes*

| Secure Boot Mode | Saturation Point (KB) |
|---|---|
| SPI Master Single Mode | 50 |
| SPI Master Dual Mode | 100 |
| SPI Master Quad Mode | 200 |
| xSPI Master Single-STR | 50 |
| xSPI Master Dual-STR | 100 |
| xSPI Master Quad-STR | 200 |
| xSPI Master Single-DTR | 100 |
| xSPI Master Dual-DTR | 200 |
| xSPI Master Qual-DTR | 400 |
| xSPI Master Octal-STR | 400 |
| xSPI Master Octal-DTR | 800 |

Because the crypto engine runs on the SYSCLK, the table saturation points vary as the frequency changes. For example, when SYSCLK changes from 500 MHz to any lower value, the authentication routine completion time increases, which results in an increase of the saturation point.

## Boot Benchmarking

Boot time benchmarking is used to estimate boot ROM execution time for each stage. A general-purpose timer is used to count the cycles. The timer runs on CLKIN until CGU configuration is complete. After CGU configuration, the timer runs on SCLK0 frequency. The cycle counts (32-bit) are logged into the benchmark buffer (at the start address of the buffer). For example, if the start is address is `0x201ff300`, the next time stamp captured is logged on `0x201ff304` and so on. Boot time benchmarking can be enabled optionally through OTP using the `ROM_OTP_bcfg_benchmark_En` field. This feature is disabled by default.

In general, this feature can be used by user to estimate the overall boot time for their firmware without the effort of usual way of probing GPIO and RESET pin.

The associated zip file[2] contains the `Boot_Time_Benchmark_EHP1.xlsx` file which can be used to convert boot time stamps into corresponding boot stage time.

Consider an example where a 500 KB BLw 256 boot stream is booted at 31.25 MHz SPI clock STR mode (BCODE 2):

| Time Stamp Name | Time consumed from end of previous stage (ms) |
|---|---|
| After L2 memory initialization is complete | 0.92872 |
| After calibration is complete | 0.88388 |
| After the CGU is taken out of bypass | 0.04452 |
| After boot release of all secondary cores from reset | 0.016304 |
| When SH FX L1 memory initialization is complete | 0.165952 |
| When M33 (all core 1) L1 memory initialization is complete | 0.001568 |
| At the start of DDR calibration | 0.0012 |
| At the end of DDR calibration | 0.001168 |
| At the start of the main kernel process | 0.001776 |
| Before calling the Init function | 0.032176 |
| Before the start of data fetch (from flash memory or host) | 0.969744 |
| After the data fetch is complete (from flash memory or host) | 136.68632 |
| After authentication is complete (for secure boot). For normal boot mode, the time stamp is recorded and can be treated as redundant. | 0.020048 |
| Total Boot Time | 139.753376 |

The total measured boot time for this boot stream on actual silicon is approximately 139.9 ms. The user can get insight about how much each boot stage takes time from the above data. Most of the time is consumed in data fetch and decryption.

## Factors Affecting Total Boot Time

Application size primarily affects the boot time for the ADSP-SC835/SC839 SHARC-FX processors. All calculated linear equations provided in the earlier sections consider only the loader stream size. There are other factors that affect the total boot time, including pre-boot time, fill blocks, and init block. These factors are explained in the following sections, which make the total boot time estimation for a given application more accurate.

### Pre-boot Time

Pre-boot time accounts for the configuration of all system resources before starting the required boot operation. This includes:

- Core initialization
- SPU and SMPU configuration
- Secure debug key processing
- CGU configuration
- DMC configuration
- Fault configuration
- L1 memory initialization, etc.

CGU configuration and DMC initialization routines impact the pre-boot execution time when programming with the OTP. See the *ADSP-SC83x/ADSP-2183x SHARC-FX Processor Hardware Reference*[1] for details about pre-boot execution. Table 4 shows the pre-boot time under different conditions.

*Table 4: Pre-boot Times*

| Condition | ADSP-SC835 Pre-boot Time (ms) |
|---|---|
| Default | 2.167 ms |
| CGU configuration enabled (OTP programmed for 1 GHz CCLK) | 2.123 ms |

### Effect of Fill Blocks in Boot Time Estimation

A fill block instructs the boot kernel to perform a 32-bit memory fill of the memory region. Fill blocks help to minimize the size of a boot stream when an application contains large data arrays that must be initialized at application startup. The size of a loader stream does not depend on this 16-byte block. But, having multiple fill blocks in a fixed size loader stream does affect the total boot time, which includes the

extra time to process each fill block header and the time required for the DMA configuration in each block.

All of the computed boot time equations in previous sections did not account for fill blocks present in the loader stream. Figure 13 provides the calculated linear equation based on testing with SPI quad boot (BCODE 9) at 62.5 MHz SPI CLK. Use this equation to compute the extra boot time taken due to fill blocks. Currently, the extrapolated equation is used for all the controller boot modes which use MDMA channels, assuming fill block processing time is independent of peripheral loading time.

*Figure 13: Extra Boot Time Due to Fill Blocks*

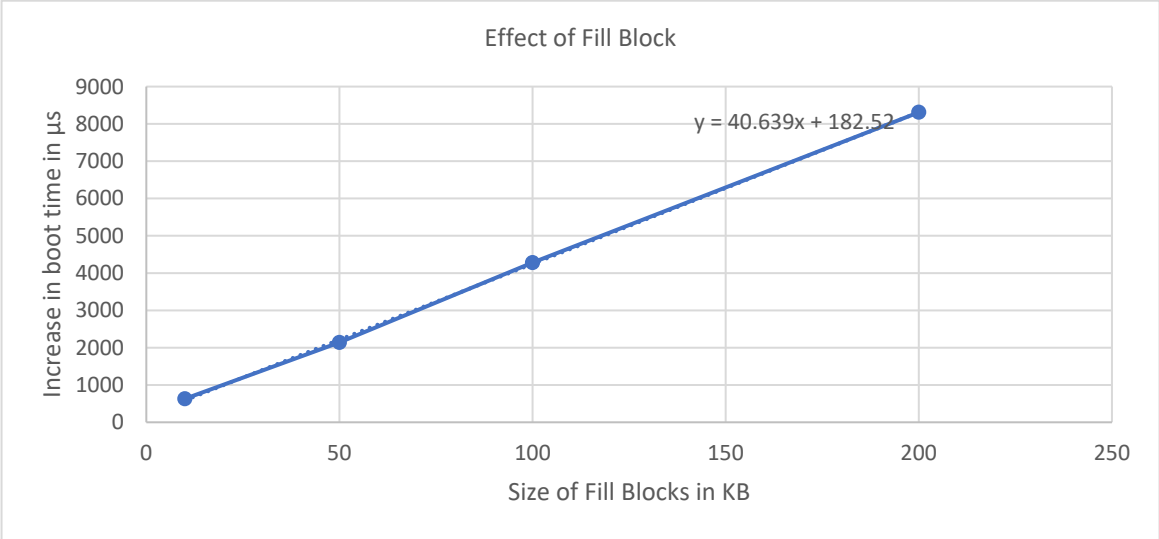



Figure 13 gives the measurement for 10 fill blocks present in the loader stream. For any other number of fill blocks, scale the boot time numbers by the same factor.

A larger loader stream always adds an extra penalty for consuming more space in the external flash, which also increases the overall system cost. Fill blocks, in such cases, help in reducing the loader stream size at the cost of additional total boot time. There should be a good trade-off between boot time and size of the loader stream.

## Init Block Effect on Boot Time Estimation

An initialization or init block instructs the boot kernel to perform a function call to the target address after the entire block has loaded. The function called is named as the initialization code (`Initcode`) routine. Use `Initcode` routines to speed up and customize booting mechanisms exposed by the boot kernel. Traditionally, engineers use an `Initcode` routine to set up the system PLL, bit rates, wait states, and external memory controllers. Significant boot time reductions happen when starting an init block early in the boot process.

Init code start time depends on all the features that are enabled inside the `Initcode` application, which impact the total boot time. For information on implementing an init block, see *ADSP-SC83x/ADSP-2183x SHARC-FX Processor Hardware Reference*[1].

The secure boot scenario does not support `Initcode` routines.

## Secure Boot Time Enhancement

With higher bus modes like Octal-DTR in xSPI flash boot mode, the crypto engine (that runs at maximum clock of 500MHz) hits a bottle neck for the authentication and decryption routine. The delay is due to the observed non-linearity in secure boot time, consuming more time than normal boot. However, this can be improved by increasing the temporary internal buffer size (the default size of internal buffer is 1KB) to 2KB, 4KB and 8KB. The buffer is used for fetching the data from the flash in page mode and, subsequently, performing the crypto operation using a multistage boot application. The following snap shows how to define a buffer of bigger size and assign the same to boot structure in an application using a hook function:

*Figure 14: secure boot time enhancement*

```
pBootConfig->bootBuffers.buffer[0].pBuffer = &tempBuffer0[0];
pBootConfig->bootBuffers.buffer[0].size = (uint32_t)2048;

pBootConfig->bootBuffers.buffer[1].pBuffer = &tempBuffer1[0];
pBootConfig->bootBuffers.buffer[1].size = (uint32_t)2048;
```

Table 5 shows the improvement in secure boot time for xSPI Octal-DTR mode at 125 MHz speed.

*Table 5: Enhanced boot time with larger size of internal buffer*

| Size of Internal Buffer (Bytes) | Secure Boot Time (ms) | |
|---|---|---|
| | BLp | BLw |
| 1024 | 71.58 | 120.3 |
| 2048 | 47.12 | 86.18 |
| 4096 | 47.12 | 69.49 |
| 8192 | 47.12 | 61.27 |

## Comparison of Boot Time Among Different Processors

This section provides a total boot time comparison for various processors including: ADSP-SC57x, ADSP-2156x, ADSP-2159x/ADSP-SC59x, ADSP-SC598 and ADSP-SC83x families. The comparisons provide the best boot time for all the variants, whether it is an SPI quad-STR boot for the ADSP-SC57x family, an OSPI quad-DTR boot for ADSP-2156x family, an OSPI quad-DTR boot for ADSP-2159x/ADSP-SC59x and ADSP-SC598 family, or an xSPI octal-DTR boot for ADSP-SC83x family.

Table 6 through Table 9 show the boot time comparisons across all three processor families for the different boot modes: Normal, Secure BLp, Secure BLx, and Secure BLw.

### *Normal Boot Time Comparison*

*Table 6: Normal Boot Time Comparison*

| Loader Stream Size (KB) | SPI Quad-STR Boot (ms) | OSPI Quad-DTR Boot (ms) | | | xSPI Octal-DTR Boot (ms) |
|---|---|---|---|---|---|
| | ADSP-SC573 | ADSP-21569 | ADSP-21593 | ADSP-SC598 | ADSP-SC835 |
| | SPI Clock=75 MHz | OSPI Clock= 62.5 MHz | | | xSPI Clock = 125 MHz |
| 500 | 24.5325 | 10.0755 | 10.2661 | 8.2054 | 3.477 |
| 1000 | 43.2825 | 18.5255 | 18.4661 | 16.4054 | 6.834 |
| 2000 | 80.7825 | 35.4255 | 34.8661 | 32.8054 | 13.55 |
| 4000 | 155.7825 | 69.2255 | 67.6661 | 65.6054 | 27.18 |
| 8000 | 305.7825 | 136.8255 | 133.2661 | 131.2054 | 53.86 |
| 12000 | 455.7825 | 204.4255 | 198.8661 | 196.8054 | 80.54 |

### *BLp Secure Boot Time Comparison*

*Table 7: BLp Secure Boot Time Comparison*

| Loader Stream Size (KB) | SPI Quad-STR Boot (ms) | OSPI Quad-DTR Boot (ms) | | | xSPI Octal-DTR Boot (ms) |
|---|---|---|---|---|---|
| | ADSP-SC573 | ADSP-21569 | ADSP-21593 | ADSP-SC598 | ADSP-SC835 |
| | SPI Clock=75 MHz | OSPI Clock= 62.5 MHz | | | xSPI Clock = 125MHz |
| 500 | 40.23 | 17.2902 | 14.9717 | 12.6565 | 8.607 |
| 1000 | 62.68 | 27.2402 | 24.1717 | 20.4565 | 8.914 |
| 2000 | 107.583 | 47.1402 | 42.5717 | 36.0565 | 19.09 |
| 4000 | 197.383 | 86.9402 | 79.3717 | 67.2565 | 41.51 |
| 8000 | 376.9 | 166.5402 | 152.9717 | 129.6565 | 73.88 |
| 12000 | 556.5 | 246.1402 | 226.5717 | 192.0565 | 107.55 |

### BLx Secure Boot Time Comparison

*Table 8: BLx Secure Boot Time Comparison*

| Loader Stream Size (KB) | SPI Quad-STR Boot (ms) | OSPI Quad-DTR Boot (ms) | | | xSPI Octal-DTR Boot (ms) |
|---|---|---|---|---|---|
| | ADSP-SC573 | ADSP-21569 | ADSP-21593 | ADSP-SC598 | ADSP-SC835 |
| | SPI Clock=75 MHz | OSPI Clock= 62.5 MHz | | | xSPI Clock = 125MHz |
| 500 | 54.877 | 19.7049 | 16.8513 | 12.6728 | 8.726 |
| 1000 | 92.627 | 30.2549 | 26.5513 | 20.4728 | 15.25 |
| 2000 | 168.127 | 51.3549 | 45.9513 | 36.0728 | 31.61 |
| 4000 | 319.127 | 93.5549 | 84.7513 | 67.2728 | 66.64 |
| 8000 | 621.127 | 177.9549 | 162.3513 | 129.6728 | 124.4 |
| 12000 | 923.127 | 262.3549 | 239.9513 | 192.0728 | 184.27 |

### BLw Secure Boot Time Comparison

*Table 9: BLw Secure I Boot Time Comparison*

| Loader Stream Size (KB) | SPI Quad-STR Boot (ms) | OSPI Quad-DTR Boot (ms) | | | xSPI Octal-DTR Boot (ms) |
|---|---|---|---|---|---|
| | ADSP-SC573 | ADSP-21569 | ADSP-21593 | ADSP-SC598 | ADSP-SC835 |
| | SPI Clock=75 MHz | OSPI Clock= 62.5 MHz | | | xSPI Clock = 125MHz |
| 500 | 54.026 | 19.5518 | 17.2634 | 12.6808 | 8.726 |
| 1000 | 91.726 | 30.1018 | 26.4134 | 20.4808 | 15.25 |
| 2000 | 167.126 | 51.2018 | 44.7134 | 36.0808 | 31.61 |
| 4000 | 317.926 | 93.4018 | 81.3134 | 67.2808 | 66.64 |
| 8000 | 619.526 | 177.8018 | 154.5134 | 129.6808 | 124.4 |
| 12000 | 921.126 | 262.2018 | 227.7134 | 192.0808 | 184.2725 |

## References


[1] *ADSP-SC83x/ADSP-2183x SHARC-FX Processor Hardware Reference.* Rev 0.1. June 2024, Analog Devices, Inc.

[2] *EE450v01.zip*. Rev 1, August 2024, Analog Devices, Inc.


## Document History

| Revision | Description |
|---|---|
| *Rev 1 – August 6, 2024* | Initial Release |