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Estimating Power for ADSP-SC596/SC598 SHARC+ Processors

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Introduction

This Engineer-to-Engineer application note describes how to estimate power consumption on the ADSP-SC596/SC598 processors, which include the SHARC+® high-performance cores and several peripherals, accelerators, and Direct Memory Access (DMA) channels. These processors have multiple power domains [6] and clock domains. Analog Devices provides a simple methodology for estimating the total System-on-Chip (SoC) power consumption that is dependent on processor activity usage.

Power estimates are based on design simulations and characterization data, measured across power supply voltage, core and system clock frequency, and junction temperature (T_J). The power can vary depending on how a customer uses the on-chip ADSP-SC596/SC598 SHARC+ Processor resources. Engineers cannot accurately estimate power consumption without an understanding of the components in use and their usage patterns. By providing the usage parameters, board designers can obtain accurate consumption estimates for developing power supply and thermal relief solutions for the ADSPSC596/SC598 SHARC+ processor-based products.

Refer to the ADSP-SC596/SC598: SHARC+ Dual-Core DSP with Arm Cortex-A55 Data Sheet [1] for specific details described in this EE Note:

- O*perating conditions*-supported power supply ranges
- *Electrical Characteristics* and *Total Internal Power Dissipation*-current specifications

The ADSP-SC596-SC598 Power Calculator Tool Rev00 [2] software performs power calculations and as directed with this EE note. The software helps users obtain a total power profile by populating the spreadsheet cells with data from the processor data sheet [1] and calculations specific for an intended application. The EE-440 note explains the situations related to the power calculator that the data sheet does *not* describe.

This EE note also describes how to provide the input to the power calculator software to obtain a full power profile for an application. It describes how the calculations are done and how the results contribute to the overall power profile.

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Power Domains

There are multiple power domains associated with the ADSP-SC596/SC598 SHARC+ processor. Its total power consumption is the sum of the power consumed across all the power domains.

These power domains are significant contributors to the overall power profile:

- V_{DD_INT}-most internal on-chip logic (for example, core, accelerators, DMA engines, etc.)
- V_{DD_EXT}-for example, I/O pad ring, JTAG
- V_{DD_REF}-I/O reference supply
- V_{DD_DMC}-DDR controller

The power consumption from the V_{DD_ANA} power supply for HADC/TMU analog blocks is insignificant and not considered part of the power calculations.

Estimating Internal Power Consumption ($P_{DD\_INT\_TOT}$)

The total power consumption for the on-chip logic (V_{DD_INT} supply) is the sum of the static (leakage) and dynamic (switching) power parts. The dynamic part depends primarily on processor activity, which includes the instruction execution sequence, the data operands involved, and the instruction rate on each core. The dynamic part also depends on the number of active peripherals and accelerators, their clock rates, and any associated DMA data traffic. Dynamic current is also influenced by temperature and voltage. The static part is independent of processor activity and is *only* a function of temperature and voltage.

The internal current ($I_{DD\_INT\_TOT}$) consumed by the ADSP-SC596/SC598 SHARC+ Processors includes the components in the Table 1.

Table 1: Internal Current ($I_{DD\_INT\_TOT}$) Components

Internal Current Component	Leakage / Dynamic Current	Processor Area
IDD_INT_STATIC	Leakage	n/a
IDD_INT_CCLK_SHARC0_DYN	Dynamic-CCLK domain	SHARC+ core 1
IDD_INT_CCLK_SHARC1_DYN	Dynamic-CCLK domain	SHARC+ core 2
IDD_INT_CCLK_A55_DYN	Dynamic-CCLK domain	Cortex A55 core
IDD_INT_DCLK_DYN	Dynamic-DCLK domain	No other activity
IDD_INT_SYSCLK_DYN	Dynamic-SYSCLK domain	No other activity
IDD_INT_SCLK0_DYN	Dynamic-SCLK0 domain	No other activity
IDD_INT_SCLK1_DYN	Dynamic-SCLK1 domain	No other activity
IDD_INT_OCLK_DYN	Dynamic-OCLK domain	No other activity
IDD_INT_DMA_DR_DYN	Dynamic	DMA activity
IDD_INT_ACCL_DYN	Dynamic	FIR/IIR accelerator blocks

The total internal current is the sum of each of the Table 1 components, where there is a single static power component and several dynamic power components that must be included in the overall power profile.

The processor data sheet provides maximum specifications for I_{DD_INT} at specific voltages, frequencies, and temperatures. The following sections describe how to use the data sheet information to calculate the total power requirements of a specific application.

Estimating Total I_{DD_INT} Dynamic Current

Because of the multi-featured clock and power capabilities of the ADSP-SC596/SC598 SHARC+ Processors, there are many contributors to the overall dynamic component. These components consist of power consumed by the core. While an application can disable clocks to the different domains, each component must be evaluated to determine what factors to account for. These components define how to compute the power dissipation for any combination of active domains.

The dynamic current data (part of this EE note) and associated power calculator spreadsheet applies to maximum junction temperature of 125°C and the worst-case (highest power) fabrication process.

Core Dynamic Current

The Core Dynamic Current includes the currents for $I_{DD\_INT\_CCLK\_A55\_DYN}$, $I_{DD\_INT\_CCLK\_SHARC0\_DYN}$, and $I_{DD\_INT\_CCLK\_SHARC1\_DYN}$.

The ADSP-SC596/SC598 SHARC+ Processor data sheet[2] provides the baseline dynamic current consumption specifications that are obtained with the processor running a *typical* application. It is represented in the data sheet by the $I_{DD\text{-}TYP}$ specification.

However, these conditions do not represent all possible application code. The silicon process variation is also ignored, which influences the power profile because of non-uniform transistor physics across the silicon. When making decisions regarding the power supply design, the worst-case scenario must always be considered.

The above assumptions are addressed using different tables in the data sheet, to extrapolate and obtain the maximum requirements for the power supply designs:

- *Dynamic Current* tables-provide the maximum (across process and temperature) core dynamic current specification as a function of voltage (V_{DD_INT}) and frequency (f_{CCLK}), while running *typical* application code.
- *Activity Scaling Factor (ASF)* tables–describe discrete dynamic activity levels to provide insight on how the dynamic current scales with changing loads on the core.

Using these combined specifications, the dynamic component of core power consumption can be obtained by multiplying the baseline spec obtained from the *Dynamic Current* tables and the associated *Activity Scaling Factor*, as further explored in the following sections.

ARM Cortex-A55 ASF Vectors

The Activity Scaling Factors (ASFs) for ARM Cortex-A55 Core table define these vectors:

- $I_{DD-IDLE}$–ARM core executing the IDLE instruction ("idle activity") only
- $I_{DD-DHRYSTON}$–ARM core executing Dhrystone benchmark algorithm
- $I_{DD-2575}$–ARM core executing 25% peak activity and 75% idle activity
- $I_{DD-5050}$–ARM core executing 50% peak activity and 50% idle activity
- $I_{DD-7525}$–ARM core executing 75% peak activity and 25% idle activity (used for I_{DD_TYP} spec)
- $I_{DD-PEAK\_100}$–ARM core continuously thrashes cache memory with maximum data changes, executing mix floating point and arithmetic instructions with PMU events enabled (peak activity).

The test code used to measure $I_{DD-PEAK\_100}$ represents the worst-case core operation and is not sustainable under normal application conditions.

In addition to the Activity Scaling Factors, the power calculator defines the following vector on the *Core Activity Factors* tab:

- $I_{DD-CLOCK\_GATED}$–Arm core clock disabled (no dynamic power)

SHARC+ Core ASF Vectors

The Activity Scaling Factors (ASFs) for the SHARC+ Core0 table in the data sheet defines these vectors:

- $I_{DD-IDLE}$–SHARC+ core executing the IDLE instruction only
- I_{DD-NOP}–SHARC+ core executing 100% NOPs
- I_{DD-TYP_3070}–SHARC+ core executing 30% floating-point (FP) multiply/add/subtract and store instructions and 70% NOPs
- I_{DD-TYP_5050}–SHARC+ core executing 50% floating-point (FP) multiply/add/ subtract and store instructions and 50% NOPs
- I_{DD-TYP_7030}–SHARC+ core executing 70% floating-point (FP) multiply/add/ subtract and store instructions and 30% NOPs (used for I_{DD_TYP} specification)
- $I_{DD-PEAK\_100}$–SHARC+ core executing 100% floating-point (FP) multiply/add/subtract and store instructions
- I_{DD-LS}: SHARC+ core in light sleep mode

The test code used to measure $I_{DD-PEAK\_100}$ represents the worst-case core operation and is not sustainable under normal application conditions.

In addition to the ASFs (Activity Scaling Factor), the ADSP-SC596-SC598 Power Calculator Tool Rev00 [2] software defines the following vector on the *Core Activity Factors* tab:

- $I_{DD-CLOCK\_GATED}$: SHARC+ core clock disabled (no dynamic power)

Low Power Features

The ADSP-SC596/SC598 SHARC+ processors provide an additional power-saving feature to reduce power consumption in the on-chip L1 memory and when the core is idle.

- Low Power Idle Mode (core light sleep)–When the core goes into the idle state, upon executing the IDLE instruction, there exists active/switching power associated with all active clocks (even though there is no activity inside the core). To reduce the power, program the core light sleep enable field, which is a core clock gating mechanism (core light sleep) for switching off these clocks.

The core light sleep mechanism is effective only when the processor is booted, and *not* when executing from an emulator.

Additional modes such as Memory Sleep and Memory Shutdown mentioned in the SHARC+ Core Programming Reference do not provide significant power savings.

Using ASFs to Establish Application-Specific Total Average Power Profile

Once the baseline dynamic current specification from the *Dynamic Current* tables is obtained from the spread sheet cell associated with the CCLK frequency (fCCLK) and the input voltage (VDD_INT) of interest, the next step is to analyze the application to identify and apply the proper Activity Scaling Factors The application must be broken down into percentages of time spent in states associated with one of these standard power vectors. With knowledge of the program flow and an estimate of the percentage of time spent at each activity level, the baseline dynamic current and the corresponding ASF can be used to determine the average dynamic current consumption for each core.

For example, $I_{DD\_INT\_CCLK\_SHARC0\_DYN}$ for the SHARC+ core0 in a specific application can be calculated according to Equation 1, where "%" is the percentage of the overall time that the application spends in that state:

Equation 1 Total Individual Core Dynamic Current

$$I_{DD\_INT\_CCLK\_SHARC0\_DYN} = (\%\ Peak\ activity\ level \times I_{DD\text{-}PEAK\_100}\ ASF \times I_{DD\_INT\_CCLK\_SHARC0\_DYN}) +$$
$$(\%\ High\ activity\ level \times I_{DD\text{-}TYP\_7030}\ ASF \times I_{DD\_INT\_CCLK\_SHARC0\_DYN}) +$$
$$(\%\ Moderate\ activity\ level \times I_{DD\text{-}TYP\_5050}\ ASF \times I_{DD\_INT\_CCLK\_SHARC0\_DYN}) +$$
$$(\%\ Low\ activity\ level \times I_{DD\text{-}TYP\_3070}\ ASF \times I_{DD\_INT\_CCLK\_SHARC0\_DYN}) +$$
$$(\%\ NOP\ activity\ level \times I_{DD\text{-}NOP}\ ASF \times I_{DD\_INT\_CCLK\_SHARC0\_DYN}) +$$
$$(\%\ IDLE\ activity\ level \times I_{DD\text{-}IDLE}\ ASF \times I_{DD\_INT\_CCLK\_SHARC0\_DYN}) +$$
$$(\%\ CCLK\ disabled \times I_{DD\text{-}CLOCK\_GATED}\ ASF \times I_{DD\_INT\_CCLK\_SHARC0\_DYN}) +$$
$$(\%\ LS\ activity\ level \times I_{DD\text{-}LS}\ ASF \times I_{DD\_INT\_CCLK\_SHARC0\_DYN})$$

Note that the $I_{DD\_INT\_CCLK\_SHARC0\_DYN}$ output is the average current, whereas the $I_{DD\_INT\_CCLK\_SHARC0\_DYN}$ inputs are with ASF = 1.0. Consider a SHARC+ core0 application that is continuously running and never idles, where the core activity is:

- $I_{DD\text{-}PEAK\_100}$ activity level–10%
- $I_{DD\text{-}TYP\_7030}$ activity level–20%
- $I_{DD\text{-}TYP\_5050}$ activity level–50%
- $I_{DD\text{-}TYP\_3070}$ activity level–10%
- $I_{DD\text{-}NOP}$ activity level–10%
- $I_{DD\text{-}LS}$, $I_{DD\text{-}IDLE}$ and $I_{DD\text{-}CLOCK\_GATED}$ activity level –0%

Applying Equation 1 to this profile yields:

$$I_{DD\_INT\_CCLK\_SHARC0\_DYN} = (0.1 \times I_{DD\text{-}PEAK\_100}\ ASF \times I_{DD\ INT\_CCLK\_SHARC0\_DYN}) + (0.2 \times I_{DD\text{-}TYP\_7030}\ ASF \times I_{DD\_INT\_CCLK\_SHARC0\_DYN}) + (0.5 \times I_{DD\text{-}TYP\_5050}\ ASF \times I_{DD\_INT\_CCLK\_SHARC0\_DYN}) + (0.1 \times I_{DD\text{-}TYP\_3070}\ ASF \times I_{DD\_INT\_CCLK\_SHARC0\_DYN}) + (0.1 \times I_{DD\text{-}NOP}\ ASF \times I_{DD\_INT\_CCLK\_SHARC0\_DYN})$$

Estimating System Clock Tree Currents

ADSP-SC596/SC598 SHARC+ processors have multiple system clock domains to clock the system buses, various peripherals, DMA controllers, L2 memory, and a DDR controller. Each of these clock domains consumes power that dissipates in the internal power domain due to its respective clock toggling inside the chip. Additional power consumed by the peripherals and DMA (when active) is attributed to individual peripherals and DMAs running in the system. The power is estimated separately and added to the baseline system power when the total power profile is calculated.

There are four major system clock domains on the ADSP-SC596/SC598 SHARC+ processors:

- SYSCLK
- SCLK0
- SCLK1
- DCLK

There is also a programmable output clock (OCLK), which can be generated by one of the CGUs and routed to an external pin on the processor. It has a small influence on the overall power profile.

To estimate the impact to the current consumed in the V_{DD_INT} domain because of each of these system clocks, unique scaling factors are furnished in the processor data sheet.

The factors represent the currents consumed per MHz per volt in each system clock domain; therefore, V_{DD_INT} is in terms of volts, and f_{XXX} is in terms of MHz in the system clock dynamic current equations:

- $I_{DD\_INT\_DCLK\_DYN} = 0.097 \times V_{DD\_INT} \times f_{DCLK}$
- $I_{DD\_INT\_SYSCLK\_DYN} = 0.792 \times V_{DD\_INT} \times f_{SYSCLK}$
- $I_{DD\_INT\_SCLK0\_DYN} = 0.451 \times V_{DD\_INT} \times f_{SCLK0}$
- $I_{DD\_INT\_SCLK1\_DYN} = 0.014 \times V_{DD\_INT} \times f_{SCLK1}$
- $I_{DD\_INT\_OCLK\_DYN} = 0.108 \times V_{DD\_INT} \times f_{OCLK}$

The scaling factor for each of the system clock dynamic current equations is in units of mA/MHz/V; therefore, the result for each is in terms of mA.

Estimating DMA Contribution to Internal Dynamic Current ($I_{DD\_INT\_DMA\_DR\_DYN}$)

Different types of DMA transactions in the system result in additional power consumption:

- DMA transfers between the various memory spaces
- DMA transfers from memory to peripherals
- DMA transfers from peripherals to memory

Power consumption varies with the number of running DMA channels and the rate at which they move data through the system. To estimate DMA power consumption, three power profiles are available in the *DMA Peripheral Usage, pull-down in the VDD_INT Clock Domains & DMA Rates* table in the ADSP-SC596-SC598 Power Calculator Tool Rev00 [2] software:

- **HIGH**–comprised of high-speed MDMA, multiple low-speed MDMAs, and several high-speed peripheral DMAs running simultaneously in the system for a combined throughput of approximately **4695** MBPS.
- **MEDIUM**–comprised of medium-speed MDMA, multiple low-speed MDMAs, and several low-speed peripheral DMAs running simultaneously in the system for a combined throughput of approximately **3665** MBPS.
- **LOW**–comprised of low-speed MDMA and several low-speed peripheral DMAs running simultaneously in the system for a combined throughput of approximately **453** MBPS.

To estimate the DMA dynamic current ($I_{DD\_INT\_DMA\_DR\_DYN}$) in the application, the combined data bandwidth of all the DMAs running in the system determines which profile to select as the closest match to the actual application and use as the $I_{DD\_INT\_DMA\_DR\_DYN}$ component for the $I_{DD\_INT\_TOT}$ calculation.

High DMA Configuration

The following peripheral and memory DMAs are active in this high DMA configuration:

- 8 SPORTS at 62.5 MHz in RX mode with PRI/SEC enabled (writing data to L2 memory)
- 8 SPORTS at 62.5 MHz in TX mode with PRI/SEC enabled (reading data from L2 memory)
- SPI2/SPI1 in quad mode, SPI0 in dual mode TX operation at 62.5 MHz (reading data from L2 memory)
- LP TX mode at 125 MHz (reading data from L2 memory)
- One times medium speed MDMA transferring data from L1 to L2 memory
- One times medium speed MDMA transferring data from L2 to L1 memory
- One times medium speed MDMA transferring data from DDR to L1 memory
- One times high speed MDMA transferring data from L1 memory to DDR

In this configuration, the $I_{DD\_INT\_DMA\_DR\_DYN}$ component (see the *V_{DD_INT} DMA Usage* tab of the ADSP-SC596-SC598 Power Calculator Tool Rev00 [2] software) is 220 mA.

Medium DMA Configuration

The following peripheral and memory DMAs are active in this medium DMA configuration:

- 8 SPORTS at 62.5 MHz in RX mode with PRI/SEC enabled (writing data to L2 memory)
- 8 SPORTS at 62.5MHz in TX mode with PRI/SEC enabled (reading data from L2 memory)
- SPI2/SPI1 in quad mode, SPI0 in dual mode TX operation at 62.5MHz (reading data from L2 memory)
- LP TX mode at 125 MHz (reading data from L2 memory)
- One times medium speed MDMA transferring data from L1 to L2 memory
- One times medium speed MDMA transferring data from L2 to L1 memory

In this configuration, the $I_{DD\_INT\_DMA\_DR\_DYN}$ component (see the *$V_{DD\_INT\ DMA}$ Usage* tab of the ADSP-SC596-SC598 Power Calculator Tool Rev00 [2] software) is 143 mA.

Low DMA Configuration

The following peripheral and memory DMAs are active in this low DMA configuration:

- 8 SPORTS at 62.5 MHz in RX mode with PRI/SEC enabled (writing data to L2 memory)
- 8 SPORTS at 62.5 MHz in TX mode with PRI/SEC enabled (reading data from L2 memory)
- SPI2/SPI1 in quad mode, SPI0 in dual mode TX operation at 62.5 MHz (reading data from L2 memory)
- LP TX mode at125 MHz (reading data from L2 memory)

In this configuration, the $I_{DD\_INT\_DMA\_DR\_DYN}$ component (see the *$V_{DD\_INT\ DMA}$ Usage* tab of the ADSP-SC596-SC598 Power Calculator Tool Rev00 [2] software is 36 mA.

The $I_{DD\_INT\_DMA\_DR\_DYN}$ component value specified for each of the three previous configurations is the difference between I_{DD_INT} current measurements obtained empirically on the ADSP-SC596/SC598 SHARC+ processors evaluation platform. The difference is measured before and after enabling the indicated DMA activity.

Estimating Accelerator Contribution to Internal Dynamic Current ($I_{DD\_INT\_ACCL\_DYN}$)

The high-performance system accelerators (FIR and IIR) consume some current in the V_{DD_INT} domain. The total accelerator current is defined as the sum of the current consumed by each of the blocks.

$$I_{DD\_INT\_ACCL\_DYN} = I_{DD\_INT\_ACCL\_FIR0\_DYN} + I_{DD\_INT\_ACCL\_FIR1\_DYN} + I_{DD\_INT\_ACCL\_IIR0\_DYN} + I_{DD\_INT\_ACCL\_IIR1\_DYN} + I_{DD\_INT\_ACCL\_IIR2\_DYN} + I_{DD\_INT\_ACCL\_IIR3\_DYN} + I_{DD\_INT\_ACCL\_IIR4\_DYN} + I_{DD\_INT\_ACCL\_IIR5\_DYN} + I_{DD\_INT\_ACCL\_IIR6\_DYN} + I_{DD\_INT\_ACCL\_IIR7\_DYN.}$$

For a peak FIR use case, the $I_{DD\_INT\_ACCL\_FIR\_DYN}$ current is 330 mA. For a typical IIR use case, the $I_{DD\_INT\_ACCL\_IIR\_DYN}$ current is 80 mA.

Estimating Total Static Current ($I_{DD\_INT\_STATIC}$)

The static current ($I_{DD\_INT\_STATIC}$) dissipated across the entire device in the V_{DD_INT} power domain results from transistor leakage. It is present when power is applied to the power domains, even when all the internal clocks are shut off (by gating/cutting the SYS_CLKIN to the ADSP-SC596/SC598 SHARC+ processor) and the device is held in reset. Alone, static current is solely a function of junction temperature (T_J) and voltage (V_{DD_INT}). Unlike dynamic current, it does not need to be adjusted for discrete core activity levels. $I_{DD\_INT\_STATIC}$ can be obtained by finding the value corresponding to the application conditions (such as at a specific V_{DD_INT} and T_J) in the *Static Current* table of the *ADSP-SC596/SC598: SHARC+ Dual-Core DSP with Arm Cortex-A55 Data Sheet*[1].

The $I_{DD\_INT\_STATIC}$ specifications in the *Static Current* table in the data sheet are maximum specifications that account for the wafer fabrication process.

Because the static power component is constant for a given voltage and temperature, it is added to the total estimated dynamic current when calculating the total power consumption due to the processor core logic. When a customer develops power supply and thermal relief designs, ensure that the highest expected junction temperature and voltage is used when extracting data from the *Static Current* table of the data sheet.

Estimating External Power Consumption

External power consumption consists of P_{DD_EXT}, P_{DD_REF}, and P_{DD_DMC}.

Total external power consumption ($P_{DD\_EXT\_TOT}$, dissipated in the V_{DD_EXT} and V_{DD_DMC} power domains) depends on these parameters:

- O–number of output pins associated with the interface
- TR–toggle ratio (percentage of pins that switch for any given cycle)
- f–maximum frequency at which the output pins can switch
- V_{DD_EXT} or V_{DD_DMC}–voltage swing of the output pins
- C_L–load capacitance of the output pins
- U–utilization factor (percentage of time for which peripheral is on and running)

In addition to the input capacitance of each device connected to an output, the total capacitance (C_L) must include the capacitance of the processor pin (C_{OUT}), which is driving the load.

The worst-case external pin power scenario occurs when the load capacitor charges and discharges continuously. This requires the pin to toggle in each cycle in terms of external power supply, over the maximum V_{DD_EXT} voltage swing (as specified in the data sheet). The maximum switching frequency *(f)* of a peripheral clock is twice the maximum toggling frequency (*f/2*) because the data pin state can change only once per clock cycle. When considering the full current profile for the V_{DD_EXT} power domain, there are several peripherals that can contribute to it. Each peripheral must be considered separately and then added together to form the single I_{DD_EXT} component of the total estimated power dissipation.

Equation 2 calculates the average external current (I_{DD_EXT}) using the previous parameters:

Equation 2 Total External Current (I_{DD_EXT}) Calculation

$$I_{DD\_EXT} = O \times f \times V_{DD\_EXT} \times C_L \times U \times TR$$

Estimated average external power consumption (P_{DD_EXT}) can then be calculated as:

$$P_{DD\_EXT} = V_{DD\_EXT} \times I_{DD\_EXT}$$

Substituting from Equation 2, this calculation yields:

$$P_{DD\_EXT} = V_{DD\_EXT}^2 \times O \times f \times C_L \times U \times TR$$

Table 2: VDD_EXT Power Consumption Example on page 11 is an excerpt from the example application use case in the *V_{DD_EXT} Power Domain* tab of the ADSP-SC596-SC598 Power Calculator Tool Rev00. It shows the Link Port interface portion to clearly illustrate the concept.

Table 2: V_{DD_EXT} Power Consumption Example

Peripheral	**Frequency in Hz (f)**	**Number of Output Pins (O)**	
Link Port - Data pins	6.25 E+07	8	
Pin Capacitance in Farads (CL)	**Toggle Ratio (TR)**	**Utilization Factor(U)**	**VDD_REF current per IO (mA)**
3.00E-11	0.25	1.00	0.8
VDD_EXT (V)	**VDD_REF (V)**	**PDD_EXT (mow)**	**PDD_REF (mW)**
3.30	1.80	40.838	11.520
Notes			
62.5 MHz max frequency cycle, 8-bit data (8 pins at 0.25 toggle ratio)			

When estimating the I_{DD_EXT} current, the I_{DD_DMC} current consumption for the on-chip DDR3 controller (DMC0) can be estimated, depending on the number of pins toggling and the toggle rate. V_{DD_DMC} is used for the voltage swing (obtain the maximum V_{DD_DMC} specification from the data sheet). The *V_{DD_DMC} Power Domain* tab in the ADSP-SC596-SC598 Power Calculator Tool Rev00 includes a table like the one referenced by Table 2. The DDR pins are grouped by function (for example, address, data, control, and clock) to help the user to customize their application.

Estimating I/O Reference Power Consumption (P_{DD_REF})

The I/O reference supply power consumption (P_{DD_REF}) depends on the frequency of I/O switching as depicted in Table 3.

Table 3: V_{DD_REF} current per I/O

Frequency of I/O switching (MHz)	**V_{DD_REF} current per I/O (mA)**
32 MHz or less	0.4 mA
33 MHz through 62.5 MHz	0.8 mA
63 MHz through 125 MHz	1.1 mA

The additional contribution for the V_{DD_REF} current results from the internal oscillator (10 mA), One Time Programmable Memory Controller (OTPC = 18 mA), and the Media Local Bus (MLB = 20 mA), which can used as is for calculation purposes.

General Guidelines for Power Supply and Thermal Relief Designs

While estimating average total power associated with a given application, power supply and thermal relief designs must always consider the worst-case scenario to prevent operational failures. Failures can happen with the processor operating out-of-spec because of a sagging power rail or an out-of-bounds junction temperature. The following sections provide specific recommendations when using this methodology.

Power Supply Sizing Recommendations

Use the following recommendations when estimating the power supply sizing.

Do:

- Use the maximum expected voltages associated with all the influencing power domains involved in each of the look-up tables and computations discussed throughout this EE note.

Power supply should be designed to remain tuned to nominal voltages throughout its lifetime.

- Use the junction temperature associated with the maximum ambient temperature (T_A) expected for this application, for all temperature-related lookups, and computations discussed throughout this EE note
- Use the highest ASF (Activity Scaling Factor) possible for the running application
- Separately calculate the power dissipation from each unique voltage domain

Do Not:

- Use typical I_{DD}, nominal voltage, or room temperature specifications.
- Use the total device power alone.

Thermal Relief Recommendations

Use the following recommendations when evaluating thermal relief solutions.

Do:

- Use nominal voltages.

Power supply should be designed to remain tuned to nominal voltages throughout its lifetime

- Use the junction temperature (Tj) that the processor is expected to be subjected to.
- Use the Full-on-Typical (or lower) ASF (Activity Scaling Factor) to match realistic application code activity levels.
- Calculate total thermal power for all voltage domains.

Do Not:

- Use the typical I_{DD} specifications or room temperature when calculating thermal power.
- Use maximum voltage. (This is not realistic, as any transient exceeds the maximum voltage specification.)

Example Application Using the Power Calculator

This section provides an example application to illustrate how to use the ADSP-SC596-SC598 Power Calculator Tool Rev00. There are three dialog tabs in the power calculator software that contain color-coded cells, plus the guidance to populate the yellow cells with the needed system settings. The software directs the calculator to automatically populate the green cells with data from other spreadsheet tabs or with a calculated result based on user inputs. Some of the yellow cells are free form, whereas others are selectable using a drop-down selection arrow. The following sections describe what user input is required on each power calculator tab to calculate the overall power dissipation estimate.

Power Estimation Tab

The *Power Estimation* tab for ADSP-SC596-SC598 Power Calculator Tool Rev00 is the main interface, where input is supplied to properly model the intended system. On this tab, the user must provide all the information for the system power supplies and clock rates. User also supplies other components that influence the overall power dissipation discussed in this EE note (for example, core activity and DMA rates). This tab works with other spreadsheet tabs to calculate the total power dissipation for the application, based on all the configurable system-dependent parameters.

The example application values used in this EE note derives its values from the default *Power Estimation* tab.

The default *Power Estimation* tab is pre-filled with data in the following list:

- Junction temperature at 125°C, to capture data at a worst-case temperature
- SHARC+ cores and A55 core running at 1 GHz and 1.2 GHz, with all other clocks at their maximum supported speeds
- A typical load profile of 70-30 considered for SHARC0 and SHARC1 (executes floating-point multiplication, addition, subtraction, and store instructions 70% of the time and 30% NOPs)
- ARM A55 performs peak operation 75% of the time and 25% IDLE)
- All instances of FIR and IIR accelerators infuse at 50% on time.
- DDR in use
- DMA bandwidth considered HIGH
- Link Port, 8xSPORT, and 3xSPI are considered the peripherals using and actively consuming I/O power.

Users can simulate any use case or application by modifying the default settings and configurations.

Set the Power Domains and Junction Temperature

Begin by setting the power domains and junction temperature to the maximum levels expected by the application. For example, consider a design with the measurements:

- V_{DD_INT} = 1.0 V
- V_{DD_EXT} = 3.3 V
- V_{DD_REF} = 1.8 V
- V_{DD_DMC} = 1.39 V
- T_J =125°C

The V_{DD_INT} domain and T_J values are used as inputs to look-up tables on other power calculator tabs to extract the needed current dissipation data for a calculation. Select the values using the drop-down selection lists in the *Operating Conditions* table on the *Power Estimation* tab. Make the selections based on the discrete levels defined in the *Static* and *Dynamic Current* tables of the *ADSP-SC596/SC598: SHARC+ Dual-Core DSP with Arm Cortex-A55 Data Sheet*.

The *Static* and *Dynamic Current* tables included in the power calculator are from the referenced processor data sheet. Always verify that the data in the calculator matches with the data in the current data sheet to ensure that the proper specifications are included.

Configure the other relevant power domains on the *Power Estimation* tab. Manually input the appropriate values for the V_{DD_EXT} (in the *V_{DD_EXT}* section), V_{DD_REF} (in the *V_{DD_REF}* section) and V_{DD_DMC} (in the *V_{DD_DMC}* section) domains into the relevant yellow cells. The calculator computes the current and/or power in the associated green cells.

There is no error-checking built into the calculator for the range of these power domains. A *Configuration Warning* is associated with each of these yellow cells indicating that the input values must be verified by referring to the processor data sheet.

The V_{DD_EXT}, V_{DD_REF}, and V_{DD_DMC} cells are influenced by activity on the *V_{DD_EXT} & V_{DD_REF} Power* and *V_{DD_DMC} Power* tabs, respectively.

Set the Clocks

Input all the clock information that defines the dynamic currents expected throughout the system. For example, consider a design that uses the following values:

- f_{CCLK_SHARC0} = 1000 MHz
- f_{CCLK_SHARC1} = 1000 MHz
- f_{CCLK_A55} = 1200 MHz
- f_{DCLK} = 900 MHz
- f_{SYSCLK} = 500 MHz
- f_{SCLK0} = 125 MHz
- f_{SCLK1} = 333 MHz
- f_{OCLK} = 125 MHz

Input the values into the corresponding yellow cells of the *Clock Domains & DMA Rates* table. The calculator computes the associated dynamic current in the adjacent green cells.

There is no error-checking built into the calculator for the range of these operating frequencies. A *Configuration Warning* is associated with each of these yellow cells indicating that the input values input must be verified by referring to the processor data sheet.

Set the Activity Scaling Factors (ASFs)

As discussed in Using ASFs to Establish Application-Specific Total Average Power Profile on page 5, analyze the application and determine the core loads to associate with the application. This step establishes the dynamic power dissipation component for each core that is handled in the yellow cells in the *COREx Average ASF* tables in the V_{DD_INT} section of the *Power Estimation* tab. The proper cell value is a fractional number that ranges from 0.0 through 1.0. This indicates the percentage of time spent by the application at that discrete ASF level. The calculator outputs the *Average ASF* (as described by Equation 1 on page 5) in the green cell based on the data on the *Core Activity Factors* tab.

There is no error-checking built into the calculator for the sum of these percentages. A hover message indicating that the "*Sum of these fractions should be 1"* displays, to advise the user when inputting data in this section.

The *ASF* tables included in the power calculator are from the referenced processor data sheet. Always verify that the data in the calculator matches the data in the current data sheet to ensure that the proper specifications are included.

A power supply design should use a maximum power dissipation profile that accounts for the worst-case scenario. However, to establish an average power profile, the calculator is built to account for all the discrete ASF levels defined by ADSP-SC596/SC598: SHARC+ Dual-Core DSP with Arm Cortex-A55 Data Sheet. The yellow cells can be populated to reflect the actual system model.

For example, after analyzing the application, it is determined that the following describes the core activity levels:

- SHARC+ Core1–100% typical application (70-30 profile)
- SHARC+ Core2–100% typical application (70-30 profile)
- ARM A55 Core0–100% typical application (75-25 profile)

While providing input to the calculator, the corresponding average ASFs are defined as:

- ASF_{SHARC1} =1.00
- ASF_{SHARC1} =1.00
- ASF_{A55} =1.00

The ASF is used by the calculator to compute the dynamic current in the green cells in the *Contribution (mA)* column, plus the *Clock Domains & DMA Rates* table.

Set the Accelerator Resource Usage

The system accelerator engines (FIR, IIR) dissipate dynamic power in the V_{DD_INT} domain. This is as part of the total internal dynamic current ($I_{DD\_INT\_TOT}$) equation in the 'Total internal power dissipation' section of processor data sheet. This power is mentioned in the *V_{DD_INT}* section of the *Power Estimation* tab in a series of yellow cells in the *Resource Usage* table. These yellow cells should be written with the percentage of time for which each instance of FIR or IIR is active. Fifty percent (50%) active time is the default. The selectable mode options for each row insert a look-up value into the associated tables on *V_{DD_INT} Accelerators* of the calculator.

Only the *Peak usage* setting is available, as discussed in Estimating Accelerator Contribution to Internal Dynamic Current (IDD_INT_ACCL_DYN) on page 9.

For example, when all instances of FIR and IIR (at 50% active time) are being used, then

$$I_{DD\_INT\_ACCL\_DYN} = 165\ mA + 165\ mA + 80\ mA + 80\ mA + 80\ mA + 80mA + 80mA + 80\ mA + 80mA + 80mA = 970mA.$$

Select Appropriate DMA Activity Level

The final user input required on the *Power Estimation* tab is the *DMA/Peripheral Usage* row in the *Clock Domains & DMA Rates* table in the *V_{DD_INT}* section. Here that the user must select from the three defined profiles discussed in Estimating Accelerator Contribution to Internal Dynamic Current (IDD_INT_ACCL_DYN) on page 9 (HIGH, MEDIUM, or LOW) as the closest match to the system data activity. When selected using the yellow drop-down selection, the corresponding look-up value from the $I_{DD\_INT\_DMA\_DR\_DYN}$ column on the *V_{DD_INT} DMA Usage* tab populates the corresponding green cell in the *Contribution (mA)* column.

When considering serial peripherals, with DDR access and additional MDMA, select a HIGH profile (4695 MBPS).

The value for DMA contribution is $I_{DD\_INT\_DMA\_DR\_DYN}$ = 220 mA

V_{DD_EXT} & V_{DD_REF} Power Domain Tab

The *V_{DD_EXT} & V_{DD_REF} Power Domain* tab is used to calculate the contribution to power from the Link Ports, SPORTs, and SPI peripherals.

Calculating V_{DD_EXT} Power

Using the *V_{DD_EXT} & V_{DD_REF} Power Domain* tab, identify:

- Each V_{DD_EXT} power domain peripheral that is in use in the system, modelling its power profile as a function of how often it is active
- How many pins switch
- The load capacitance associated with the pins
- The voltage swing on the pins
- The frequency at which the pins can switch

Like the *Power Estimation* tab, the yellow cells require user input, and the green cells are populated by the calculator.The *V_{DD_EXT}* column is automatically populated from the *Power Estimation* tab. The user must fill in the yellow cells. Consider an application that uses the Link Port, eight serial ports (SPORTs), and three SPIs. For a rough estimation, consider external frame syncs for SPORTs and low target selects for SPIs. Most of the columns populate with the appropriate clock frequencies. However, some frequency area functions depend on the peripheral configuration. The configuration includes the pin capacitance from the design, the application's use of the peripheral (see Estimating External Power Consumption on page 10), the *Number of Output* pins, and the *Utilization Factor*.

With the following peripheral configuration information, Table 4: Example VDD_EXT Peripheral Usage on page 18, would represent such a system, once the user:

- Inputs the proper number of output pins (O)
- Makes a reasonable guess of the number of pins switching in any given cycle (TR)
- Populates the frequency (*f*) and load capacitance (C_L)
- Supplies information about the percentage of the time the peripheral is enabled (U)

The *P_{DD_EXT} (mW)* column contains the results of the calculator applying Equation 2 Total External Current (IDD_EXT) Calculation on page 10 to the input data in the other columns. The sum of the power contributions from each of the individual peripheral components is calculated at the bottom of the column. Peripherals can be added or deleted from this profile by inserting or removing rows.

Table 4: Example V_{DD_EXT} Peripheral Usage

Peripheral	Frequency in Hz (f)	Number of Output Pins (O)	Pin Capacitance in Farads (cL)	Toggle Ratio (TR)	Utilization Factor (U)	VDD_REF current per IO (mA)	V_{DD_EXT} (V)	V_{DD_REF} (V)	P_{DD_EXT} (mW)	P_{DD_REF} (mW)	Notes
Link Port Data pins	6.25E+07	8	3.00E-11	0.25	1.00	0.8	3.30	1.80	40.838	11.520	62.5 MHz max frequency cycle, 8-bit data (8 pins at 0.25 toggle ratio)
Link Port - Clock	1.25E+08	1	3.00E-11	1	1.00	1.1	3.30	1.80	40.838	1.980	125Mhz operation
SPORT0-7 -Data pins	3.13E+07	16	3.00E-11	0.25	1.00	0.4	3.30	1.80	40.838	11.520	31.25 MHz max frequency cycle, 2 pins per SPORT x 8 (16 pins at 0.25 toggle ratio)
SPORT0-7 - Clock	6.25E+07	8	3.00E-11	1	1.00	0.8	3.30	1.80	163.350	11.520	62.5Mhz operation
SPI2 Data pins	3.13E+07	4	3.00E-11	0.25	1.00	0.4	3.30	1.80	10.209	2.880	31.25 MHz max frequency cycle, Quad mode (4 pins at 0.25 toggle ratio)
SPI2 - Clock	6.25E+07	1	3.00E-11	1	1.00	0.8	3.30	1.80	20.419	1.440	62.5 MHz operation
SPI1 - Data pins	3.13E+07	4	3.00E-11	0.25	1.00	0.4	3.30	1.80	10.209	2.880	31.25 MHz max frequency cycle, Quad mode (4 pins at 0.25 toggle ratio)
SPI1- Clock	6.25E+07	1	3.00E-11	1	1.00	0.8	3.30	1.80	20.419	1.440	62.5 MHz operation
SPI10- Data pins	3.13E+07	2	3.00E-11	0.25	1.00	0.4	3.30	1.80	5.105	1.440	31.25 MHz max frequency cycle, Dual mode (2 pins at 0.25 toggle ratio)
SPI0- Clock	6.25E+07	1	3.00E-11	1	1.00	0.8	3.30	1.80	20.419	1.440	62.5 MHz operation
						Total External Power Dissipation (mW)			**372.64**		
						Total VREF Dissipation (mW)			**89.460**		

Calculating V_{DD_REF} Power

The V_{DD_REF} power is automatically calculated in the same spreadsheet as V_{DD_EXT} power, since both are related to I/O switching of peripherals. The calculation is done by referring to Table 5 for each I/O pin.

Table 5: I/O V_{REF} Current for P_{DD_REF} Calculation

Frequency of I/O switching (MHz)	V_{DD_REF} current per IO (mA)
32 MHz or less	0.4 mA
33 MHz through 62.5 MHz	0.8 mA
63 MHz through 125 MHz	1.1 mA

V_{DD_DMC} Power Domain Tab

The *V_{DD_DMC} Power Domain* tab must be used when using DDR in the application. The concepts from VDD_EXT & VDD_REF Power Domain Tab on page 17 also apply to this tab. However, the table is slightly different because it is modeling a single interface that has numerous groups of pins that need to be treated differently, based on factors that do not remain consistent across the interface. Like the *V_{DD_EXT} Power Domain* tab, the green cells are populated by the calculator or are the output of a computation. The user must populate the yellow cells with information regarding the configuration of the DDR controller.

For the green cells on the *V_{DD_DMC} Power Domain* tab, the power supply information for the *V_{DD_DMC} (V)* column and the *Frequency in Hz (f)* column is obtained from the *Power Estimation* tab. The calculator automatically applies the f_{DCLK} rate to the clock (*CLK*) and *Address pins [15:0]* rows, as these pins can switch at this rate in a worst-case scenario.

As indicated in the Set the Clocks section on page 15, the DDR clock was configured to 900 MHz on the *Power Estimation* tab. Table 6: Example VDD_DMC Use Case on page 20 is an example model for the application DDR interface, after the user finalizes the pin capacitance and other inputs.

Because typical DDR accesses are sequential in nature, it is unlikely that the number of address pins toggling at any maximum frequency cycle will exceed 25% (four pins). The worst-case model assumes the interface is always running (U = 1.00). For average power dissipation, there can be low-power modes employed, This makes a fractional *Utilization Factor* possible, which is also supported by the calculator software.

Table 6: Example V_{DD_DMC} Use Case

Peripheral		Frequency in Hz (f)	Number of Output Pins (O)	Pin Capacitance in Farads (C_L)	Toggle Ratio (TR)	Utilization (U)	V_{DDR} (V)	Pout (mW)	Reasoning
DDR3L	Address pins [15:0]	4.50E+08	16	5.00E-12	0.25	1.00	1.39	17.39	DCLK_FREQ operation; Worst case execution --> State of pin changes roughly every one fourth max frequency cycle (toggle ratio: 0.5)
	Data pins [15:0]	9.00E+08	16	5.00E-12	1	1.00	1.39	139.11	2x DCLK_FREQ operation, Assume DDR configured for write operation; Worst case execution --> State of pin changes twice every clock cycle (toggle ratio:1)
	CTRL	9.00E+08	15	5.00E-12	0.25	1.00	1.39	16.30	DCLK_FREQ/Burst Mode operation, Assume DDR configured for write operation; Worst case execution --> State of pin changes roughly every one fourth max frequency cycle (toggle ratio:0.25)
	CLK	9.00E+08	2	5.00E-12	1	1.00	1.39	17.39	DCLK_FREQ operation; Clk and the differential clock signal ; Worst case execution --> State of pin changes twice every clock cycle (toggle ratio:1)

Procedure for Estimating Total Power

Use the following major steps to estimate total overall power in an ADSP-SC596/SC598 SHARC+ processor design:

1. Step 1–Obtain the Internal Static Current Component (IDD_INT_STATIC)
2. Step 2–Obtain Baseline Core Dynamic Currents
3. Step 3–Model Application to Establish Activity Scale Factors (ASFSHARC0)
4. Step 4-Apply ASFs to Core Dynamic Components
5. Step 5-Calculate the System Clock Tree Core Dynamic Currents
6. Step 6-Choose a DMA Profile to Obtain Core Dynamic DMA Current (IDD_INT_DMA_DR_DYN)
7. Step 7-Account for Core Dynamic Currents from Accelerator Blocks (IDD_INT_ACCL_DYN)
8. Step 8-Calculate Total Internal Power Dissipation (PDD_INT_TOT)
9. Step 9-Calculate External Power Dissipation (PDD_EXT_TOT)
10. Step 10-Calculate Total Power Dissipation (PDD_TOT)

Step 1–Obtain the Internal Static Current Component ($I_{DD\_INT\_STATIC}$)

Use the maximum power rail (V_{DD_INT}) and the junction temperature (T_J) values to obtain the maximum $I_{DD\_INT\_STATIC}$ specification from the *Static Current* table described in the processor data sheet. The example discussed in the Set the Power Domains and Junction Temperature section on page 14 where:

- V_{DD_INT} = 1.0 V and T_J = 125°C, yields
- *V_{DD_INT} Maximum Static Current* tab is 3523 mA.

Step 2–Obtain Baseline Core Dynamic Currents

The baseline core dynamic currents are $I_{DD\_INT\_CCLK\_A55\_DYN}$, $I_{DD\_INT\_CCLK\_SHARC1\_DYN}$, and $I_{DD\_INT\_CCLK\_SHARC2\_DYN}$. Use the V_{DD_INT} power rail and the expected core clock frequency (f_{CCLK}) to obtain the values for each core in the *Dynamic Current* tables of the processor data sheet. For the example discussed in the Set the Clocks section on page 15, V_{DD_INT} = 1.0 V and the core is running at 1000 MHz. The equation values in the Core Dynamic Current on page 3 and in the *Dynamic Current* data sheet table are:

- $I_{DD\_INT\_CCLK\_SHARCx\_DYN}$= 0.714 x V_{DD_INT} **x** f_{CCLK_SHARCx} →0.714 **x** 1.0 **x** 1000 = 714 mA
- $I_{DD\_INT\_CCLK\_A55\_DYN}$ = 0.468 **x** V_{DD_INT} x f_{CCLK_A55} →0.468 **x** 1.0 **x** 1200 = 561 mA

Step 3–Model Application to Establish Activity Scale Factors (ASF_{SHARC0})

Using the scale factor definitions found in the *Activity Scaling Factors* model tables of the processor data sheet, model each core's application to determine the processor load for the executed code. For a maximum calculation, use the worst-case ASF. Calculate an average ASF, as described in the Using ASFs to Establish Application-Specific Total Average Power Profile section on page 5. For the example provided in Set the Activity Scaling Factors (ASFs) section on page 15:

- ASF_{SHARC0}=1.00
- ASF_{SHARC1}=1.00
- ASF_{A55}=1.00

Step 4-Apply ASFs to Core Dynamic Components

Apply the calculated average ASF or the worst-case ASF to the core dynamic component for each core:

- $I_{DD\_INT\_CCLK\_SHARC0\_DYN}$ = $I_{DD\_INT\_CCLK\_SHARC0\_DYN}$ **x** ASF_{SHARC0} →714 **x** 1.00 = 714 mA
- $I_{DD\_INT\_CCLK\_SHARC1\_DYN}$ = $I_{DD\_INT\_CCLK\_SHARC1\_DYN}$ **x** ASF_{SHARC1} →714 **x** 1.00 = 714 mA
- $I_{DD\_INT\_CCLK\_A55\_DYN}$ = $I_{DD\_INT\_CCLK\_A55\_DYN}$ **x** ASF_{A55} →110 **x** 1.00 = 110 mA

Step 5-Calculate the System Clock Tree Core Dynamic Currents

The dynamic current dissipated in the V_{DD_INT} domain because of the clocks toggling inside the processor, are a function of the internal voltage (in Volts) and the frequency of each clock (in MHz), This is governed by the equations in the processor data sheet. Using the example from the Estimating System Clock Tree Currents section on page 6:

- $I_{DD\_INT\_DCLK\_DYN}$ = 0.097 **x** f_{DCLK} **x** V_{DD_INT} → 0.097 **x** 900 **x** 1.0 = 87.30 mA
- $I_{DD\_INT\_SYSCLK\_DYN}$ = 0.792 **x** f_{SYSCLK} **x** V_{DD_INT} → 0.792 **x** 500 x 1.0 = 396 mA
- $I_{DD\_INT\_SCLK0\_DYN}$ = 0.451 **x** f_{SCLK0} x V_{DD_INT} → 0.451 **x** 125 x 1.0 = 56.38 mA
- $I_{DD\_INT\_SCLK1\_DYN}$ = 0.014 **x** f_{SCLK1} **x** V_{DD_INT} → 0.014 **x** 333.3 **x** 1.0 = 4.67 mA
- $I_{DD\_INT\_OCLK\_DYN}$ = 0.108 **x** f_{OCLK} **x** V_{DD_INT} → 0.108 **x** 125 **x** 1.0 = 13.50 mA

Step 6-Choose a DMA Profile to Obtain Core Dynamic DMA Current ($I_{DD\_INT\_DMA\_DR\_DYN}$)

Calculate the total system DMA bandwidth during peak activity and select the profile that is the closest match. The example in Select Appropriate DMA Activity Level section on page 16 sets the DMA profile to **HIGH**:

- $I_{DD\_INT\_DMA\_DR\_DYN}$ =220 mA

Step 7-Account for Core Dynamic Currents from Accelerator Blocks ($I_{DD\_INT\_ACCL\_DYN}$)

Each of these blocks dissipates power in the V_{DD_INT} domain and must be considered when estimating the total core dynamic current. The example discussed in the Set the Accelerator Resource Usage section on page 16 has the system acceleration engine enabled:

- $I_{DD\_INT\_ACCL\_DYN}$ =650 mA

Step 8-Calculate Total Internal Power Dissipation ($P_{DD\_INT\_TOT}$)

Add the static internal current [Step 1–Obtain the Internal Static Current Component (IDD_INT_STATIC)] component to the sum of all the dynamic internal current components [Step 4-Apply ASFs to Core Dynamic Components through Step 7-Account for Core Dynamic Currents from Accelerator Blocks (IDD_INT_ACCL_DYN)] to get the total current in the V_{DD_INT} domain ($I_{DD\_INT\_TOT}$):

$$I_{DD\_INT\_TOT} = I_{DD\_INT\_STATIC} + I_{DD\_INT\_CCLK\_SHARC0\_DYN} + I_{DD\_INT\_CCLK\_SHARC1\_DYN} + I_{DD\_INT\_CCLK\_A55\_DYN} + I_{DD\_INT\_DCLK\_DYN} + I_{DD\_INT\_SYSCLK\_DYN} + I_{DD\_INT\_SCLK0\_DYN} + I_{DD\_INT\_SCLK1\_DYN} + I_{DD\_INT\_OCLK\_DYN} + I_{DD\_INT\_ACCL\_DYN} + I_{DD\_INT\_DMA\_DR\_DYN}$$

$$I_{DD\_INT\_TOT} = 3523.00 + 714.00 + 714.00 + 561.60 + 87.30 + 396.00 + 56.38 + 4.67 + 13.50 + 650.00 + 220 = 6940.45 \text{ mA}$$

With the total $I_{DD\_INT\_TOT}$ current calculated, estimate the total power ($P_{DD\_INT\_TOT}$):

$P_{DD\_INT\_TOT} = I_{DD\_INT\_TOT}$ **x** V_{DD_INT} →6940.45 mA **x** 1.0 V =6940.45 mW

Step 9-Calculate External Power Dissipation ($P_{DD\_EXT\_TOT}$)

The total external power dissipation ($P_{DD\_EXT\_TOT}$) is comprised of the power dissipated in each of the two critical power domains (V_{DD_EXT}, V_{DD_DMC}) and the V_{DD_REF} domain.

Calculate Power Dissipated in the V_{DD_EXT} and V_{DD_REF} Domain (P_{DD_EXT} & P_{DD_REF})

Model the application using the concepts discussed in Estimating External Power Consumption on page 10 to estimate the power dissipated in the V_{DD_EXT} domain (P_{DD_EXT}) and V_{DD_REF} domain (P_{DD_REF}). From the example discussed in the VDD_EXT & VDD_REF Power Domain Tab section on page 17:

- P_{DD_EXT} = 372.64 mW
- P_{DD_REF} = 89.460 mW

Calculate Power Dissipated in the V_{DD_DMC} Domain (P_{DD_DMC})

Model the application using the concepts discussed in Estimating External Power Consumption on page 10 to estimate the power dissipated in the V_{DD_DMC} domain (P_{DD_DMC}). From the example discussed in the VDD_EXT & VDD_REF Power Domain Tab section on page 17:

- P_{DD_DMC} = 190.19 mW

Step 10-Calculate Total Power Dissipation (P_{DD_TOT})

Once all the core and system elements are properly modelled, calculate the total power dissipation as the sum of the internal ($P_{DD\_INT\_TOT}$) and external ($P_{DD\_EXT\_TOT}$) power dissipation components:

$$P_{DD\_EXT\_TOT} = P_{DD\_EXT} + P_{DD\_REF} + P_{DD\_DMC}$$

- $P_{DD\_TOT} = P_{DD\_INT\_TOT} + P_{DD\_EXT\_TOT}$ → 6940.45 + 372.64 +89.46 + 190.19
  = 7593 mW or approximately 7.593 W

Because of the rounding in the calculations for this example, the values in the green cells of the user power calculator can differ slightly from those in the EE note.

References

[1] *ADSP-SC596/SC598: SHARC+ Dual-Core DSP with Arm Cortex-A55 Data Sheet (Rev. 0),* March 2023. Analog Devices, Inc.

[2] *ADSP-SC596-SC598 Power Calculator Tool Rev00*. Found in the associated file named *EE440_ADSP-SC596-SC598_Power_Calculator_Tool_Rev00.ZIP*, at the *Analog.com* website.

[3] *EE-414: Estimating Power for ADSP-2156x SHARC+ Processors Rev. 1*, March 2021. Analog Devices, Inc.

[4] *ADSP-SC596/SC598 SHARC+ Processor Hardware Reference*, August 2022. Analog Devices, Inc.

[5] *SHARC+ Core Programming Reference, Revision 1.4*, May 2021. Analog Devices, Inc.

[6] **Power Domains**–Power domains enable or disable power to a region of a system on chip (SoC) and can control the clock rate or amount of power supplied to that SoC region.

Document History

Revision	Description
Rev 1 – September 25, 2022 by Deepak Huchaiah	Initial Draft
Rev 1 – April 13, 2023	Final Published version of EE-440 Note
Rev 2 – July 10, 2023	Remove all references to the obsolete ADSP-SC595