Engineer-to-Engineer Note EE-438

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Boot Time Estimation for ADSP-SC598 SHARC+® Processors

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Introduction

A fast boot time creates the first impression to a customer about the device. For automotive infotainment applications, users are concerned about *Time to Audio* when booting applications. This EE-note guides users in accurately estimating the boot time for the ADSP-SC598 SHARC+ processors. This is useful in designing an application and defining the boot strategy to adopt to reduce the overall boot-up time.

The boot time in ADSP-SC595/SC596/SC598 SHARC+ processors depends on numerous factors, which include boot mode used, size of the loader stream, and types of blocks present within the loader stream. This EE-Note explains the impact of these factors and provides an estimate of boot time for ADSP-SC598 SHARC+ processors. ADI has documented the boot time comparison between previous products (ADSP-SC57x, ADSP-2156x, ADSP-2159x, and ADSP-SC594 families) to assist engineers in selecting the appropriate processor for their application boot time needs.

Take-aways

Boot time estimation helps a user to construct an optimized loader stream that gives a faster boot time. The EE-Note provides calculated linear equations for boot time estimation in different boot modes (varying with boot image size). The EE-Note also discusses how distinct factors affect total boot time and explains how to incorporate those factors for a more accurate estimation of boot time.

Use this EE-Note to design a multi-stage boot strategy. For example, a user wants to boot an application having a 2 MB loader stream in less than 50 ms time using the OSPI Quad DTR boot mode. In this case, the user can only achieve 23.4375 MHz OSPI Clock (With 750 MHz CCLK and 375 MHz SYSCLK) at power up. That means the 50 ms requirement cannot be met (as shown by the calculated equation in *Figure 9. OSPI Octal-STR Boot at 62.5 MHz*). In this situation, updating the CGU and Boot Command for 62.5 MHz OSPI clock with the correct RDCR value solves the problem. The user has the following different options:

- **Normal Boot with OTP**–Do the CGU initialization, Boot Command, and RDCR programming through OTP, while doing the DMC initialization using Initcode or a primary application using a multi-stage boot.
- **Normal Boot without OTP**–Initialize CGU and DMC, Boot Command, and RDCR programming using Initcode or a primary application using a multi-stage boot.
- **Secure Boot**–Program the CGU initialization, security keys, Boot Command, and RDCR using the OTP. Do the DMC initialization through a primary application using a multi-stage boot.

For situations where a multi-stage boot strategy must be adapted, one can minimize the size for the primary application using this guide to meet the total boot time requirement. Boot time estimation can be useful for an user to decide a complex multi-phase boot strategy; where they can choose the size of each boot stage to help meet their requirements and reduce the overall boot time.

This EE-Note Describes

Terms Used in This EE-Note

- ECDSA–Elliptical Curve Digital Signature Algorithm
- BLp–Boot Loader plaintext, Plaintext Format
- BLx–Boot Loader without key, Keyless Format
- BLw–Boot Loader wrapped, Wrapped Format
- STR–Single transfer rate
- DTR–Dual transfer rate
- GPIO–General-purpose input/output

Boot Time for ADSP-SC598 SHARC+ Processors

Total boot time for ADSP-SC595/SC596/SC598 SHARC+ processors includes the sum of processor pre-boot time and the boot time consumed spent loading the application (for a defined boot mode).

- Pre-boot time configures all system resources prior to executing the required boot operation.
- Application loading time depends on the nature of loader stream and the peripheral used for a particular boot mode.

Several factors affects the boot time in a processor. The size of the loader stream, presence of fill blocks, and init block inside the loader stream have the most impact on boot time duration. This EE-note explains how you can estimate the boot time accurately for a given loader stream by considering the impact of these factors.

Boot Time Estimation

Assume the pre-boot takes a fix duration under certain conditions, engineers can separately compute the application loading time (boot time) for any loader stream using the Boot ROM API. ADI has measured boot times with different sized loader streams in each boot mode. Using the data, linear equations were calculated for different boot modes supported in ADSP-SC595/SC596/SC598 SHARC+ processors using the maximum system frequency (1.2 GHz Cortex A55 CCLK, SHARC+ 1 GHz CCLK, and 500 MHz SYSCLK). It was determined that the boot time varies linearly with the size of the loader stream. Using

these graphs as shown in Figure 1, linear equations are calculated in the form of $y = ax + b$, where $\boldsymbol{x}$ is size of loader stream in KB and $\boldsymbol{y}$ is boot time in milliseconds. Using these equations, an engineer can estimate the boot time for any loader stream size.

The associated *EE438 Note Example_Codes.zip file* [5] has the boot application code `Application_Code` folder that toggles a GPIO pin during start up to measure boot time. Similarly, the example code `BootTimeMsmt_ROMAPI` folder has code to call the ROM API boot.

Hardware Setup Used

All EE-Note measurements used the EV-SC598-SOM-EZKIT and EV-SOMCRR-EZKIT evaluation kits.

ADSP-SC595/SC596/SC598 SHARC+ Processors support normal and secure boot. Secure boot supports integrity, authentication, and confidentiality in three formats for protecting the IP and data:

- Plaintext (BLp) format
- Wrapped (BLw) format
- Keyless (BLx) format

For more information on secure boot, see the *EE366: Secure Booting Guide for Blackfin+® and SHARC+® Processors* [2].

The following sections have the derived boot time linear equations for different boot modes that support the ADSP-SC598 SHARC+ processors.

SPI Flash Boot

The SPI Flash Boot (SYS_BMODE 1) mode supports booting from flash device using the SPI peripheral. In ADSP-SC595/SC596/SC598 SHARC+ processors, the SPI2 instance drives the default SPI boot, which supports single, dual, and quad STR modes. Table 1 shows the different BCODEs supported for the maximum SPI clock frequency for the IS25LP512M flash device, which is present on the EV-SC598-SOM-EZKIT.

Table 1: Supported BCODE Values for SPI Flash Boot

Boot Mode	Max SPI Clock	BCODE Value
Single STR	75 MHz	0x2
Dual STR	75 MHz	0x3, 0x5
Quad STR	75 MHz	0x4, 0x9

Different BCODEs support different I/O modes of different flash devices depending on number of dummy cycles needed for the flash. See the *SPI Master BCODE Configuration Lookup Table* in the *ADSP-SC59x/SC596/SC598 SHARC+® Processor Hardware Reference* [1] for all the details.

For this section, Figure 1 through Figure 4 display calculated linear boot time equations for all the SPI flash boot modes at 62.5 MHz SPI clock frequency, including normal boot and secure boot with ECDSA-256 authentication.

Figure 1: SPI Flash Normal Boot at 62.5 MHz

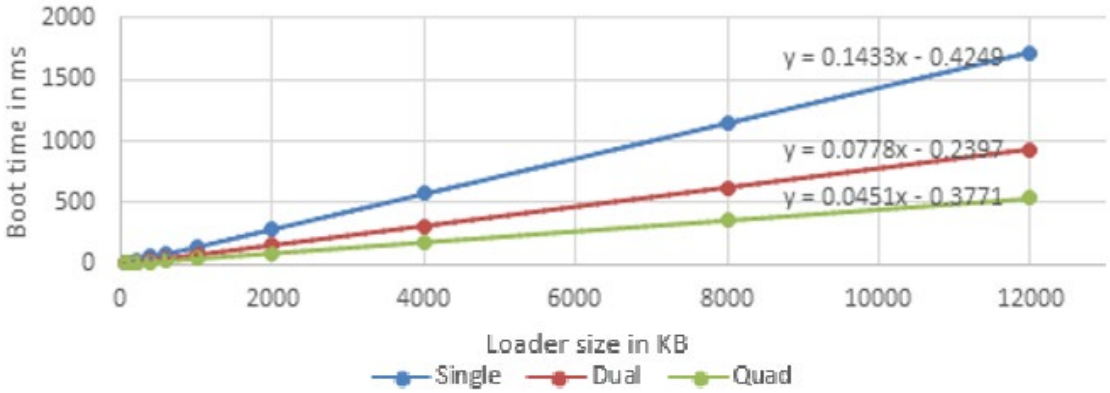


Figure 2: SPI2 Flash BLP Secure Boot at 62.5 MHz

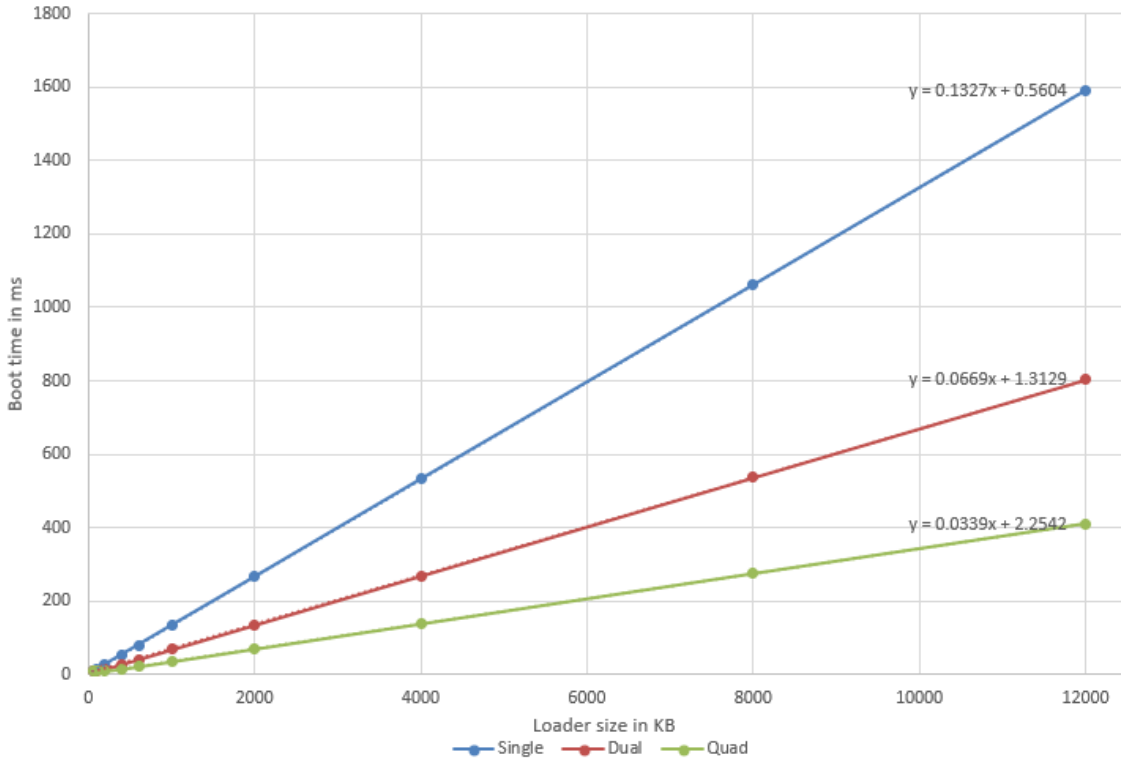


Figure 3: SPI Flash BLx Boot at 62.5 MHz

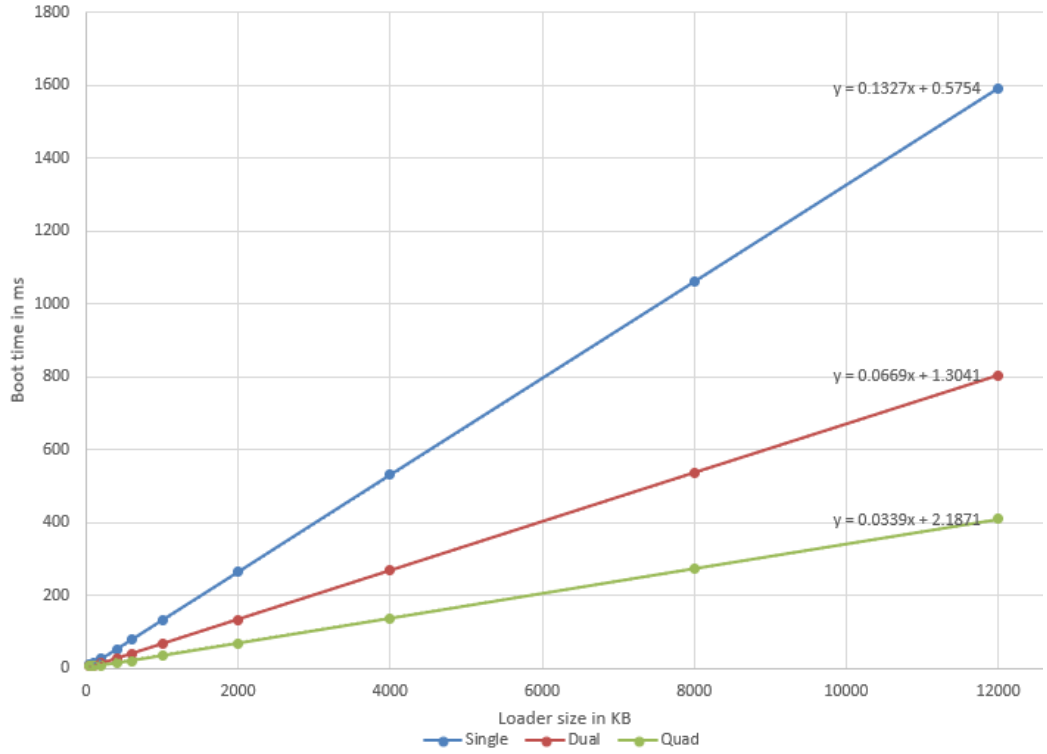
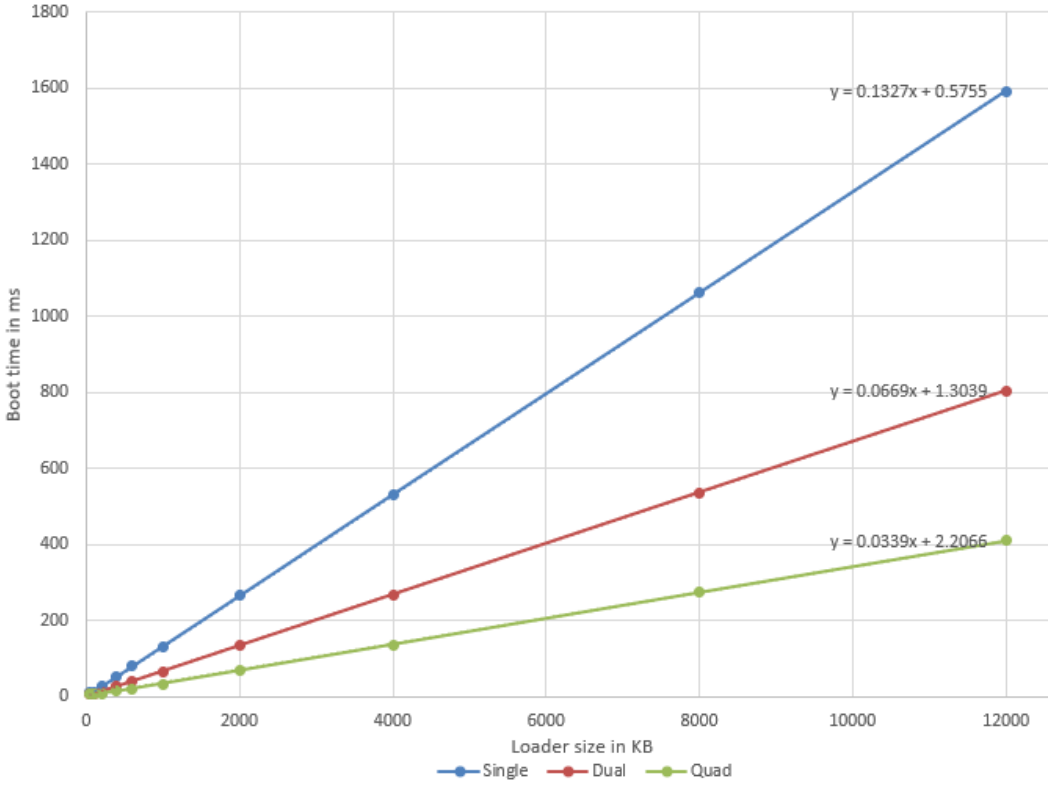


Figure 4: SPI2 Flash BLw Secure Boot at 62.5 MHz



Because of authentication and decryption routine actions done by the Crypto Engine in secure boot, a difference between normal and secure boot time happens.

The above numbers can be linearly extrapolated to a maximum 75 MHz SPI clock frequency, Table 2 shows the improved boot time estimate and measurement at the 75 MHz SPI clock frequency.

Table 2: Boot Times for Maximum SPI Clock Frequency

Condition with SPI Single STR boot	Boot Time
Estimated Boot time at 62.5 MHz	68.88 ms
Estimated Boot time after linear scaling at 75 MHz	57.4 ms
Measured boot time at 75 MHz	58.58 ms

Expect a small error margin involving a tradeoff in CCLK and SYSCLK frequencies while attaining 75 MHz SPI CLK. Users can measure the boot time at the default 43 MHz SPI frequency for a power-on reset and estimate the boot time at 62.5 MHz or 75 MHz from linear scaling.

OSPI Flash Boot

OSPI Flash Boot (SYS_BMODE 5) supports booting from the SPI flash or Octal flash using the OSPI peripheral, which includes the single-STR, dual-STR, quad-STR, single-DTR, dual-DTR, and quad-DTR modes. The OSPI flash boot supports a maximum 62.5 MHz OSPI clock frequency. The ADSP-SC598 family simultaneously supports two flash devices for booting, where SPI and OSPI signals reside on different port pins.

Table 3 shows the different BCODEs supported for the OSPI flash boot that uses maximum OSPI clock frequency with the IS25LP512M SPI flash device (EV-SC598-SOM-EZKIT).

Table 3: BCODE Values Supported for OSPI Flash Boot

Boot Mode	Max OSPI Clock	BCODE Value
Single STR	62.5 MHz	0x2
Dual STR	62.5 MHz	0x3
Quad STR	62.5 MHz	0x5
Single DTR	62.5 MHz	0x8
Dual DTR	62.5 MHz	0xA
Quad DTR	62.5 MHz	0xC

Figure 5 through Figure 8 show the different BCODEs supporting different I/O modes for different flash devices, depending on number of dummy cycles needed for the flash. See the *OSPI Master BCODE Configuration Lookup Table* in the *ADSP-SC59x/SC596/SC598 SHARC+® Processor Hardware Reference* [1] for details.

Figure 5: OSPI Normal Boot at 62.5 MHz

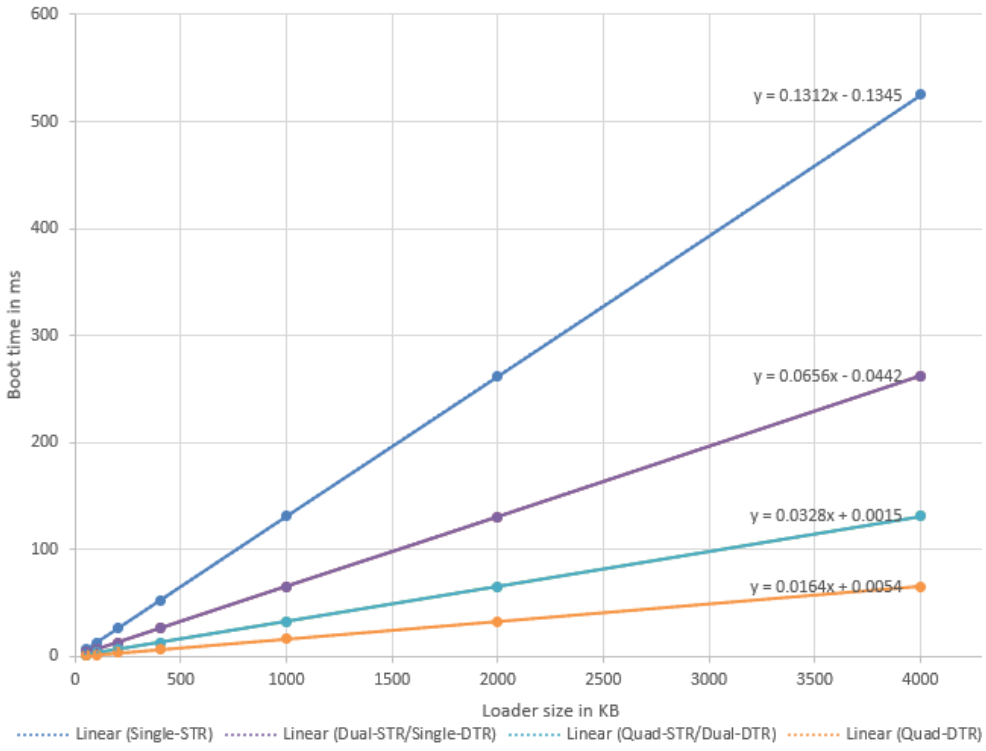


Figure 6: OSPI BLp Secure Boot at 62.5 MHz

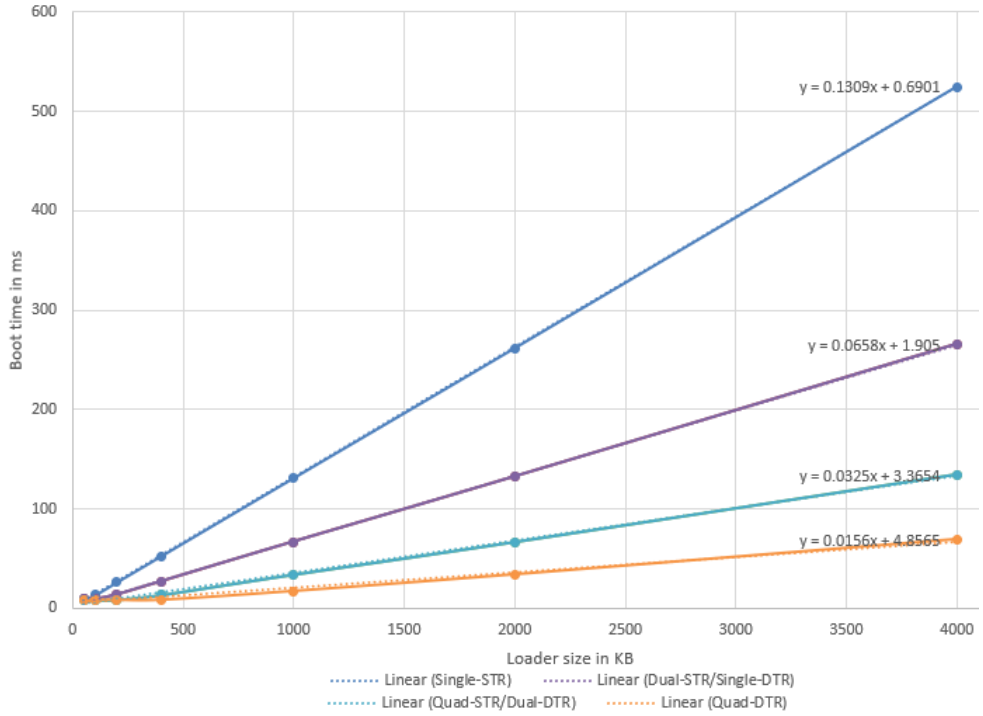


Figure 7: OSPI BLx Secure Boot at 62.5 MHz

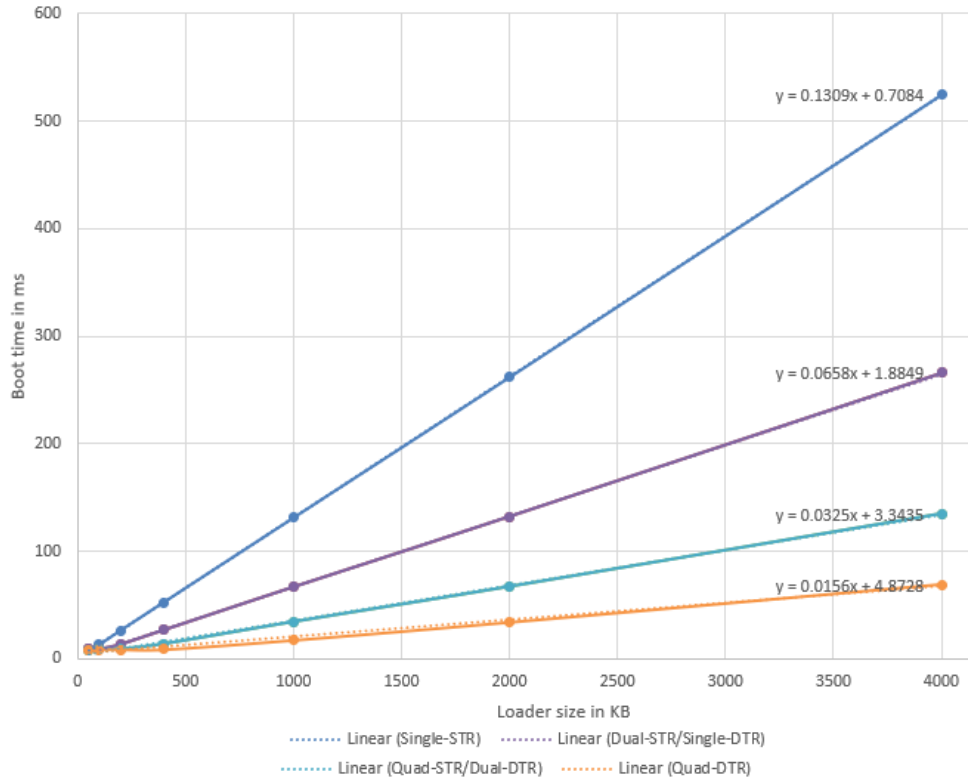
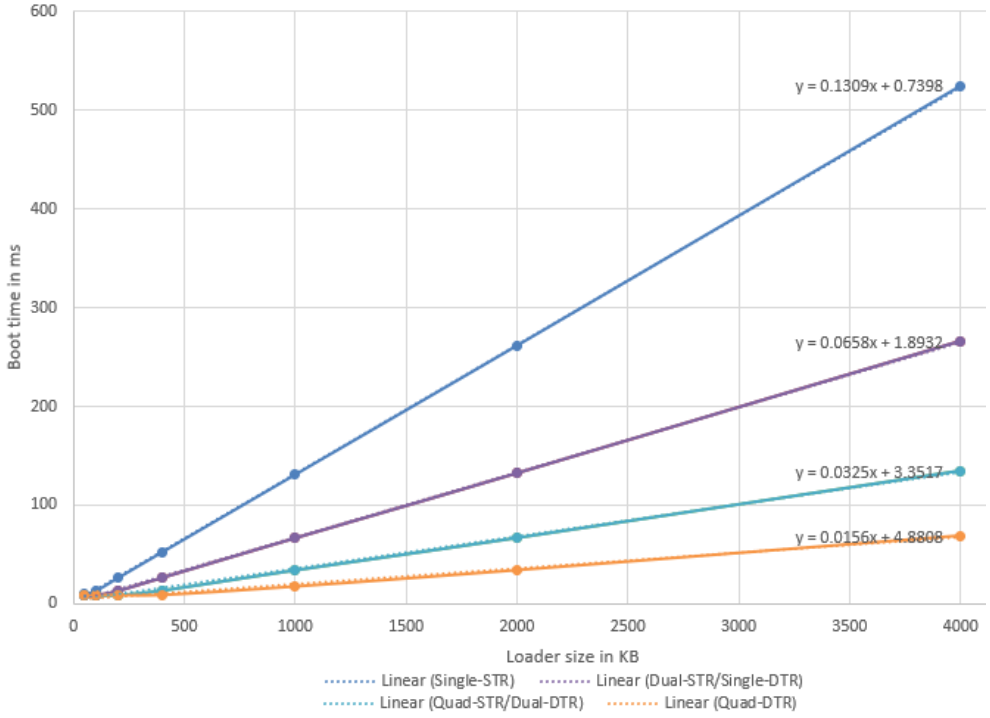


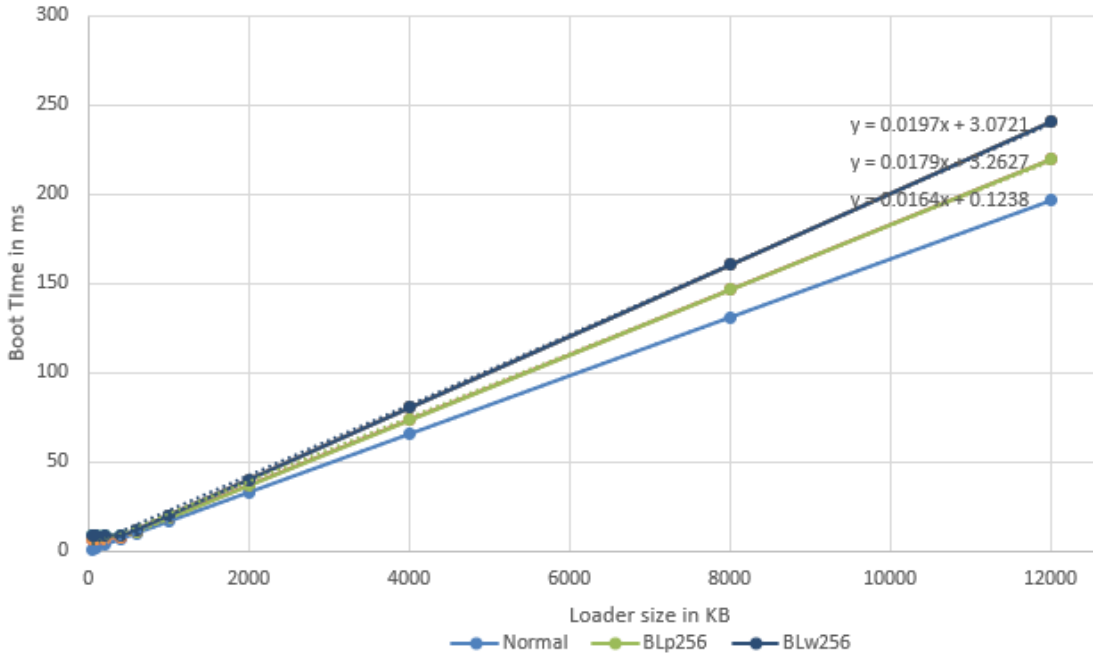
Figure 8: OSPI BLw Secure Boot at 62.5 MHz



The OSPI Controller for the ADSP-SC595/SC596/SC598 SHARC+ processors do not support Octal boot by default. Using a secondary stage boot, engineers can support an Octal boot, which further improves the boot time. Engineers achieve boot time improvement by using a custom boot implementation or a hook function. See the octal boot example code found in the `BootTimeMsmt_ROMAPI` folder of the *EE438 Note Example_Codes.zip file* [5].

Figure 9 shows the Octal-STR boot with normal and secure (BLp256 and BLw256 format) boot timings, It was measured with the MX66LM1G45GMI00 flash device (EV-SOMCRR-EZKIT).

Figure 9: OSPI Octal STR Boot at 62.5 MHz



eMMC Boot

The eMMC Boot (SYS_BMODE 6) supports booting from eMMC device through the eMSI peripheral that includes 1-bit SDR, 4-bit SDR, 8-bit SDR, 4-bit DDR, and 8-bit DDR modes. The eMMC boot supports a maximum of 50 MHz eMSI bus clock frequency. The ADSP-SC598 processor family only supports a single eMMC device. The eMMC device has two memory partitions, named the *User area partition* and *Boot area partition*. The ADSP-SC598 processor family supports an eMMC boot from both partitions. There are two ways a user can boot from User area partition, named *Default boot mode* and *Safe Boot mode*. For the Boot area partition a user can only boot in the *Default boot mode*.

The Default boot mode supports 1-bit SDR, 4-bit SDR, and 8-bit SDR modes (with tuning enabled as described in the *ADSP-SC595/SC596/SC598 Anomaly List* [6]). In this boot mode, a read command is only issued once for fetching the boot stream.

The Safe boot mode supports 1-bit SDR, 4-bit SDR, 8-bit SDR, 4-bit DDR, and 8-bit DDR modes. In this boot mode, a read command is issued each time to fetch 1 KB of boot stream data. The Safe boot mode latency exceeds the default boot mode time.

Different timing parameters involved with eMMC boot mode are useful in calculating the total boot time. See the parameter explanations in the following sections.

- eMMC Device Initialization Time (User Area Partition)
- eMMC Device Initialization Time (Boot Area Partition) on page 10
- NAC Timings on page 11

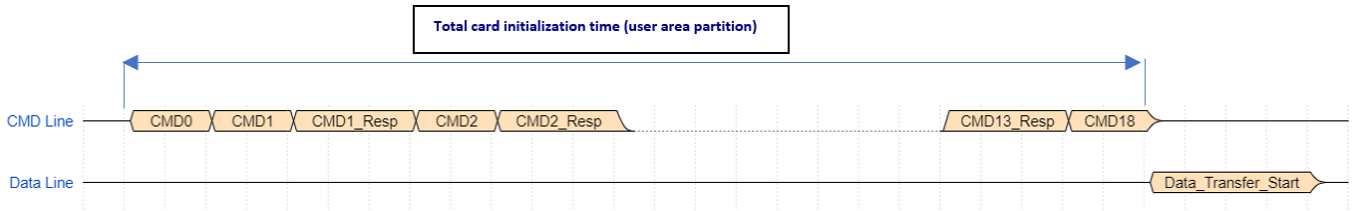
eMMC Device Initialization Time (User Area Partition)

To access the user area partition of the eMMC device, identification sequence must be carried out as a part of eMMC boot mode initialization. The time is added into data fetch time calculated from the graph (explained in later EE-Note sections). Because the initialization time (time required for sending each command and receiving response) varies for each eMMC device, it should be calculated separately (Equation 1 and Figure 10) for individual eMMC devices.

Equation 1: Total Card Initialization (User Area Partition)

Total card initialization time (User Area Partition) =
CMD0 + CMD1 (Till eMMC device is busy) + CMD1 response + CMD2 + CMD2 response + CMD3 + CMD3 response + CMD7 + CMD7 response + CMD6 + CMD6 response + CMD13 + CMD13 response + CMD 18

Figure 10: eMMC Initialization Time (User Area Partition)

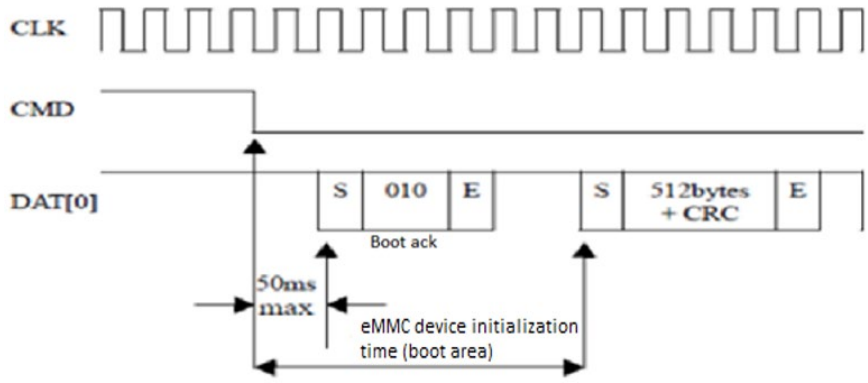


eMMC Device Initialization Time (Boot Area Partition)

To access the Boot area partition data using a mandatory boot process, there is some delay before eMMC device starts sending data. This time adds to the data fetch time calculated from graph (explained in later EE-Note sections). This initialization time (starting when the CMD line goes low to the start bit of first data block) varies for each eMMC device; therefore calculate it separately for each device.

See Figure 11 for details about the eMMC device initialization time (Boot area partition).

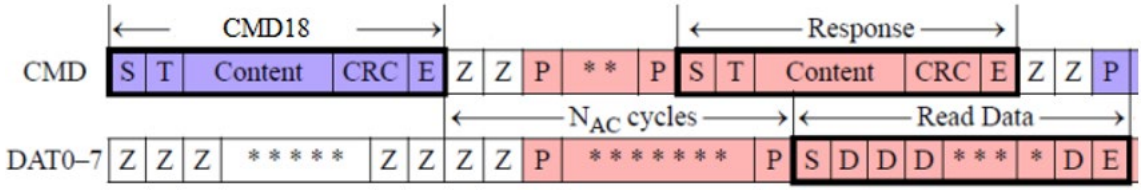
Figure 11: eMMC Initialization Time (Boot Area Partition)



NAC Timings

After issuing the multi-block read command (CMD18) to eMMC device to read data from the User area partition, the device sends the data (after a fixed access time delay), called NAC. The NAC calculation (Figure 12) is different for each eMMC device. Engineers should measure the value separately for each eMMC device.

Figure 12: NAC Data Response



Total Boot Timings Calculation

This section uses an example to describe how to calculate total boot time using equations for each eMMC boot mode. The example shows difference between the measured boot time and the calculated boot time.

User Area Partition

Figure 13 through Figure 16 shows linear equations for all the eMMC user area boot modes for data fetching at 50 MHz eMSI bus clock frequency, including normal boot and secure boot with ECDSA-256 authentication.

Figure 13: eMMC Normal Boot Data Fetch at 50 MHz (User Area Partition)

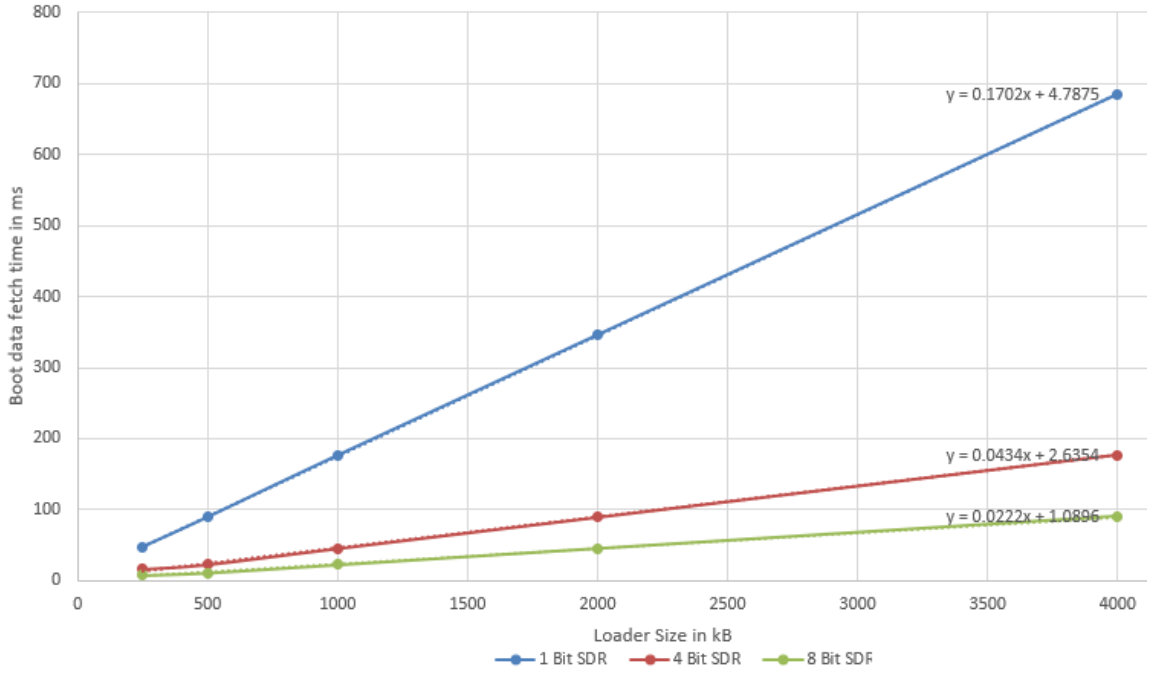


Figure 14: eMMC BLp Secure Boot Data Fetch at 50 MHz (User Area Partition)

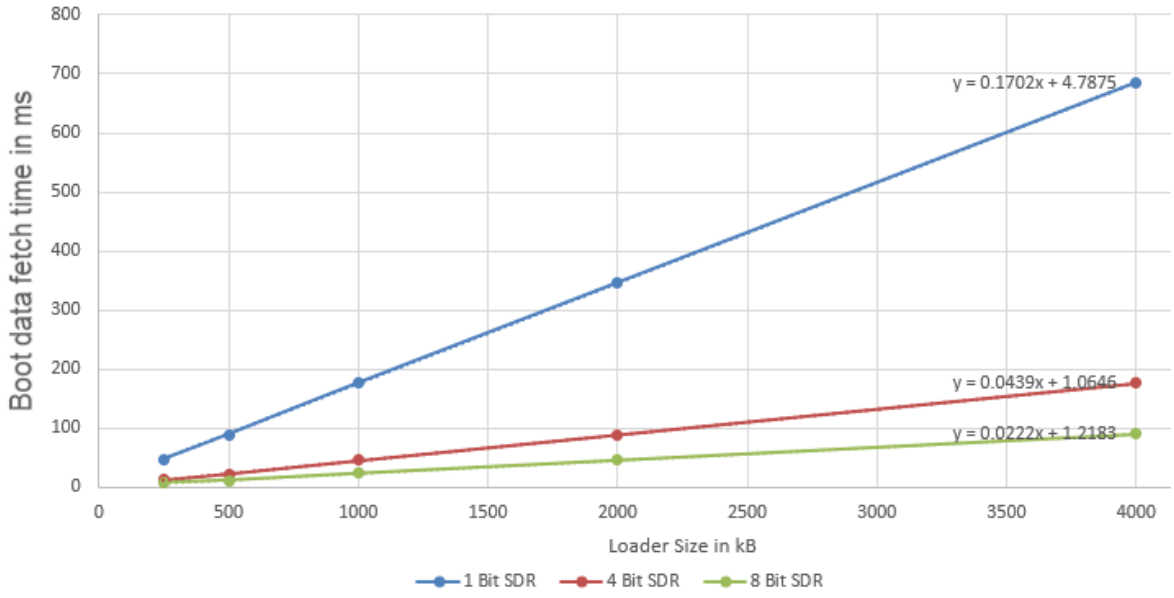


Figure 15: eMMC BLx Secure Boot Data Fetch at 50 MHz (User Area Partition)

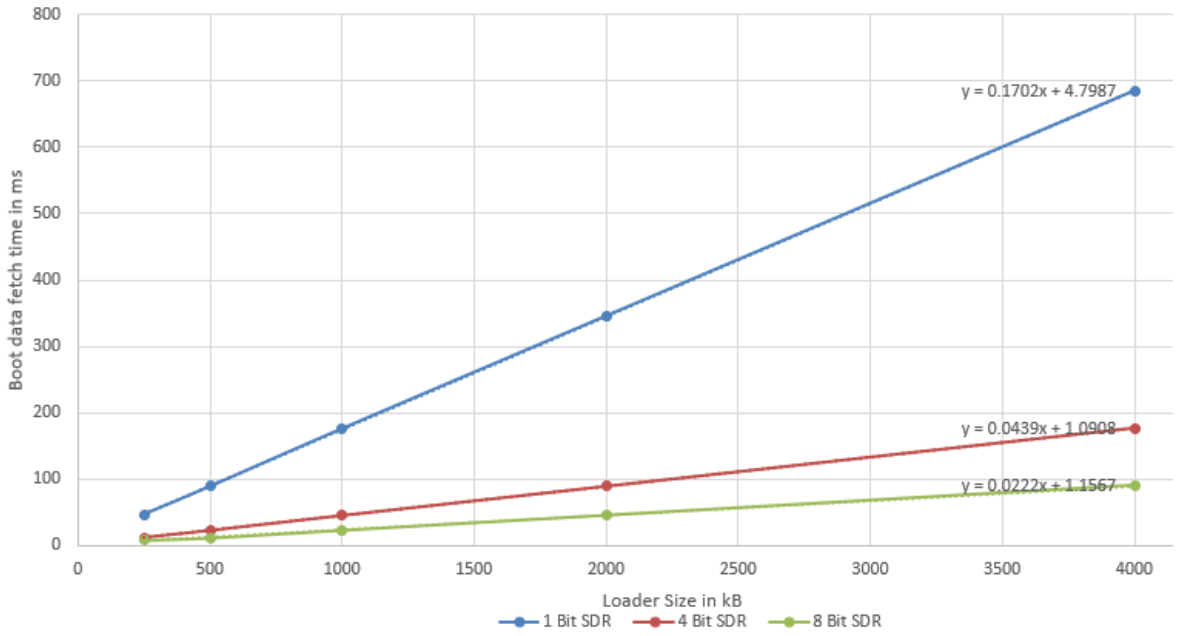


Figure 16: eMMC BLw Secure Boot Data Fetch at 50 MHz (User Area Partition)

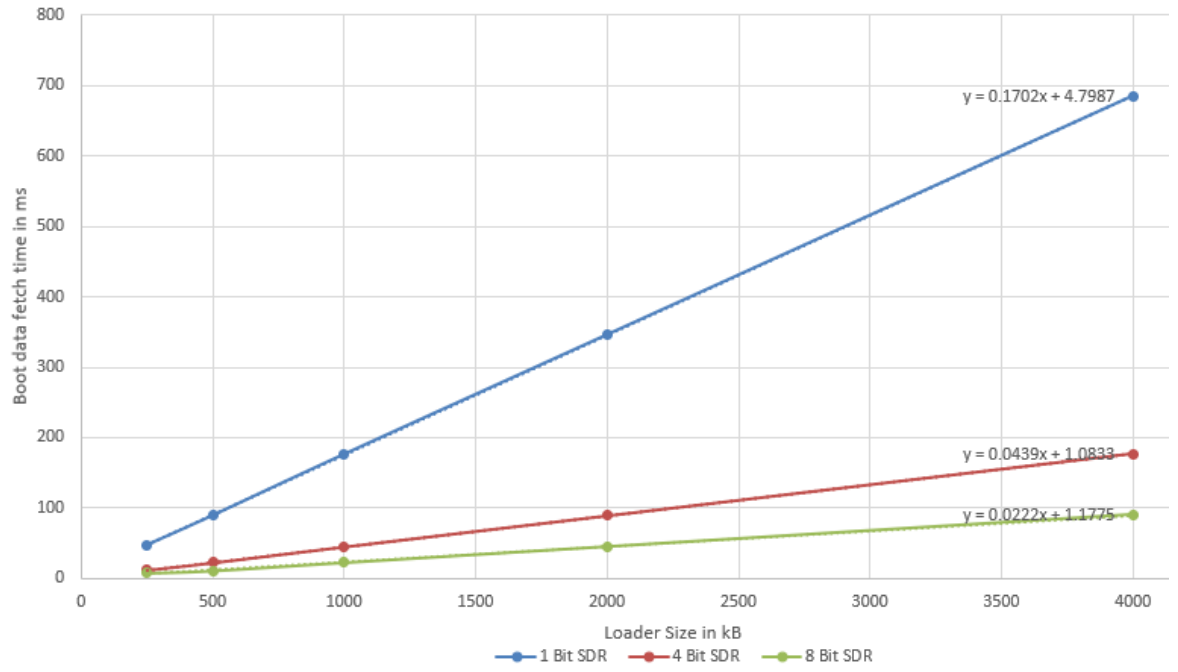


Figure 13 through Figure 16 data was measured with the IS22ES08G-JCLA1 eMMC device (EV-SC598-SOM-EZKIT).

User Area Partition Total Boot Time Calculation (Safe Boot Mode)

Equation 2: Total Boot Time (Safe Boot Mode)

Total boot time in safe boot mode (measured in µs) = Processing time + Command time + N_{AC} Time + Data time + Constant timings (Independent of number of blocks)

Variables:

- **Processing time**–7 * (Number of 1 kB blocks)
- **Command time**–240 * (eMSI bus clock period in µs) * (Number of 1 kB blocks)
- **N_{AC} Time**–N_{AC} (in µs) * (Number of 1 kB blocks)
- **Data time**–1024 * (eMSI bus clock period * [8 / (Bus width * Data Rate)]
- **Constant timings** (Independent of number of blocks)–
- eMMC device initialization time (user area partition) + 1 ms to 2 ms (Miscellaneous, same for all eMMC devices)
  - **Number 1 kB blocks**–Total loader size (in bytes) / 1024
  - **Data Rate**–1 for SDR speed mode or 2 for DDR speed mode

Total Boot Time Calculation Example (Safe Boot Mode)

This example uses timing parameters calculated for the ISSI eMMC device (IS22ES08G-JCLA1). Table 4 displays the parameters used in calculating total boot time in safe boot mode.

Table 4: Safe Boot Mode Example Parameter Values

Parameter	Value
Loader image size	1088624 bytes
Number of 1 kB blocks	1064
N_{AC}	142 µs
eMSI bus clock period	0.02 µs (50 MHz)
Bus width	8 Bit
Speed mode	1=SDR
Card initialization time	7000 µs

Substituting the Table 4 parameter values into Equation 2, yields a total boot time:

= (((7) + (240 * (0.02)) + (142) + (1024 * (0.02) * (8/(8*1))))*1064)

+ (7000+ (1000)) = 193433.92 µs

Table 5 shows the estimated boot time, measured boot time, and the error percentage

Table 5: Estimated and Measured Boot Time (Safe Boot Mode)

Parameter	Value
Estimated boot time using equation	193,433.92 µs

Actual measured boot time	194,800 µs
Percentage Error	0.7 %

User Area Partition Total Boot Time Calculation (Default Boot Mode)

Equation 3: Total Boot Time (Default Boot Mode)

Total boot time in default boot mode (in ms) = Time Calculated from graph + Constant timings for eMMC device

- Constant timing timings for eMMC device–eMMC device initialization time (user area partition) + 1 ms to 2 ms (Miscellaneous, same for all eMMC devices)

Total Boot Time Calculation Example (Default Boot Mode, User Area Partition)

This example uses timing parameters calculated for ISSI eMMC device (IS22ES08G-JCLA1). Table 6 shows the parameters and the equation used in calculating the total boot time in the default boot mode (User area partition).

Table 6: Default Boot Mode Example Parameter Values (User Area Partition)

Parameter	Value
Loader image size	108,8624 bytes (1000 kB)
eMSI bus clock period	0.02 µs (50 MHz)
Bus width	8 Bit
Speed mode	SDR
Card initialization time	7000 µs
Equation used from graph	y = 0.0222x + 1.0896 (Figure 13)

After substituting Table 6 parameter values into Equation 3, the total boot time equals:

= 0.0222(1000) + 1.0896 + (7 ms + 1 ms)

= 31.28 ms

Table 7 shows the estimated boot time, measured boot time, and error percentage.

Table 7: Estimated and Measured Boot Time (Default Boot Mode)

Parameter	Value
Estimated boot time using equation	31.28 ms
Actual measured boot time	30.65 ms
Percentage Error	2 %

Boot Area Partition

Figure 17 through Figure 20 show the calculated linear equations for the eMMC boot area boot mode for data fetching at the 50 MHz eMSI bus clock frequency, including normal boot and secure boot with ECDSA-256 authentication.

Figure 17: eMMC Normal Boot Data Fetch at 50 MHz (Boot Area Partition)

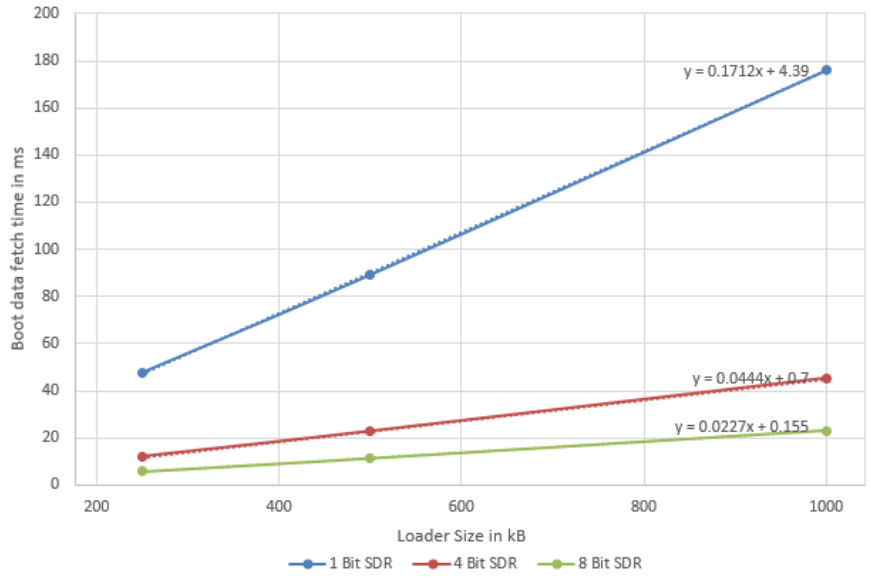


Figure 18: eMMC BLp Secure Boot Data Fetch at 50 MHz (Boot Area Partition)

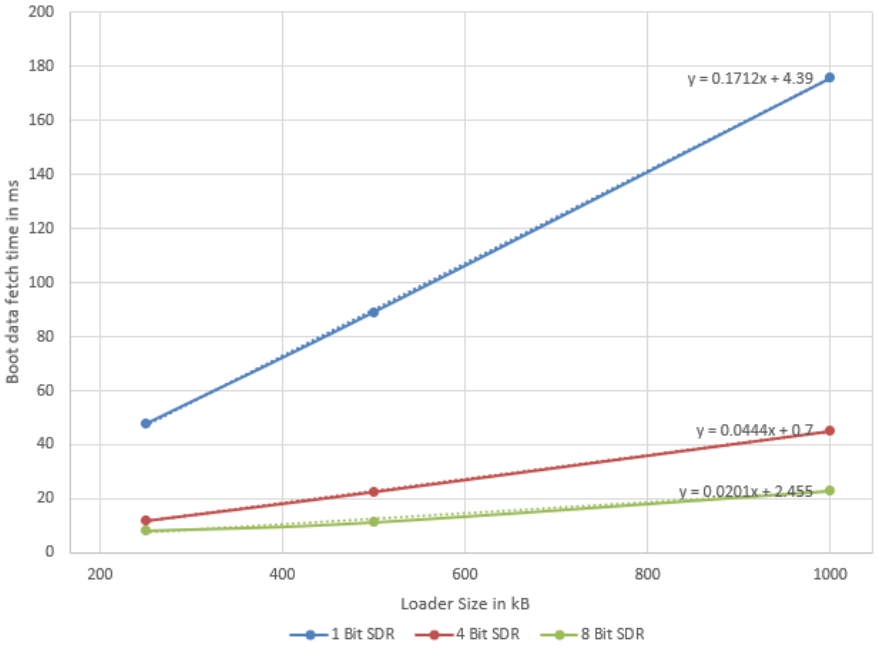


Figure 19: eMMC BLx Secure Boot Data Fetch at 50 MHz (Boot Area Partition)

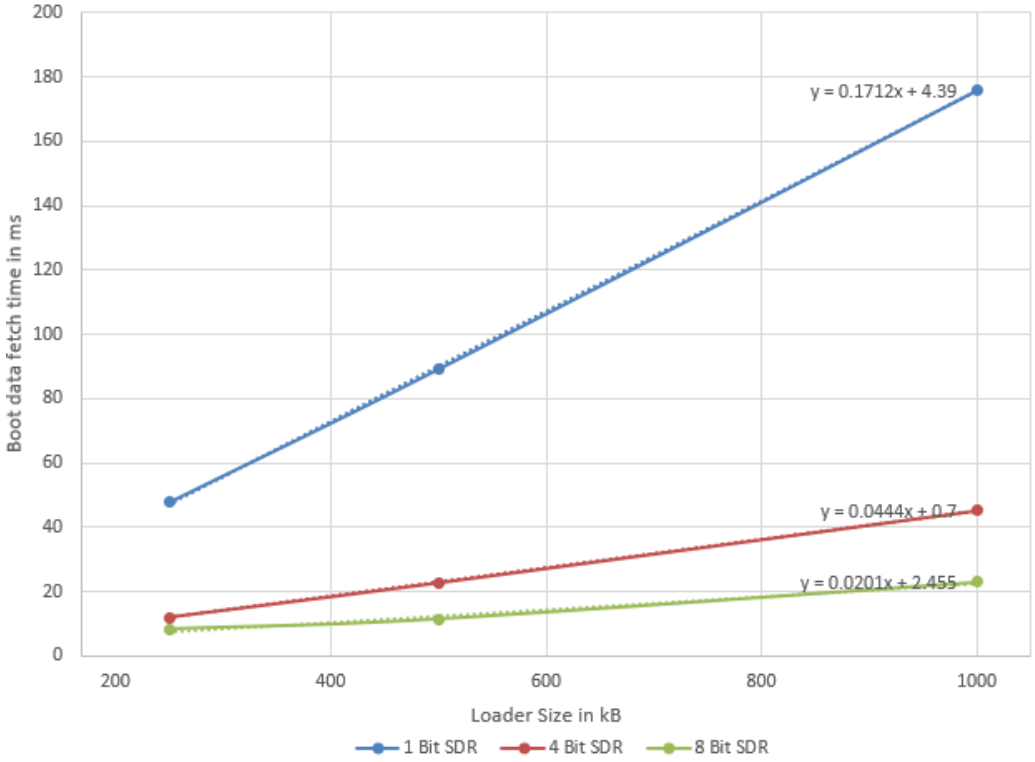
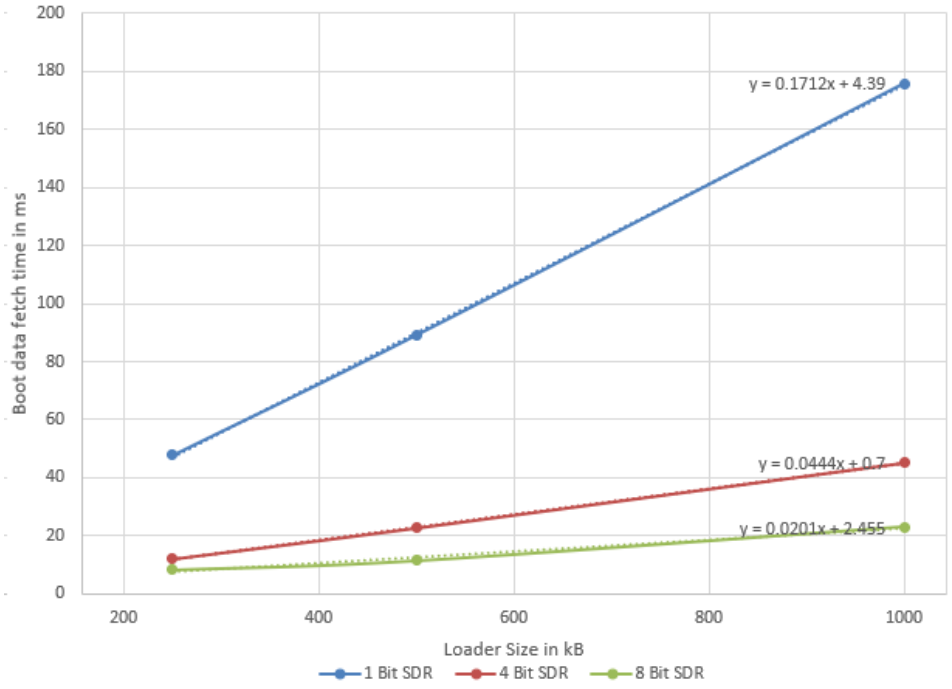


Figure 20: eMMC BLw Secure Boot Data Fetch at 50 MHz (Boot Area Partition)



All data was measured using the IS22ES08G-JCLA1 eMMC device present on the EV-SC598-SOM-EZKIT.

Boot Area Partition Total boot Time Calculation (Default Boot Mode)

Equation 4: Total Boot Time (Boot Area Partition, Default Boot Mode)

Total boot time in default boot mode (in ms) = Time Calculated from graph + Constant timings for eMMC device

- Constant timings for eMMC device–eMMC device initialization time (User area partition) + 1 ms (miscellaneous, same for all eMMC devices)

Total Boot Time Calculation Example (Boot Area Partition, Default Boot Mode)

This example is based on timing parameters calculated for the ISSI eMMC device (IS22ES08G-JCLA1). Table 8 shows various parameters and equation which are useful in calculating total boot time in default boot mode (Boot area partition).

Table 8: Boot Time Calculation Parameter Values (Default Boot Mode)

Parameter	Value
Loader image size	1088624 bytes (1000 kB)
eMSI bus clock period	0.02 µs (50 MHz)
Bus width	8 Bit
Speed mode	SDR
Card initialization time	4.8 ms
Equation used from graph	y = 0.0227x + 0.155 (Figure 17)

The total boot time after substituting all Table 8 values into Equation 4 yields:

= 0.0227 * (1000) + 0.155 + (4.8 ms + 1 ms)
= 28.655 ms

Table 9 shows estimated boot time, actual measured boot time, and percentage error.

Table 9: Estimated and Measured Boot Time (Default Boot Mode)

Parameter	Value
Estimated boot time using equation	28.655 ms
Actual measured boot time	27.7 ms
Percentage Error	3.3 %

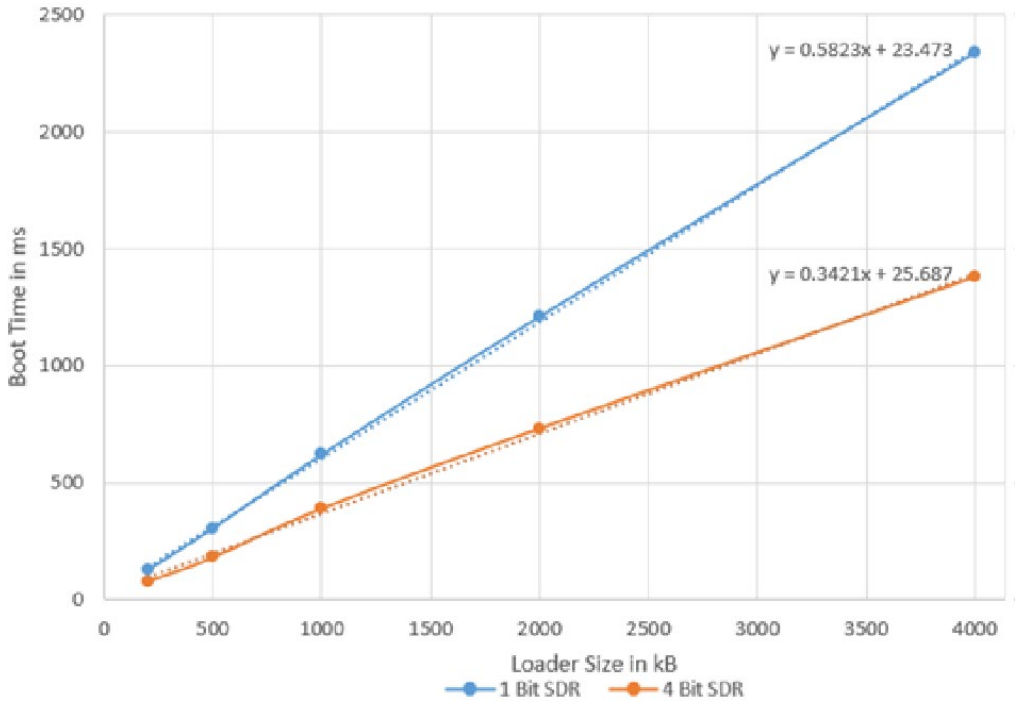
SD Card Custom Boot

The SD card custom boot can be used to boot from SD cards trough the eMSI peripheral that includes 1-bit SDR and 4-bit SDR speed modes. The boot supports a maximum of 44.4 MHz eMSI bus clock frequency. The ADSP-SC598 processor family only supports a single SD card.

The custom boot support developed for this EE- Note is like the safe boot mode option in eMMC boot mode. In this mode, a read command is issued each time to fetch 1 KB of boot stream data. An engineer can modify the init, config, load, and cleanup routines to further customize SD card boot.

Figure 21 provides the calculated linear boot time equation for SD card normal boot at 25 MHz eMSI bus clock.

Figure 21: SD Card Custom Boot (Normal) at 25 MHz



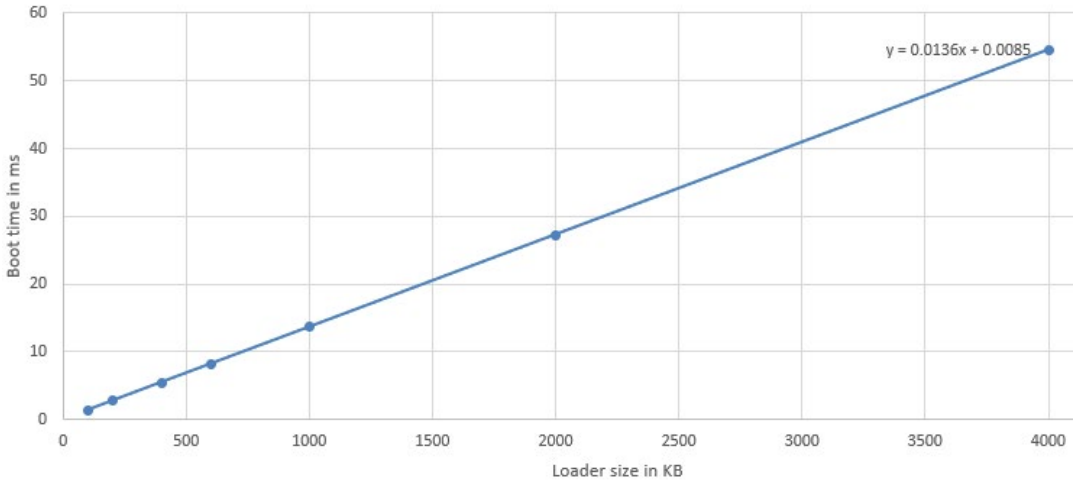
All data was measured using the SanDisk Extreme PRO SD card and connected externally to EV-SC598-SOM-EZKIT using a socket.

Linkport External Host Boot

The Link port boot (SYS_BMODE 4) is an external host boot mode in which the processor receives boot data from an external link port host through link port (LP0). The link port is configured as receiver with 8-bit SDR and the host needs to send the data in the same mode. DMA control performs all transfers from the link port to memory. The maximum supported operating frequency of the link port is 125 MHz, where the host boot source must drive the clock frequency. By using Initcode or OTP to configure the CGU for the maximum clock supported (SYSCLK 500 MHz and SCLK0 125 MHz), the host boot source drives the clock frequency. The link port receiver operates at an asynchronous frequency up to the maximum supported operating frequency.

Figure 22 provides the calculated linear boot time equation for Linkport normal boot at 75 MHz LP CLK.

Figure 22: Linkport Normal Host Boot at 75 MHz (8-bit SDR)



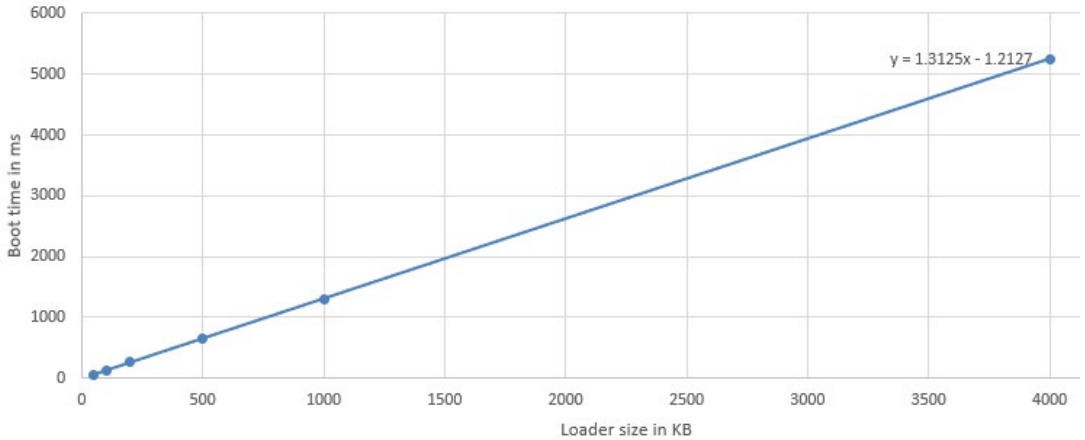
Linkport boot timings further improve using the125 MHz maximum clock frequency.

UART External Host Boot

UART External Host Boot (SYS_BMODE 3) for ADSP-SC595/SC596/SC598 SHARC processors is an external host boot mode, where the processor receives boot data from a UART host device connected to the UART interface. UART0 is the default booting peripheral. The maximum UART Clock supported for UART boot is 7.8 MHz, which can be achieved by using init code or OTP to configure the CGU for maximum clock supported (SYSCLK 500 MHz and SCLK0 125 MHz). Because UART is a slow peripheral, the boot time for normal and secure boot modes is identical, with boot time primarily dependent on the peripheral loading time.

Figure 23 provides the calculated linear boot time equation for UART normal boot at 7.8 MHz UART CLK.

Figure 23: UART External-host Boot at 7.8 MHz



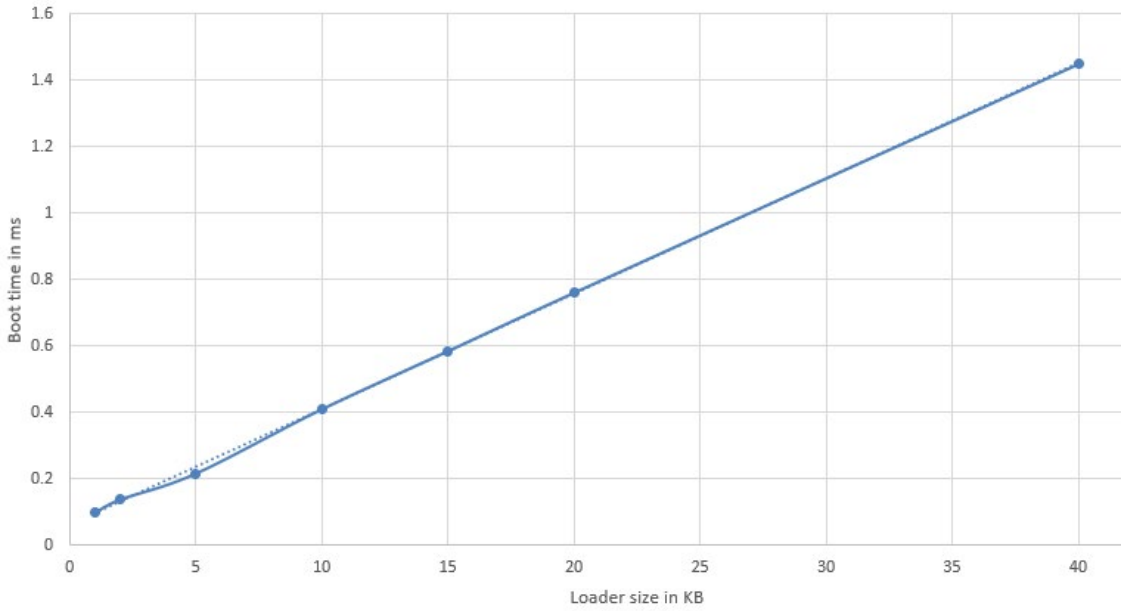
Boot Time Nonlinearity

The figures from earlier sections provide calculated linear equations for boot time using varied sizes of loader stream. But the linearity relationship is not consistent when the loader stream is smaller (both non-secure and secure boot). This section shows how boot time for a small loader stream follows a non-linearity in terms of non-secure boot, and reaches a saturation time for a secure boot.

Nonlinearity in Non-secure Boot Time

Figure 24 shows the boot time for SPI Quad Flash boot (BCODE 9) with smaller loader stream and a size less than 10 KB is non-linear. Estimating the boot time using linear equations calculated in earlier sections is not accurate. ADI advises users to test the exact boot time for loader streams smaller than 10 KB.

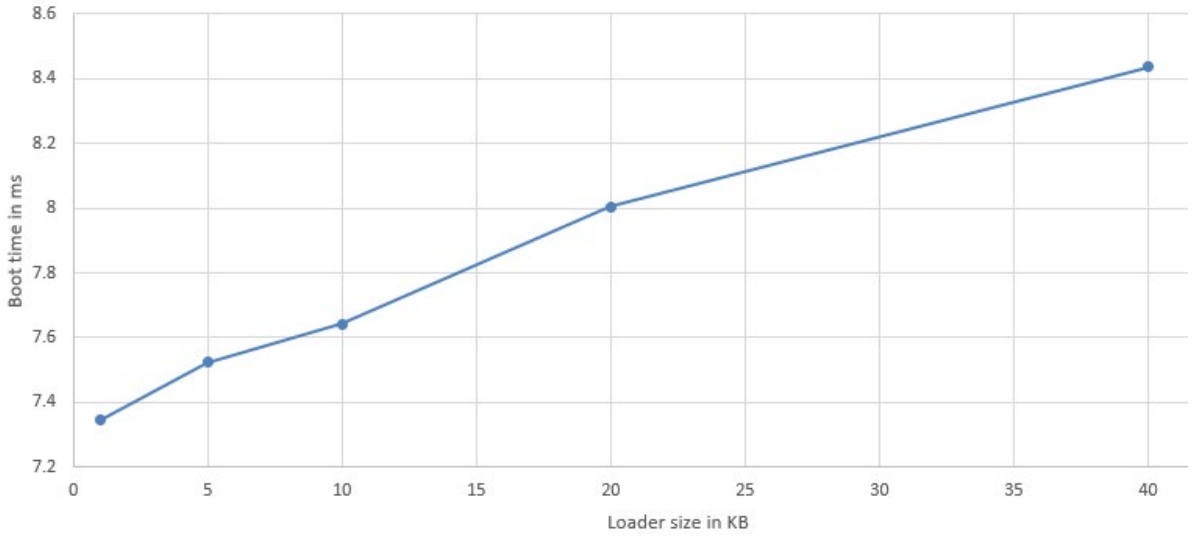
Figure 24: SPI2 Quad Boot Time Nonlinearity at 62.5 MHz (CCLK= 1.2 GHz and SPI CLK=62.5 MHz)



Nonlinearity in non-secure boot time is not affected by the Boot ROM, but due to the smaller measured sample size for the smaller (KB) loader stream.

Figure 25 shows the boot time for an 8-bit SDR (default boot mode, User area partition, CCLK=1.2 GHz, and eMSI CLK=1.2 GHz), with small loader stream of less than 20 KB, is non-linear.

Figure 25: eMMC Non-linear Boot Time (50 MHz, Default Boot Mode, User Area Partition)



Nonlinearity in Secure Boot Time

The pre-calculated SHA hash digest in the secure header starts the authentication process in parallel with the booting process, while loading the full image for processing hash and decryption. Because in large boot images, secure boot time is independent of the authentication routine. For smaller boot images, where loading time is less than authentication routine completion time, secure boot time reaches a saturation point. Because of the parallel activity, the authentication routine determines the saturation point.

Figure 26 shows that the saturation level for SPI BLw secure quad (BCODE 9) boot (CCLK=1.2 GHz, SYSCLK=500 MHz, and SPI CLK=62.5 MHz) starts at 200 KB stream size. The boot time saturates at approximately 9 milliseconds. The linear equation for computing the boot time of a BLw secure boot (see earlier sections) supports a loader stream size larger than 200 KB.

Figure 26: SPI2 Secure Quad Non-linear Boot Time Saturation

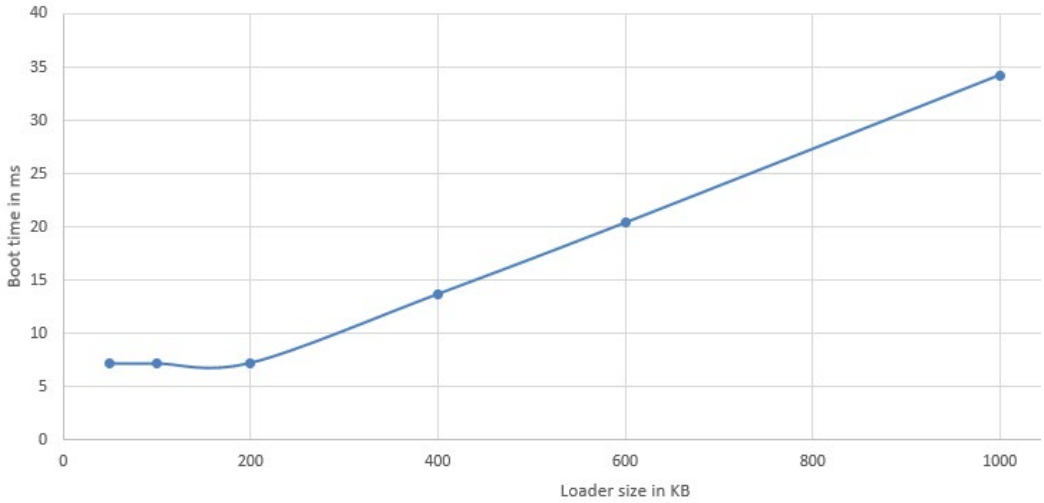


Table 10 shows the approximate saturation points for different secure boot using ECDSA-256 authentication in all the flash boot modes, with a maximum frequency (CCLK=1.2 GHz, SYSCLK=500 MHz, and SPI/OSPI CLK=62.5 MHz). Boot time is below saturation or approximately 9 ms.

Table 10: Non-linear Saturation Point for Different Flash Secure Boot Modes

Secure Boot Mode	Saturation Point
SPI Master Single Mode	50 KB
SPI Master Dual Mode	100 KB
SPI Master Quad Mode	200 KB
OSPI Master Single-STR	50 KB
OSPI Master Dual-STR	100 KB
OSPI Master Quad-STR	200 KB
OSPI Master Single-DTR	100 KB
OSPI Master Dual-DTR	200 KB
OSPI Master Qual-DTR	400 KB

As the crypto engine runs on the SYSCLK, the table saturation points vary as the frequency changes. For example, when SYSCLK changes from 500 MHz to any lower value, the authentication routine completion time increases, which results in an increase of the saturation point.

Factors Affecting Total Boot Time

Application size primarily affects the boot time for the ADSP-SC595/SC596/SC598 SHARC processors. All calculated linear equations provided in the earlier sections consider only the loader stream size. There are other factors that affect the total boot time, including pre-boot time, fill blocks, and init block. These factors are explained in the following sections, which make the total boot time estimation for a given application more accurate.

Pre-boot Time

Pre-boot time accounts for the configuration of all system resources before starting the required boot operation. This includes:

- Core Initialization
- SPU and SMPU configuration
- Secure debug key processing
- CGU configuration
- DMC configuration
- Fault configuration
- L1 memory initialization etc.

CGU configuration and DMC initialization routines impact the pre-boot execution time when programming with the OTP. See the *ADSP-SC59x/SC596/SC598 SHARC+® Processor Hardware Reference* [1] for more details about pre-boot. Table 11 shows the pre-boot time under different conditions.

Table 11: Pre-boot Times Under Different Conditions

Condition	ADSP-SC594 Pre-boot Time
Default	2.294 ms
CGU configuration enabled (OTP programmed for 1 GHz CCLK)	2.253 ms

ADI advises against using OTP programming for DMC initialization in pre-boot, as per *Anomaly :20000124*. Instead, use the Initcode routine or a multi-stage boot to perform pre-boot.

Effect of Fill Blocks in Boot Time Estimation

A fill block instructs the boot kernel to perform a 32-bit memory fill of the memory region. Fill blocks help to minimize the size of a boot stream, when an application contains large data arrays that must be initialized at application startup. The size of a loader stream does not depend on this 16-byte block. But having multiple fill blocks in a fixed size loader stream does affect the total boot time, which includes the extra time to process each fill block header and the time required for the DMA configuration in each block.

All the computed boot time equations in previous sections did not account for fill blocks present in the loader stream. Figure 27 provides the calculated linear equation based on testing with SPI quad boot (BCODE 9) at 62.5 MHz SPI CLK. Use this equation to compute the extra boot time taken because of fill blocks. Currently, the extrapolated equation is used for all the controller boot modes which use MDMA channels, assuming fill block processing time is independent of peripheral loading time. Expect more data in future EE-Note revisions to generalize the fill block time across all the boot modes.

Figure 27: Extra Boot Time Because of Fill Blocks

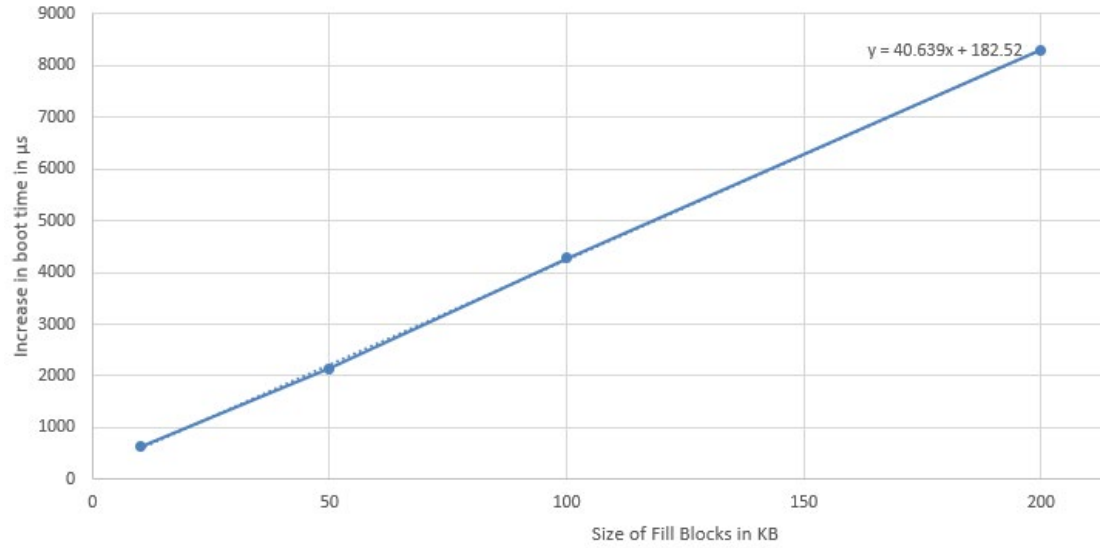


Figure 26 gives the measurement for 10 fill blocks present in the loader stream. For any other number of fill blocks, scale the boot time numbers by the same factor.

EE432: Boot Time Estimation for ADSP-SC59x/ADSP-2159x SHARC+ Processors [4] explains more on fill blocks with an example on how to estimate boot time for any user loader stream more accurately with the presence of fill blocks.

A larger loader stream always adds an extra penalty for consuming more space in the external flash, which also increases the overall system cost. Fill blocks in such cases, help in reducing the loader stream size at the cost of additional total boot time. There should be a good trade-off between boot time and size of the loader stream.

Init Block Effect on Boot Time Estimation

An initialization or init block instructs the boot kernel to perform a function call to the target address after the entire block has loaded. The called function called is named as the initialization code (Initcode) routine. Use Initcode routines to speed up and customize booting mechanisms exposed by the boot kernel. Traditionally, engineers use an Initcode routine to set up the system PLL, bit rates, wait states, and external memory controllers. Significant boot time reductions happen when starting an init block early in the boot process.

Init Code start time depends on all the features that are enabled inside the initcode application, which impact the total boot time. For information on implementing an init block, see *ADSP-SC59x/SC596/SC598 SHARC+® Processor Hardware Reference* [1].

The secure boot scenario does not support Initcode routines.

Comparison of Boot Time Among Different Processors

This section provides total boot time comparison for various processors that includes ADSP-SC57x, ADSP-2156x, ADSP-2159x/ADSP-SC59x, and ADSP-SC598 families. The comparisons provide the best boot time for all the variants, whether it is an SPI quad-STR boot for the ADSP-SC57x family, an OSPI quad-DTR boot for ADSP-2156x family, or an OSPI quad-DTR boot for ADSP-2159x/ADSP-SC59x and ADSP-SC598 family.

Table 12 through Table 15 give the boot time comparisons across all three processor families for the four different boot modes; that is, Normal, Secure BLp, Secure BLx, and Secure BLw.

Normal Boot Time Comparison

Table 12: Normal Boot Time Comparison Among Processors

Loader Stream Size in KB	SPI Quad-STR Boot in ms	OSPI Quad-DTR Boot in ms		
	ADSP-SC573	ADSP-21569	ADSP-21593	ADSP-SC598
	SPI Clock=75 MHz	OSPI Clock= 62.5 MHz		
500	24.5325	10.0755	10.2661	8.2054
1000	43.2825	18.5255	18.4661	16.4054
2000	80.7825	35.4255	34.8661	32.8054
4000	155.7825	69.2255	67.6661	65.6054
8000	305.7825	136.8255	133.2661	131.2054
12000	455.7825	204.4255	198.8661	196.8054

BLp Secure Boot Time Comparison

Table 13 :Secure BLp Boot Time Comparison Among Processors

Loader Stream Size in KB	SPI Quad-STR Boot in ms	OSPI Quad-DTR Boot in ms		
	ADSP-SC573	ADSP-21569	ADSP-21593	ADSP-SC598
	SPI Clock=75 MHz	OSPI Clock= 62.5 MHz		
500	40.23	17.2902	14.9717	12.6565
1000	62.68	27.2402	24.1717	20.4565
2000	107.583	47.1402	42.5717	36.0565
4000	197.383	86.9402	79.3717	67.2565
8000	376.9	166.5402	152.9717	129.6565
12000	556.5	246.1402	226.5717	192.0565

BLx Secure Boot Time Comparison

Table 14: Secure BLx Boot Time Comparison Among Processors

Loader Stream Size in KB	SPI Quad-STR Boot in ms	OSPI Quad-DTR Boot in ms		
	ADSP-SC573	ADSP-21569	ADSP-21593	ADSP-SC598
	SPI Clock=75 MHz	OSPI Clock= 62.5 MHz		
500	54.877	19.7049	16.8513	12.6728
1000	92.627	30.2549	26.5513	20.4728
2000	168.127	51.3549	45.9513	36.0728
4000	319.127	93.5549	84.7513	67.2728
8000	621.127	177.9549	162.3513	129.6728
12000	923.127	262.3549	239.9513	192.0728

BLw Secure Boot Time Comparison

Table 15: Secure BLw Boot Time Comparison Among Processors

Loader Stream Size in KB	SPI Quad-STR Boot in ms	OSPI Quad-DTR Boot in ms		
	ADSP-SC573	ADSP-21569	ADSP-21593	ADSP-SC598
	SPI Clock=75 MHz	OSPI Clock= 62.5 MHz		
500	54.026	19.5518	17.2634	12.6808
1000	91.726	30.1018	26.4134	20.4808
2000	167.126	51.2018	44.7134	36.0808
4000	317.926	93.4018	81.3134	67.2808
8000	619.526	177.8018	154.5134	129.6808
12000	921.126	262.2018	227.7134	192.0808

References

[1] *ADSP-SC59x/SC596/SC598 SHARC+® Processor Hardware Reference*. Rev 0.2, August 2023, Analog Devices, Inc. https://www.analog.com/media/en/dsp-documentation/processor-manuals/adsp-sc595-sc596-sc598-hrm.pdf

[2] *EE366: Secure Booting Guide for Blackfin+® and SHARC+® Processors*. Rev 2, October 19, 2016, Analog Devices, Inc. https://www.analog.com/media/en/technical-documentation/application-notes/EE366v02.pdf

[3] *EE384: Tips and Tricks Using the ADSP-SC58x/ADSP-2158x Processor Boot ROM*, Rev 1, September 30,2015, Analog Devices, Inc. https://www.analog.com/media/en/technical-documentation/application-notes/EE384v01.pdf

[4] *EE432: Boot Time Estimation for ADSP-SC59x/ADSP-2159x SHARC+ Processors*. Rev 1, August 23, 2021, Analog Devices, Inc. https://www.analog.com/media/en/technical-documentation/application-notes/ee432.pdf

[5] *EE438 Note* `Example_Codes.zip` *file*. Rev1, September 17, 2023, Analog Devices, Inc. https://www.analog.com/en/products/adsp-sc598.html#product-documentation

[6] *ADSP-SC595/SC596/SC598 Anomaly Lis*t, Rev D, April 2023, Analog Devices, Inc. https://www.analog.com/media/en/dsp-documentation/integrated-circuit-anomalies/adsp-sc595-sc596-sc598-anomaly.pdf

Document History

Revision	Description
Rev 1 – October 4, 2023 Saikia, Juganta & Joshi, Sammit*3*	Initial Draft Release