Engineer-to-Engineer Note   EE-433

Estimating Power for ADSP-2159x/SC59x SHARC+® Processors

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Introduction

This EE-note describes how to estimate power consumption on ADSP-2159x/SC59x processors, which include SHARC+[®] high-performance cores and a multitude of peripherals, accelerators, and high-speed Direct Memory Access (DMA) channels. These processors have multiple power and clock domains. This application note provides a simplified methodology for estimating the total System-on-Chip (SoC) power consumption depending on the amount of processor activity.

Power estimates are based on design simulations and characterization data measured across power supply voltage, core and system clock frequency, and junction temperature (T_J). The power can vary widely depending on how the on-chip ADSP-2159x/SC59x SHARC+® Processor resources are used. Thus, power consumption cannot be estimated accurately without an understanding of the components in use and the usage patterns for those components. By providing the usage parameters, board designers can obtain accurate consumption estimates for developing power supply and thermal relief solutions for their ADSP-2159x/SC59x SHARC+® Processor based products.

See the following sections of the *ADSP-2159x/SC59x SHARC+® Processors datasheet[1]* for details specific to discussions throughout this EE-Note:

- See the O*perating conditions* section for details regarding supported power supply ranges
- See the *Electrical Characteristics* and subsequent *Total Internal Power Dissipation* sections for details regarding current specifications.

In the *associated file[2]* furnished with this EE-note, there is a convenient power calculator tool. This tool allows users to obtain a total power profile by populating the cells in a spreadsheet with data found both in the processor data sheet and calculations specific to the intended application. This document explains the cases related to the information of the power calculator, not mentioned in the data sheet.

This EE-note also describes how to provide the appropriate input to the power calculator such that the full power profile for the application can be obtained. It describes how the calculations are made and how the results contribute to the overall power profile.

Power Domains

There are multiple power domains associated with the ADSP-2159x/SC59x SHARC+® processor; total power consumption is the sum of the power consumed across all the power domains. There are four major power domains that are significant contributors to the overall power profile:

- V_{DD_INT}: most internal on-chip logic (for example, core, accelerators, DMA engines etc.)
- V_{DD_EXT}: for example, I/O pad ring, JTAG
- V_{DD_REF}: I/O reference supply
- V_{DD_DMC}: DDR controller

The power consumption from the following supply domains is insignificant and not considered part of the associated power calculator.

- V_{DD_ANA}: Power supply for HADC/TMU analog blocks.

Estimating Internal Power Consumption ($P_{DD\_INT\_TOT}$)

The total power consumption associated with the on-chip logic (on the V_{DD_INT} supply) is the sum of the static (leakage) and dynamic (switching) power components. The dynamic component depends primarily on processor activity, which includes the instruction execution sequence, the data operands involved, and the instruction rate on each core, as well as the number of active peripherals/accelerators, their clock rates, and any associated DMA data traffic. The dynamic current is also influenced by temperature. The static component is independent of processor activity and is a function of temperature and voltage.

The internal current ($I_{DD\_INT\_TOT}$) consumed by the ADSP-2159x/SC59x SHARC+® Processors comprises of:

- $I_{DD\_INT\_STATIC}$: leakage current
- $I_{DD\_INT\_CCLK\_SHARC0\_DYN}$: dynamic current in the CCLK domain for the SHARC+ core 0
- $I_{DD\_INT\_CCLK\_SHARC1\_DYN}$: dynamic current in the CCLK domain for the SHARC+ core 1
- $I_{DD\_INT\_CCLK\_A5\_DYN}$: dynamic current in the CCLK domain for the A5 core
- $I_{DD\_INT\_DCLK\_DYN}$: dynamic current in the DCLK domain (no other activity)
- $I_{DD\_INT\_SYSCLK\_DYN}$: dynamic current in the SYSCLK domain (no other activity)
- $I_{DD\_INT\_SCLK0\_DYN}$: dynamic current in the SCLK0 domain (no other activity)
- $I_{DD\_INT\_SCLK1\_DYN}$: dynamic current in the SCLK1 domain (no other activity)
- $I_{DD\_INT\_OCLK\_DYN}$: dynamic current in the OCLK domain (no other activity)
- $I_{DD\_INT\_DMA\_DR\_DYN}$: dynamic current consumed due to DMA activity
- $I_{DD\_INT\_ACCL\_DYN}$: dynamic current consumed by the FIR/IIR accelerator blocks

Therefore, the total current can be expressed as the sum of each of the above components, where there is a single static power component and several dynamic power components that must be included in the overall power profile.

Maximum specifications for I_{DD_INT} are provided in the processor data sheet at specific voltages, frequencies, and temperatures. The following sections describe how to use this

data to calculate the overall power requirements of the application.

Estimating Total I$_{DD\_INT}$ Dynamic Current

Due to the multi-featured clock and power capabilities of the ADSP-2159x/SC59x SHARC+® Processors, there are many contributors to the overall dynamic component associated with the power consumed by the core. While there is opportunity to disable clocks to the various domains, each must be scrutinized to determine what factors must be accounted for with respect to power dissipation when any combination of these domains is active in the system.

> ⓘ The dynamic current data included as part of this EE-note and associated power calculator spreadsheet pertains to maximum junction temperature of 125°C and the worst-case (highest-power) fabrication process.

Core Dynamic Current ((IDD_INT_CCLK_A5_DYN, IDD_INT_CCLK_SHARC1_DYN, and IDD_INT_CCLK_SHARC2_DYN))

The ADSP-2159x/SC59x SHARC+® Processor data sheet provides the baseline dynamic current consumption specifications, which are obtained with the processor running a 'typical' application. It is represented in the data sheet by the I$_{DD\text{-}TYP}$ specification. However, these conditions do not represent all possible application code. The concept of silicon process variation is also ignored, which influences the power profile because of non-uniform transistor physics across the silicon. When making decisions regarding the power supply design, the worst-case scenario must always be considered. The above assumptions are addressed using two different tables in the data sheet, to extrapolate and obtain the maximum requirements for the power supply design:

- *Dynamic Current* tables – provide the maximum (across process and temperature) core dynamic current specification as a function of voltage (V$_{DD\_INT}$) and frequency (f$_{CCLK}$) while running 'typical' application code
- *Activity Scaling Factor (ASF)* tables – describe discrete dynamic activity levels to provide insight on how the dynamic current scales with changing loads on the core

Using these combined specifications, the dynamic component of core power consumption can be obtained by multiplying the baseline spec obtained from the *Dynamic Current* tables and the associated *Activity Scaling Factor*, as further explored in the following sections.

ARM Cortex-A5 Activity Scaling Factor (ASF) Vectors

The Activity Scaling Factors for ARM Cortex-A5 Core table in the datasheet defines the following vectors:

- I$_{DD\text{-}IDLE}$: ARM core executing the IDLE instruction ("idle activity") only

- I$_{DD\text{-}DHRYSTONE}$: ARM core executing Dhrystone benchmark algorithm
- I$_{DD\text{-}2575}$: ARM core executing 25% peak activity and 75% idle activity
- I$_{DD\text{-}5050}$: ARM core executing 50% peak activity and 50% idle activity
- I$_{DD\text{-}7525}$: ARM core executing 75% peak activity and 25% idle activity (used for

IDD_TYP spec)

- $I_{DD\text{-PEAK\_100}}$: ARM core continuously thrashing cache memory with maximum data changes ("peak activity")

> The test code used to measure $I_{DD\text{-PEAK\_100}}$ represents the worst-case core operation and is not sustainable under normal application conditions.

In addition to the ASFs (Activity Scaling Factor), the power calculator defines the following vector on the *Core Activity Factors* tab:

- $I_{DD\text{-CLOCK\_GATED}}$: Arm core clock disabled (no dynamic power)

SHARC+® Core Activity Scaling Factor (ASF) Vectors

The *Activity Scaling Factors for SHARC+ Core0* table in the data sheet defines the following vectors:

- $I_{DD\text{-IDLE}}$: SHARC+ core executing the IDLE instruction only
- $I_{DD\text{-NOP}}$: SHARC+ core executing 100% NOPs
- $I_{DD\text{-TYP\_3070}}$: SHARC+ core executing 30% floating-point (FP) multiply/add/subtract and store instructions and 70% NOPs
- $I_{DD\text{-TYP\_5050}}$: SHARC+ core executing 50% floating-point (FP) multiply/add/ subtract and store instructions and 50% NOPs
- $I_{DD\text{-TYP\_7030}}$: SHARC+ core executing 70% floating-point (FP) multiply/add/ subtract and store instructions and 30% NOPs (used for I_{DD_TYP} specification)
- $I_{DD\text{-PEAK\_100}}$: SHARC+ core executing 100% floating-point (FP) multiply/add/subtract and store instructions
- $I_{DD\text{-LS}}$: SHARC+ core in light sleep mode (new feature added in ADSP-2159x/SC59x SHARC+® Processors)

> The test code used to measure $I_{DD\text{-PEAK\_100}}$ represents the worst-case core operation and is not sustainable under normal application conditions.

In addition to the ASFs (Activity Scaling Factor), the *power calculator* defines the following vector on the *Core Activity Factors* tab:

- $I_{DD\text{-CLOCK\_GATED}}$: SHARC+ core clock disabled (no dynamic power)

Low Power Features

The ADSP-2159x/SC59x SHARC+® processors provide an additional power-saving feature to reduce power consumption in on-chip L1 memory and when the core is idle.

- Low Power Idle Mode (core light sleep): When the core goes into the idle state, upon executing the IDLE instruction, there exists active/switching power associated with all active clocks (even though there is no activity inside the core). To reduce the power, program the core light sleep enable field, which is a core clock gating mechanism (core light sleep) for switching off these clocks.

> The core light sleep mechanism is effective only when the processor is booted, and NOT when executing from an emulator.

> Additional modes such as Memory Sleep and Memory Shutdown mentioned in the SHARC+ Core Programming Reference do not provide significant power savings.

Using ASFs to Establish Application-Specific Total Average Power Profile

Once the baseline dynamic current specification from the *Dynamic Current* tables is obtained from the spread sheet cell associated with the CCLK frequency (f_{CCLK}) and the input voltage (V_{DD_INT}) of interest, the next step is to analyze the application to identify and apply the proper ASFs (Activity Scaling Factor). The application must be broken down into percentages of time spent in states associated with one of these standard power vectors. With knowledge of the program flow and an estimate of the percentage of time spent at each activity level, the baseline dynamic current and the corresponding ASF can be used to determine the average dynamic current consumption for each core.

For example, $I_{DD\_INT\_CCLK\_SHARC0\_DYN}$ for the SHARC+ core0 in a specific application can be calculated according to Equation 1, where "%" is the percentage of the overall time that the application spends in that state:

$I_{DD\_INT\_CCLK\_SHARC0\_DYN}$ = (% Peak activity level x $I_{DD-PEAK\_100}$ ASF x $I_{DD\_INT\_CCLK\_SHARC0\_DYN}$) +

(% High activity level x I_{DD-TYP_7030} ASF x $I_{DD\_INT\_CCLK\_SHARC0\_DYN}$) +

(% Moderate activity level x I_{DD-TYP_5050} ASF x $I_{DD\_INT\_CCLK\_SHARC0\_DYN}$) +

(% Low activity level x I_{DD-TYP_3070} ASF x $I_{DD\_INT\_CCLK\_SHARC0\_DYN}$) +

(% NOP activity level x I_{DD-NOP} ASF x $I_{DD\_INT\_CCLK\_SHARC0\_DYN}$) +

(% IDLE activity level x $I_{DD-IDLE}$ ASF x $I_{DD\_INT\_CCLK\_SHARC0\_DYN}$) +(% CCLK disabled x $I_{DD-CLOCK\_GATED}$ ASF x $I_{DD\_INT\_CCLK\_SHARC0\_DYN}$) + (% LS activity level x I_{DD-LS} ASF x $I_{DD\_INT\_CCLK\_SHARC0\_DYN}$)

Equation 1. Total Individual Core Dynamic Current

Note that the $I_{DD\_INT\_CCLK\_SHARC0\_DYN}$ output is the average current, whereas the $I_{DD\_INT\_CCLK\_SHARC0\_DYN}$ inputs are with ASF = 1.0. Consider a SHARC+ core 0 application that is continuously running and never idles, where core activity is:

- $I_{DD-PEAK\_100}$ activity level –10%
- I_{DD-TYP_7030} activity level –20%
- I_{DD-TYP_5050} activity level –50%
- I_{DD-TYP_3070} activity level –10%
- I_{DD-NOP} activity level –10%
- I_{DD-LS}, $I_{DD-IDLE}$ and $I_{DD-CLOCK\_GATED}$ activity level –0%

Applying Equation 1 to this profile yields:

$I_{DD\_INT\_CCLK\_SHARC0\_DYN}$ = (0.1 x $I_{DD\text{-}PEAK\_100}$ ASF x $I_{DD\_INT\_CCLK\_SHARC0\_DYN}$) + (0.2 x $I_{DD\text{-}TYP\_7030}$ ASF x $I_{DD\_INT\_CCLK\_SHARC0\_DYN}$) + (0.5 x $I_{DD\text{-}TYP\_5050}$ ASF x $I_{DD\_INT\_CCLK\_SHARC0\_DYN}$) + (0.1 x $I_{DD\text{-}TYP\_3070}$ ASF x $I_{DD\_INT\_CCLK\_SHARC0\_DYN}$) + (0.1 x $I_{DD\text{-}NOP}$ ASF x $I_{DD\_INT\_CCLK\_SHARC0\_DYN}$)

Estimating System Clock Tree Currents

ADSP-2159x/SC59x SHARC+® processors have multiple system clock domains to clock the system buses, various peripherals, DMA controllers, L2 memory, and a DDR controller. Each of these clock domains consumes power that dissipates in the internal power domain due to its respective clock toggling inside the chip. Additional power consumed by the peripherals and DMA (when turned on) is attributed to individual peripherals/DMAs running in the system. This power is estimated separately and added to the baseline system power when the total power profile is calculated.

There are four major system clock domains on ADSP-2159x/SC59x SHARC+® processors: SYSCLK, SCLK0, SCLK1, and DCLK.

There is also a programmable output clock (OCLK), which can be generated by one of the CGUs and routed to an external pin on the processor. It has a small influence on the overall power profile as well.

To estimate the impact to the current consumed in the V_{DD_INT} domain because of each of these system clocks, unique scaling factors are furnished in the processor data sheet. The factors represent the currents consumed per MHz per volt in each system clock domain; therefore, V_{DD_INT} is in terms of volts, and f_{xxx} is in terms of MHz in the system clock dynamic current equations:

- $I_{DD\_INT\_DCLK\_DYN}$ = 0.097 x V_{DD_INT} x f_{DCLK}
- $I_{DD\_INT\_SYSCLK\_DYN}$ = 0.651 x V_{DD_INT} x f_{SYSCLK}
- $I_{DD\_INT\_SCLK0\_DYN}$ = 0.41 x V_{DD_INT} x f_{SCLK0}
- $I_{DD\_INT\_SCLK1\_DYN}$ = 0.015 x V_{DD_INT} x f_{SCLK1}
- $I_{DD\_INT\_OCLK\_DYN}$ = 0.093 x V_{DD_INT} x f_{OCLK}

> The scaling factor for each of the system clock dynamic current equations is in units of mA/MHz/V; therefore, the result for each is in terms of mA.

Estimating DMA Contribution to Internal Dynamic Current ($I_{DD\_INT\_DMA\_DR\_DYN}$)

Different types of DMA transactions in the system result in additional power consumption:

- DMA transfers between the various memory spaces
- DMA transfers from memory to peripherals
- DMA transfers from peripherals to memory

Power consumption varies with the number of running DMA channels and the rate at which they move data through the system. To estimate DMA power consumption, three power

profiles are available in the power calculator in the *DMA/Peripheral Usage, pull-down in the VDD_INT Clock Domains & DMA Rates table on the Power Estimation tab:*

1. **HIGH**: comprised of high-speed MDMA, multiple low-speed MDMAs, and several high-speed peripheral DMAs running simultaneously in the system for a combined throughput of ~5198 MBPS.

2. **MEDIUM**: comprised of medium-speed MDMA, multiple low-speed MDMAs, and several low-speed peripheral DMAs running simultaneously in the system for a combined throughput of ~4224 MBPS.

3. **LOW**: comprised of low-speed MDMA and several low-speed peripheral DMAs running simultaneously in the system for a combined throughput of ~456 MBPS.

To estimate the DMA dynamic current ($I_{DD\_INT\_DMA\_DR\_DYN}$) in the application, the combined data bandwidth of all the DMAs running in the system determines which profile to select as the closest match to the actual application and use as the $I_{DD\_INT\_DMA\_DR\_DYN}$ component for the $I_{DD\_INT\_TOT}$ calculation.

High DMA Configuration

The following peripheral and memory DMAs are active in this configuration:

- 8 SPORTS @62.5MHz in RX mode with PRI/SEC enabled (writing data to L2)
- 8 SPORTS @62.5MHz in TX mode with PRI/SEC enabled (reading data from L2)
- SPI2/SPI1 in quad mode, SPI0 in dual mode TX operation @62.5MHz (reading data from L2)
- LP TX mode @125MHz (reading data from L2)
- 1x medium speed MDMA transferring data from L1 to L2
- 1x medium speed MDMA transferring data from L2 to L1
- 1x medium speed MDMA transferring data from DDR to L1
- 1x high speed MDMA transferring data from L1 to DDR

[1]   In this configuration, the $I_{DD\_INT\_DMA\_DR\_DYN}$ component (see the *VDD_INT DMA Usage* tab of the *power calculator*) is 240 mA.

Medium DMA Configuration

The following peripheral and memory DMAs are active in this configuration:

- 8 SPORTS @62.5MHz in RX mode with PRI/SEC enabled (writing data to L2)
- 8 SPORTS @62.5MHz in TX mode with PRI/SEC enabled (reading data from L2)
- SPI2/SPI1 in quad mode, SPI0 in dual mode TX operation @62.5MHz (reading data from L2)
- LP TX mode @125MHz (reading data from L2)
- 1x medium speed MDMA transferring data from L1 to L2
- 1x medium speed MDMA transferring data from L2 to L1

In this configuration, the $I_{DD\_INT\_DMA\_DR\_DYN}$ component (see the *VDD_INT DMA Usage* tab of the *power calculator*) is 180 mA.

Low DMA Configuration

The following peripheral and memory DMAs are active in this configuration:

- 8 SPORTS @62.5MHz in RX mode with PRI/SEC enabled (writing data to L2)
- 8 SPORTS @62.5MHz in TX mode with PRI/SEC enabled (reading data from L2)
- SPI2/SPI1 in quad mode, SPI0 in dual mode TX operation @62.5MHz (reading data from L2)
- LP TX mode @125MHz (reading data from L2)

In this configuration, the $I_{DD\_INT\_DMA\_DR\_DYN}$ component (see the V_{DD_INT} *DMA Usage* tab of the *power calculator*) is 40 mA.

> The $I_{DD\_INT\_DMA\_DR\_DYN}$ component value specified for each of the configurations above is the delta between I_{DD_INT} current measurements obtained empirically on the ADSP-2159x/SC59x SHARC+® processors evaluation platform before and after enabling the indicated DMA activity.

Estimating Accelerator Contribution to Internal Dynamic Current ($I_{DD\_INT\_ACCL\_DYN}$)

The high-performance system acceleration engines (FIR and IIR) consume some current in the V_{DD_INT} domain. The total accelerator current is defined as the sum of the current consumed by each of the blocks.

$$I_{DD\_INT\_ACCL\_DYN} = I_{DD\_INT\_ACCL\_FIR0\_DYN} + I_{DD\_INT\_ACCL\_FIR1\_DYN} + I_{DD\_INT\_ACCL\_IIR0\_DYN} +$$

$$I_{DD\_INT\_ACCL\_IIR1\_DYN} + I_{DD\_INT\_ACCL\_IIR2\_DYN} + I_{DD\_INT\_ACCL\_IIR3\_DYN} +$$

$$I_{DD\_INT\_ACCL\_IIR4\_DYN} + I_{DD\_INT\_ACCL\_IIR5\_DYN} + I_{DD\_INT\_ACCL\_IIR6\_DYN}$$

$$+ I_{DD\_INT\_ACCL\_IIR7\_DYN}.$$

For a peak FIR use case, the $I_{DD\_INT\_ACCL\_FIR\_DYN}$ current is 330mA. For a typical IIR use case, the $I_{DD\_INT\_ACCL\_IIR\_DYN}$ current is 80 mA.

Estimating Total Static Current ($I_{DD\_INT\_STATIC}$)

The static current ($I_{DD\_INT\_STATIC}$) dissipated across the entire device in the V_{DD_INT} power domain is due to transistor leakage. It is present when power is applied to the power domains, even when all the internal clocks are shut off (by gating/cutting the SYS_CLKIN to the ADSP-2159x/SC59x SHARC+® processor) and the device is held in reset. As such, static current is solely a function of junction temperature (T_J) and voltage (V_{DD_INT}). Unlike dynamic current, it does not need to be adjusted for discrete core activity levels. $I_{DD\_INT\_STATIC}$ can be obtained by looking up the value corresponding to the application conditions (such as at a specific V_{DD_INT} and T_J) in the *Static Current* table in the processor *data sheet*.

> The $I_{DD\_INT\_STATIC}$ specifications in the *Static Current* table in the data sheet are maximum specifications that account for the wafer fabrication process.

Since the static power component is constant for a given voltage and temperature, it is simply added to the total estimated dynamic current while calculating the total power consumption due to the core logic of the processor. When developing power supply and thermal relief designs, ensure that the

highest expected junction temperature and voltage is used when extracting data from the *Static Current table.*

Estimating External Power Consumption (P_{DD_EXT}, P_{DD_REF} and P_{DD_DMC})

Total external power consumption ($P_{DD\_EXT\_TOT}$, dissipated in the V_{DD_EXT} and V_{DD_DMC} power domains) depends on several parameters:

- O – number of output pins associated with the interface
- TR – toggle ratio (percentage of pins that switch any given cycle)
- f – maximum frequency at which the output pins can switch
- V_{DD_EXT} or V_{DD_DMC} – voltage swing of the output pins
- C_L – load capacitance of the output pins
- U – utilization factor (percentage of time for which peripheral is on and running)

(i) In addition to the input capacitance of each device connected to an output, the total capacitance (C_L) must include the capacitance of the processor pin (C_{OUT}), which is driving the load.

The worst-case external pin power scenario occurs when the load capacitor charges and discharges continuously. This requires the pin to toggle in each cycle in terms of external power supply, over the maximum V_{DD_EXT} voltage swing (as specified in the data sheet). The maximum switching frequency of a peripheral clock can be considered as *f*. Since the state of a data pin can change only once per clock cycle, the maximum toggling frequency in that case is *f/2*. When considering the full current profile for the V_{DD_EXT} power domain, there are several peripherals that can contribute to it; each must be considered separately and then summed together to form the single I_{DD_EXT} component of the total estimated power dissipation.

Equation 2 shows how to calculate the average external current (I_{DD_EXT}) using the above parameters:

$$I_{DD\_EXT} = O \text{ x } f \text{ x } V_{DD\_EXT} \text{ x } C_L \text{ x } U \text{ x } TR$$

Equation 2. Total External Current (I_{DD_EXT}) Calculation

Estimated average external power consumption (P_{DD_EXT}) can then be calculated as:

$$P_{DD\_EXT} = V_{DD\_EXT} \text{ x } I_{DD\_EXT}$$

Substituting from Equation 2, this calculation becomes:

$$P_{DD\_EXT} = V_{DD\_EXT}^{2} \text{ x } O \text{ x } f \text{ x } C_L \text{ x } U \text{ x } TR$$

Table1 is an excerpt from the example application use case contained on the *V_{DD_EXT} Power Domain* tab in the *Power Calculator*. It shows the Link Port interface portion to illustrate the concept more clearly.

Peripheral	Frequency in Hz (f)	Number of Output Pins (O)	Pin Capacitance in Farads (C_L)	Toggle Ratio (TR)	Utilization Factor(U)	VDD_REF current per IO (mA)	V_{DD_EXT} (V)	V_{DD_REF} (V)	P_{DD_EXT} (mow)	P_{DD_REF} (mW)	Notes
Link Port - Data pins	6.25E+07	8	3.00E-11	0.25	1.00	0.8	3.30	1.80	40.838	11.520	62.5MHz max frequency cycle, 8-bit data (8 pins @ 0.25 toggle ratio)

Table 1 VDD_EXT Power Consumption Example

As with estimating the I_{DD_EXT} current, the I_{DD_DMC} current consumption for the on-chip DDR3 controller (DMC0) can be estimated depending on the number of pins toggling and the toggle rate. V_{DD_DMC} is used for the voltage swing (obtain the maximum V_{DD_DMC} specification from the datasheet).

The *V_{DD_DMC} Power Domain* tab in the *Power Calculator* includes a table like the one referenced by Table 1. The DDR pins are grouped by function (for example, address, data, control, and clock) for the user to customize based on the application.

Estimating I/O Reference Power Consumption (P_{DD_REF})

The I/O reference supply power consumption (P_{DD_REF}) depends on the frequency of I/O switching as depicted in Table 2.

Frequency of I/O switching (MHz)	V_{DD_REF} current per I/O (mA)
Up to 32	0.4
33 to 62.5	0.8
63 to 125	1.1

Table 2 VDD_REF current per I/O

The additional contribution for the VDD_REF current is due to the internal oscillator (10 mA), One Time Programmable Memory Controller (OTPC = 18 mA) and Media Local Bus (MLB = 20 mA) which can be taken as it is for calculation purposes.

General Guidelines for Power Supply and Thermal Relief Designs

While estimating average total power associated with a given application, power supply and thermal relief designs must always consider the worst-case scenario to prevent operational failures due to the processor being operated out-of-spec because of a sagging power rail or an out-of-bounds junction temperature. The following sections provide some advice for supporting this methodology.

Power Supply Sizing

It is encouraged to follow the dos and don'ts regarding estimating the power supply sizing, given below:

DO:

- Use the maximum expected voltages associated with all the influencing power domains involved in each of the look-up tables and computations discussed throughout this EE-note

    ⓘ Power supply should be designed to remain tuned to nominal voltages throughout its lifetime

- Use the junction temperature associated with the maximum ambient temperature (T_A) that the application is expected to be subjected, for all temperature-related lookups and computations discussed throughout this EE-note
- Use the highest ASF (Activity Scaling Factor) possible for the application being run
- Calculate power dissipation from each unique voltage domain separately

DO NOT:

- Use typical I_{DD}, nominal voltage, or room temperature specifications
- Use total device power alone

Recommendations for Thermal Relief

Following recommendations can be used when evaluating thermal relief solutions.

DO:

- Use nominal voltages

    ⓘ Power supply should be designed to remain tuned to nominal voltages throughout its lifetime

- Use the junction temperature (Tj) that the processor is expected to be subjected to
- Use the Full-on-Typical (or lower) ASF (Activity Scaling Factor) to match realistic application code activity levels
- Calculate total thermal power for all voltage domains

DO NOT:

- Use typical I_{DD} specifications or room temperature when calculating thermal power
- Use maximum voltage (this is not realistic, as any transient will then exceed the maximum voltage specification)

Example Application Using the Power Calculator

This section provides an example application to illustrate how to use the *power calculator.* There are three tabs in the power calculator that contain color-coded cells along with the guidance to populate the yellow cells with the needed system settings. It lets the calculator automatically populate the green cells with either data from other tabs on the spreadsheet or with a calculated result from the user inputs. Some of the yellow cells are free form, whereas others are selectable via a pull-down. The following sections describe what user input is required on each tab to arrive at the overall power dissipation estimation.

Power Estimation Tab

The first tab in the *power calculator spreadsheet* is the *Power Estimation* tab. This is the main interface for the power calculator, where input is required to properly model the intended system. On this tab, the user must provide all the information regarding the power supplies and intended clock rates throughout the system, as well as the other influences on the overall power dissipation discussed throughout this EE-note (for example, core activity and DMA rates). This tab works in conjunction with the other tabs in the spreadsheet to provide the total power dissipation for the application as a function of all the configurable system-dependent parameters.

The default *Power Estimation* tab is pre-filled with data pertaining to the following conditions. The example application explained further is derived out of this default *Power Estimation* tab.

- ➢ Junction temperature at 125°C, to capture data at a worst-case temperature
- ➢ SHARC+ cores and A5 core running at 1GHz speed, with all other clocks at their maximum supported speeds
- ➢ A typical load profile of 70-30 considered for SHARC0 and SHARC1 (executes floating-point multiplication, addition, subtraction, and store instructions 70% of the time (30% NOPs))
- ➢ ARM A5 performs ALU operation 75% of the time (25% IDLE)
- ➢ All instances of FIR and IIR accelerators infuse at 50% on time.
- ➢ DDR in use
- ➢ DMA bandwidth considered HIGH
- ➢ Link Port, 8xSPORT, 3xSPI considered as peripherals in usage and actively consuming I/O power

ⓘ   Data for any use case/application can be generated easily by modifying the default settings and configurations.

Set the Power Domains and Junction Temperature

The first step is to set the power domains and junction temperature to the maximum levels expected by the application. For example, consider a design that utilizes the following:

- • $V_{DD\_INT} = 1.0$ V
- • $V_{DD\_EXT} = 3.3$ V
- • $V_{DD\_REF} = 1.8$ V
- • $V_{DD\_DMC} = 1.39$ V
- • $T_J = 125°C$

The V_{DD_INT} domain and T_J values are used as inputs to look-up tables on other tabs in the power calculator to extract the needed current dissipation data for the calculation. Select the values using the pull-down menus in the *Operating Conditions* table on the *Power Estimation* tab based on the discrete levels defined in the *Static* and *Dynamic Current* tables in the processor datasheet.

The *Static* and *Dynamic Current* tables included in the power calculator are from the referenced processor *data sheet*. Always verify that the data in the calculator matches with the data in the current data sheet to ensure that the proper specifications are being included.

Configure the other relevant power domains on the *Power Estimation* tab. Manually input the appropriate values for the V_{DD_EXT} (in the *V_{DD_EXT}* section), V_{DD_REF} (in the *V_{DD_REF}* section) and V_{DD_DMC} (in the *V_{DD_DMC}* section) domains into the relevant yellow cells. The calculator computes the current and/or power in the associated green cells.

There is no error-checking built into the calculator for the range of these power domains. A *Configuration Warning* is associated with each of these yellow cells indicating that the values input must be verified by referring the processor data sheet.

The $V_{DD\_EXT,}$ V_{DD_REF} and V_{DD_DMC} cells are influenced by activity on the *V_{DD_EXT} & V_{DD_REF} Power* and *V_{DD_DMC} Power* tabs, respectively.

Set the Clocks

Input all the clocking information that defines the dynamic currents expected throughout the system. For example, consider a design that utilizes the following:

- f_{CCLK_SHARC0}= 1000 MHz

- f_{CCLK_SHARC1}= 1000 MHz

- f_{CCLK_A50}= 1000 MHz
- f_{DCLK} = 800 MHz
- f_{SYSCLK} = 500 MHz
- f_{SCLK0} = 125 MHz
- f_{SCLK1} = 333 MHz
- f_{OCLK} = 125 MHz

Manually input the values into the corresponding yellow cells in the *Clock Domains & DMA Rates* table. The calculator computes the associated dynamic current in the adjacent green cells.

There is no error-checking built into the calculator for the range of these operating frequencies. A *Configuration Warning* is associated with each of these yellow cells indicating that the values input must be verified by referring the processor data sheet.

Set the Activity Scaling Factors (ASFs)

As discussed, ***Using ASFs to Establish Application-Specific Total Average Power Profile***, analyze the application and determine the core loads to associate with the application. This step establishes the dynamic power dissipation component for each core, which is handled in the yellow cells in the *COREx Average ASF* tables in the *V_{DD_INT}* section of the *Power Estimation* tab. The proper input for these cells is a fractional number from 0.0 to 1.0 indicating the percentage of time spent by the application at that discrete ASF level. The calculator outputs the *Average ASF* (as described by Equation 1) in the green cell based on the data on the *Core Activity Factors* tab.

There is no error-checking built into the calculator for the sum of these percentages. A hover message indicating that the "*Sum of these fractions should be 1*" appears, to advise the user when inputting data in this section.

The *ASF* tables included in the power calculator are from the referenced processor *data sheet.* Always verify that the data in the calculator matches with the data in the current data sheet to ensure that the proper specifications are being included.

A power supply design should use a maximum power dissipation profile accounting for the worst-case scenario. However, to establish an average power profile, the calculator is built to account for all the discrete ASF levels defined by *data sheet*. The yellow cells can be populated to reflect the actual system model.

For example, after analyzing the application, it is determined that the following describes the core activity levels:

- SHARC+ Core 1: 100% typical application (70-30 profile)
- SHARC+ Core 2: 100% typical application (70-30 profile)
- ARM A5 Core 0: 100% typical application (75-25 profile)

While providing input to the calculator, the corresponding average ASFs are computed as follows:

- $ASF_{SHARC0}=1.00$
- $ASF_{SHARC1}=1.00$
- $ASF_{A5}=1.00$

The ASF is then used by the calculator to compute the dynamic current component in the green cells in the *Contribution (mA)* column, in the *Clock Domains & DMA Rates* table.

Set the Accelerator Resource Usage

The system accelerator engines (FIR, IIR) dissipate dynamic power in the V_{DD_INT} domain. This is as part of the total internal dynamic current ($I_{DD\_INT\_TOT}$) equation in the 'Total internal power dissipation' section of processor *data sheet*. This power is mentioned in the *V_{DD_INT}* section of the *Power Estimation* tab in a series of yellow cells in the *Resource Usage* table. These yellow cells should be written with the percentage of time for which each instance of FIR or IIR is active. 50% active time is selected by default. The selectable mode options for each row provide a look-up value into associated tables on *V_{DD_INT} Accelerators* in the calculator.

Only the *Peak usage* setting is available, as discussed in Estimating Accelerator Contribution to InternalDynamic Current ($I_{DD\_INT\_ACCL\_DYN}$).

For example, if all instances of FIR and IIR at 50% active time, are being used, then

$$I_{DD\_INT\_ACCL\_DYN} = 165mA + 165mA + 80mA + 80mA + 80mA + 80mA + 80mA + 80mA + 80mA + 80mA = 970mA.$$

Select Appropriate DMA Activity Level

The final user input required on the *Power Estimation* tab is the *DMA/Peripheral Usage* row in the *Clock Domains & DMA Rates* table in the V_{DD_INT} section. It is here that the user must select from the three defined profiles discussed in Estimating DMA Dynamic Current ($I_{DD\_INT\_DMA\_DR\_DYN}$) (HIGH, MEDIUM, or LOW) as the closest match to the data activity in the system. When selected using the yellow pull-down, the corresponding look-up value from the $I_{DD\_INT\_DMA\_DR\_DYN}$ column on the V_{DD_INT} *DMA Usage* tab is populated in the corresponding green cell in the *Contribution (mA)* column.

When considering serial peripherals, along with DDR access and additional MDMA, a HIGH profile is selected (5198 MBPS). The value for DMA contribution is:

$$I_{DD\_INT\_DMA\_DR\_DYN} = 240 \text{ mA}$$

V_{DD_EXT} & V_{DD_REF} Power Domain Tab

The V_{DD_EXT} & V_{DD_REF} Power Domain tab is used to calculate the contribution to power from the Link Ports, SPORTs, and SPI peripherals.

Calculating V_{DD_EXT} Power

Using the V_{DD_EXT} & V_{DD_REF} *Power Domain* tab, identify:

- Each V_{DD_EXT} power domain peripheral that is in use in the system, modelling its power profile as a function of how often it is active
- How many pins switch
- The load capacitance associated with the pins
- The voltage swing on the pins
- The frequency at which the pins can switch

Similar to the case with the *Power Estimation* tab, the yellow cells are those requiring user input, and the green cells are those populated by the calculator.The $V_{DD\ EXT}$ column is automatically populated from the *Power Estimation* tab; the user must fill in all the yellow cells. Consider an application that uses the Link Port, eight serial ports (SPORTs) and three SPIs. For a rough estimation, external frame syncs for SPORTs and low slave selects for SPIs are considered. Most of the columns are easy to populate with the appropriate clock frequencies. However, some frequency areas function depending on how the peripheral is configured: the pin capacitance from the design, and the application's use of the peripheral (see Estimating External Power Consumption(PDD_EXT and PDD_DMC)), the *Number of Output* pins and the *Utilization Factor*.

With the above peripheral configuration information, Table 3 could represent such a system after the user:
- inputs the proper number of output pins (O)
- makes a reasonable guess of the number of pins switching in any given cycle (TR)
- populates the frequency (f) and load capacitance (C_L), and then
- supplies information about the percentage of the time the peripheral is enabled (U)

Peripheral	Frequency in Hz (f)	Number of Output Pins (O)	Pin Capacitance in Farads (C$_L$)	Toggle Ratio (TR)	Utilization Factor (U)	VDD_REF current per IO (mA)	V$_{DD\_EXT}$ (V)	V$_{DD\_REF}$ (V)	P$_{DD\_EXT}$ (mW)	P$_{DD\_REF}$ (mW)	Notes
Link Port - Data pins	6.25E+07	8	3.00E-11	0.25	1.00	0.8	3.30	1.80	40.838	11.520	62.5MHz max frequency cycle, 8-bit data (8 pins @ 0.25 toggle ratio)
Link Port - Clock	1.25E+08	1	3.00E-11	1	1.00	1.1	3.30	1.80	40.838	1.980	125Mhz operation
SPORT0-7 -Data pins	3.13E+07	16	3.00E-11	0.25	1.00	0.4	3.30	1.80	40.838	11.520	31.25MHz max frequency cycle, 2 pins per SPORT x 8 (16 pins @ 0.25 toggle ratio)
SPORT0-7 - Clock	6.25E+07	8	3.00E-11	1	1.00	0.8	3.30	1.80	163.350	11.520	62.5Mhz operation
SPI2 - Data pins	3.13E+07	4	3.00E-11	0.25	1.00	0.4	3.30	1.80	10.209	2.880	31.25MHz max frequency cycle, Quad mode (4 pins @ 0.25 toggle ratio)
SPI2 - Clock	6.25E+07	1	3.00E-11	1	1.00	0.8	3.30	1.80	20.419	1.440	62.5Mhz operation
SPI1 - Data pins	3.13E+07	4	3.00E-11	0.25	1.00	0.4	3.30	1.80	10.209	2.880	31.25MHz max frequency cycle, Quad mode (4 pins @ 0.25 toggle ratio)
SPI1- Clock	6.25E+07	1	3.00E-11	1	1.00	0.8	3.30	1.80	20.419	1.440	62.5Mhz operation
SPI10- Data pins	3.13E+07	2	3.00E-11	0.25	1.00	0.4	3.30	1.80	5.105	1.440	31.25MHz max frequency cycle, Dual mode (2 pins @ 0.25 toggle ratio)
SPI0- Clock	6.25E+07	1	3.00E-11	1	1.00	0.8	3.30	1.80	20.419	1.440	62.5Mhz operation

Total External Power Dissipation (mW)	372.64
Total VREF Dissipation (mW)	89.460

Table 3. Example VDD_EXT Peripheral Usage

The P_{DD_EXT} *(mW)* column contains the results of the calculator applying Equation 2 to the input data in the other columns. The sum of the power contributions from each of the individual peripheral components is calculated at the bottom of the column. Peripherals can be added or deleted from this profile by inserting or removing rows.

Calculating VDD_REF Power

The V$_{DD\_REF}$ power is automatically calculated in the same spreadsheet as V$_{DD\_EXT}$ power, since both are related to I/O switching of peripherals. The calculation is done by referring to Table 4 for each I/O pin.

Frequency of I/O switching (MHz)	VDD_REF current per IO (mA)
Up to 32Mhz	0.4
From 33Mhz to 62.5Mhz	0.8
From 63Mhz to 125Mhz	1.1

Table 4. I/O VREF Current for PDD_REF Calculation

VDD_DMC Power Domain Tab

The V_{DD_DMC} *Power Domain* tab must be used when using DDR in the application. The concepts from V$_{DD\_EXT}$ Power Domain Tab apply to this tab as well. However, the table is slightly different because it is modeling a single interface that has numerous groups of pins that need to be treated differently based on factors that do not remain consistent across the interface. Similar to the V_{DD_EXT} *Power Domain* tab, there are green cells that are either populated by the calculator from elsewhere or are the output of a computation. The user must populate the yellow cells with information regarding the configuration of the DDR controller.

As for the green cells on the *V$_{DD\_DMC}$ Power Domain* tab, the power supply information for the *V$_{DD\_DMC}$ (V)* column is automatically extracted from the *Power Estimation* tab, as is the *Frequency in Hz (f)* column. Note that the calculator automatically applies the f$_{DCLK}$ rate to the clock (*CLK*) and *Address pins [15:0]* rows, as these pins can switch at this rate in a worst-case scenario.

As indicated in Set the Clocks, the DDR clock was configured to 800 MHz on the *Power Estimation* tab. Therefore, Table 5 could be an example model for the DDR interface for this application after the pin capacitance and other inputs are finalized by the user.

Peripheral		Frequency in Hz (f)	Number of Output Pins (O)	Pin Capacitance in Farads (C$_L$)	Toggle Ratio (TR)	Utilization (U)	V$_{DDDR}$ (V)	Pout (mW)	Reasoning
DDR3L	Address pins [15:0]	4.00E+08	16	5.00E-12	0.25	1.00	1.39	15.46	DCLK_FREQ operation; Worst case execution --> State of pin changes roughly every one fourth max frequency cycle (toggle ratio: 0.5)
	Data pins [15:0]	8.00E+08	16	5.00E-12	1	1.00	1.39	123.65	2x DCLK_FREQ operation, Assume DDR configured for write operation; Worst case execution --> State of pin changes twice every clock cycle (toggle ratio:1)
	CTRL	4.00E+08	15	5.00E-12	0.25	1.00	1.39	14.49	DCLK_FREQ/Burst Mode operation, Assume DDR configured for write operation; Worst case execution --> State of pin changes roughly every one fourth max frequency cycle (toggle ratio:0.25)
	CLK	8.00E+08	2	5.00E-12	1	1.00	1.39	15.46	DCLK_FREQ operation; Clk and the differential clock signal ; Worst case execution --> State of pin changes twice every clock cycle (toggle ratio:1)

Table 5. Example V$_{DD\_DMC}$ Use Case

Because typical DDR accesses are sequential in nature, it is unlikely that the number of address pins toggling any maximum frequency cycle would exceed 25% (four pins). The worst-case model assumes the interface is always running (U = 1.00). For average power dissipation, there could be low-power modes employed, making a fractional *Utilization Factor* possible, which is supported by the calculator.

Summarizing the Process of Estimating Power

Use the following steps as an example to estimate total overall power in an ADSP-2159x/SC59x SHARC+® processor design.

Step 1: Obtain the Internal Static Current Component (I$_{DD\_INT\_STATIC}$)
Use the maximum power rail (V$_{DD\_INT}$) and junction temperature (T$_J$) values for the application to look up the appropriate maximum I$_{DD\_INT\_STATIC}$ specification from the *Static Current* table in the processor *data sheet*. In the example discussed in Set the Power Domains and Junction Temperature, V$_{DD\_INT}$ = 1.0 V and T$_J$ = 125 °C; therefore, the associated value from the *V$_{DD\_INT}$ Maximum Static Current* tab is 2551 mA.

Step 2: Obtain Baseline Core Dynamic Currents (IDD_INT_CCLK_A5_DYN, IDD_INT_CCLK_SHARC1_DYN, IDD_INT_CCLK_SHARC2_DYN)
Use the same V$_{DD\_INT}$ power rail and the expected core clock frequency (f$_{CCLK}$) to look up the appropriate values in the *Dynamic Current* tables in the processor *data sheet* for each core. In the example discussed in Set the Clocks, V$_{DD\_INT}$ = 1.0 V and the core is running at 1000 MHz; therefore, the associated values from the equations in Core Dynamic Current

(also in the *Dynamic Current* data sheet table) are:

- $I_{DD\_INT\_CCLK\_SHARCx\_DYN} = 0.701 \times V_{DD\_INT} \times f_{CCLK\_SHARCx} \rightarrow 0.701 \times 1.0 \times 1000 = 701$ mA

- $I_{DD\_INT\_CCLK\_A5\_DYN} = 0.15 \times V_{DD\_INT} \times f_{CCLK\_A5} \rightarrow 0.11 \times 1.0 \times 1000 = 110$ mA

Step 3: Model Application to Establish Activity Scale Factors (ASF$_{SHARC0}$)

Using the definitions of the scale factors in the *Activity Scaling Factors* tables in the *data sheet*., model the application for each core to determine the processor load because of the code being executed. For a maximum calculation, use the worst-case ASF at any given time. Calculate an average ASF, as described in the *Using ASFs* section. From the example provided in Set the Activity Scaling Factors (ASFs):

- $ASF_{SHARC0} = 1.00$

- $ASF_{SHARC1} = 1.00$

- $ASF_{A5} = 1.00$

Step 4: Apply ASFs to Core Dynamic Components

Apply the calculated average ASF or the worst-case ASF to the core dynamic component for each core as a simple multiplication:

- $I_{DD\_INT\_CCLK\_SHARC0\_DYN} = I_{DD\_INT\_CCLK\_SHARC0\_DYN} \times ASF_{SHARC0} \rightarrow 701 \times 1.00 = 701$ mA

- $I_{DD\_INT\_CCLK\_SHARC1\_DYN} = I_{DD\_INT\_CCLK\_SHARC1\_DYN} \times ASF_{SHARC1} \rightarrow 701 \times 1.00 = 701$ mA

- $I_{DD\_INT\_CCLK\_A5\_DYN} = I_{DD\_INT\_CCLK\_A5\_DYN} \times ASF_{A5} \rightarrow 110 \times 1.00 = 110$ mA

Step 5: Calculate the System Clock Tree Core Dynamic Currents

The dynamic current dissipated in the V_{DD_INT} domain because of the clocks toggling inside the processor are a function of the internal voltage (in Volts) and the frequency of each clock (in MHz), as governed by the equations in the processor *data sheet*. Using the example from Estimating System Clock Tree Currents:

- $I_{DD\_INT\_DCLK\_DYN} = 0.097 \times f_{DCLK} \times V_{DD\_INT} \rightarrow 0.097 \times 800 \times 1.0 = 77.60$ mA
- $I_{DD\_INT\_SYSCLK\_DYN} = 0.651 \times f_{SYSCLK} \times V_{DD\_INT} \rightarrow 0.651 \times 500 \times 1.0 = 325.50$ mA
- $I_{DD\_INT\_SCLK0\_DYN} = 0.41 \times f_{SCLK0} \times V_{DD\_INT} \rightarrow 0.41 \times 125 \times 1.0 = 51.25$ mA
- $I_{DD\_INT\_SCLK1\_DYN} = 0.015 \times f_{SCLK1} \times V_{DD\_INT} \rightarrow 0.015 \times 333.3 \times 1.0 = 5.00$ mA
- $I_{DD\_INT\_OCLK\_DYN} = 0.093 \times f_{OCLK} \times V_{DD\_INT} \rightarrow 0.093 \times 125 \times 1.0 = 11.63$ mA

Step 6: Choose a DMA Profile to Obtain Core Dynamic DMA Current (I$_{DD\_INT\_DMA\_DR\_DYN}$)

Calculate the total system DMA bandwidth during peak activity and select the profile that is the closest match. The example in Select Appropriate DMA Activity Level sets the DMA profile to HIGH, therefore:

- $I_{DD\_INT\_DMA\_DR\_DYN} = 240$ mA

Step 7: Account for Core Dynamic Currents from Accelerator Blocks (I$_{DD\_INT\_ACCL\_DYN}$)

Each of these blocks dissipates power in the V_{DD_INT} domain and must be considered when estimating the total core dynamic current. The example discussed in Set the Peripheral

Resource Usage has the system acceleration engine enabled, therefore:

- $I_{DD\_INT\_ACCL\_DYN} = 650$ mA

Add the static internal current (Step 1) component to the sum of all the dynamic internal current components (Step 4 through Step 7) to get the total current in the V_{DD_INT} domain ($I_{DD\_INT\_TOT}$):

$$I_{DD\_INT\_TOT} = I_{DD\_INT\_STATIC} + I_{DD\_INT\_CCLK\_SHARC0\_DYN} + I_{DD\_INT\_CCLK\_SHARC1\_DYN} +$$
$$I_{DD\_INT\_CCLK\_A5\_DYN} + I_{DD\_INT\_DCLK\_DYN} + I_{DD\_INT\_SYSCLK\_DYN} +$$
$$I_{DD\_INT\_SCLK0\_DYN} + I_{DD\_INT\_SCLK1\_DYN} + I_{DD\_INT\_OCLK\_DYN} +$$
$$I_{DD\_INT\_ACCL\_DYN} + I_{DD\_INT\_DMA\_DR\_DYN}$$

$I_{DD\_INT\_TOT} = 2551.00 + 701.00 + 701.00 + 110.00 + 77.60 + 325.00 + 51.25 + 5.00 + 11.63 + 650.00 + 240 = 5423.48$ mA

With the total $I_{DD\_INT\_TOT}$ current calculated, estimate the total power ($P_{DD\_INT\_TOT}$):

- $P_{DD\_INT\_TOT} = I_{DD\_INT\_TOT}$ x V_{DD_INT} → 5423.97 mA x 1.0 V = 5423.97 mW

The total external power dissipation ($P_{DD\_EXT\_TOT}$) is comprised of the power dissipated in each of the two critical power domains (V_{DD_EXT}, V_{DD_DMC}) as well as from V_{DD_REF} domain.

Calculate Power Dissipated in the V_{DD_EXT} and V_{DD_REF} Domain (P_{DD_EXT} & P_{DD_REF})

Model the application using the concepts discussed in Estimating External Power Consumption (PDD_EXT and PDD_DMC)) to estimate the power dissipated in the V_{DD_EXT} domain (P_{DD_EXT}) and V_{DD_REF} domain (P_{DD_REF}). From the example discussed in V_{DD_EXT} & V_{DD_REF} Power Domain Tab:

- $P_{DD\_EXT} = 372.64$ mW
- $P_{DD\_REF} = 89.460$ mW

Calculate Power Dissipated in the V_{DD_DMC} Domain (P_{DD_DMC})

Model the application using the concepts discussed in Estimating External Power Consumption (PDD_EXT and PDD_DMC)) to estimate the power dissipated in the V_{DD_DMC} domain (P_{DD_DMC}). From the example discussed in V_{DD_DMC} Power Domain Tab:

- $P_{DD\_DMC} = 169.06$ mW

Finally, with all the core and system elements properly modelled, calculate the total power dissipation as the sum of the internal ($P_{DD\_INT\_TOT}$) and external ($P_{DD\_EXT\_TOT}$) power dissipation components:

$$P_{DD\_EXT\_TOT} = P_{DD\_EXT} + P_{DD\_REF} + P_{DD\_DMC}$$

- $P_{DD\_TOT} = P_{DD\_INT\_TOT} + P_{DD\_EXT\_TOT} \rightarrow 5423.97 + 372.64 + 89.46 + 169.06 = 6055$ mW
  $=\sim 6.055W$

> Due to rounding in the calculations in the example, the values output in the green cells of the power calculator may differ slightly from those presented.

References

[1] ADSP-21594/ADSP-SC591/SC592/SC594: SHARC+ Dual-Core DSP with Arm Cortex-A5 Preliminary Data Sheet (Rev. PrE), August 2021. Analog Devices, Inc.

[2] ADSP-2159x_SC59x_Power_Calculator_Tool_Rev00

[3] ADSP-21591/21593: SHARC+ Dual-Core DSP with Arm Cortex-A5 Data Sheet (Rev. 0), August 2021. Analog Devices, Inc.

[4] EE-414: Estimating Power for ADSP-2156x SHARC+ Processors Rev. 1, March 2021. Analog Devices, Inc.

[5] ADSP-2159x/ADSP-SC591/592/594 SHARC+ Processor Hardware Reference, August 2021. Analog Devices, Inc.

[6] SHARC+ Core Programming Reference. Revision 1.4, May 2021. Analog Devices, Inc.

Document History

Revision	Description
Rev 1 – April 14, 2022 *by Deepak SH*	Initial Release.