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Recommendations for Compatible Design Between ADSP-21593 and ADSP-21834/21835 Processors

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Introduction

This EE note provides recommendations to design a printed circuit board (PCB) that is compatible between ADSP-21593 and ADSP-21834/21835 processors. The note aids customers in understanding the difference between the pinouts of the processors and design recommendations for various I/O pins. It also discusses some of the reference implementation of compatible schematic design.

Pin Compatibility Between ADSP-21593 and ADSP-21834/21835 Processors

The ADSP-21834/21835 processors are designed to be pin compatible with the ADSP-21593 processor. Most pins share a common functionality between these DSP products, but there are several pins which provide additional features in the ADSP-21834/21835 processors. Table 1 shows the list of such pins to pay attention to when designing the compatible PCB.

Table 1. Pin Comparison Between ADSP-21593 and ADSP-21834/21835 Processors

Ball No.	ADSP-21593 Processor	ADSP-21834/21835 Processors	Additional Functions ADSP-21834/21835 Processors
N05	VDD_REF	VDD_FPLLANA	Fractional PLL Supply Voltage
N03	PA_00/SPI2_MISO/ OSPI0_MISO	PA_00/SPI2_MISO/xSPI_MISO/PWM0_AH	PWM0_AH
P03	PA_01/SPI2_MOSI/ OSPI0_MOSI	PA_01/SPI2_MOSI/xSPI_MOSI/PWM0_AL	PWM0_AL
R01	PA_04/SPI2_CLK/ OSPI0_CLK	PA_04/SPI2_CLK/xSPI_CLK/PWM0_BH	PWM0_BH
T02	PA_05/SPI2_SEL1/ OSPI0_SEL1/$\overline{\text{SPI2_SS}}$	PA_05/SPI2_SEL1/xSPI_SEL1/ FRACNPLL_FLOCK/$\overline{\text{SPI2_SS}}$	FRACNPLL_FLOCK
V05	PB_06/LP0_CLK/SPI1_SEL5/ TRACE0_CLK	PB_06/LP0_CLK/SPI1_SEL5/PWM0_BL/ TRACE0_CLK	PWM0_BL

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Ball No.	ADSP-21593 Processor	ADSP-21834/21835 Processors	Additional Functions ADSP-21834/21835 Processors
Y03	PB_10/LP0_D3/SPI1_SEL2/ TRACE0_D03	PB_10/LP0_D3/SPI1_SEL2/PWM0_CH/ TRACE0_D3	PWM0_CH
Y04	PB_11/LP0_D4/SPI0_RDY/ UART2_RX/TM0_ACI02	PB_11/LP0_D4/SPI0_RDY/PWM0_CL/ UART2_RX/TM0_ACI02	PWM0_CL
V07	PB_12/LP0_D5/SPI2_SEL3/ UART2_TX	PB_12/LP0_D5/SPI2_SEL3/PWM0_DH/ UART2_TX	PWM0_DH
Y14	PB_14/LP0_D7/SPI0_SEL3/ UART2_CTS	PB_14/LP0_D7/SPI0_SEL3/PWM0_DL/ UART2_CTS	PWM0_DL
Y17	PC_04/LP1_D5/OSPI0_SEL2	PC_04/LP1_D5/xSPI_SEL2/PWM0_SYNC	PWM0_SYNC
W17	PC_06/LP1_D7/SPI1_RDY	PC_06/LP1_D7/SPI1_RDY/$\overline{\text{PWM0_TRIP}}$	$\overline{\text{PWM0_TRIP}}$

Table 2. ADSP-21834/21835 Pins with Additional Functions

Ball No.	Ball Name	Additional Function	Description
N05	VDD_FPLLANA	Fractional PLL Supply Voltage	Analog VDD for Frac-N PL. VDD_REF can be used to source VDD_FPLLANA. For lower noise on VDD_FPLLANA, filtering on VDD_REF is recommended before connecting to VDD_FPLLANA.
N03	PA_00	PWM0_AH	Channel A High Side. High-side drive signal
P03	PA_01	PWM0_AL	Channel A Low Side. Low-side drive signal
R01	PA_04	PWM0_BH	Channel B High Side. High-side drive signal
T02	PA_05	FRACNPLL_FLOCK	Frac PLL Lock
V05	PB_06	PWM0_BL	Channel B Low Side. Low-side drive signal
Y03	PB_10	PWM0_CH	Channel C High Side. High-side drive signal
Y04	PB_11	PWM0_CL	Channel C Low Side. Low-side drive signal
V07	PB_12	PWM0_DH	Channel D High Side. High-side drive signal
Y14	PB_14	PWM0_DL	Channel D Low Side. Low-side drive signal
Y17	PC_04	PWM0_SYNC	PWMTMR Grouped. This input is for an externally-generated sync signal. If the sync signal is internally generated, no connection is necessary.
W17	PC_06	$\overline{\text{PWM0_TRIP}}$	Shutdown Input n. When asserted, the selected PWM channel outputs are shut down immediately.

Below are recommendations to follow when designing a compatible circuit between the ADSP-21593 and ADSP-21834/21835 processors.

N05 Pin: Connect to 1.8 V supply voltage.

- VDD_REF in ADSP-21593
- VDD_FPLLANA in ADSP-21834/21835

When using ADSP-21834/21835 processors, it is recommended to add a filtering network to achieve lower noise on the VDD_FPLLANA pin before connecting the 1.8 V power rail to VDD_FPLLANA, as shown in Figure 1. If FPLL is not used in the ADSP-21834/21835 processors, pin N05 can be directly connected to the VDD_REF supply voltage.

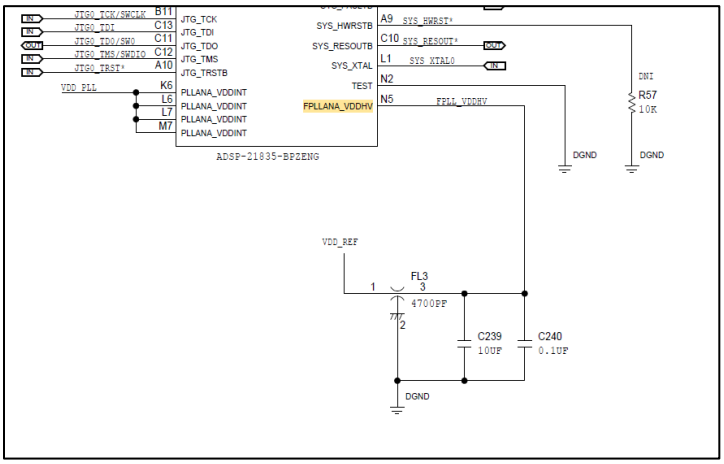


Figure 1. Implementation of Filter Network for the VDD_FPLLANA Pin

When using the ADSP-21593 processor, the filter/ferrite bead (FL3) shown in Figure 1 can be replaced with a 0Ω resistor and the capacitors (C239 and C240) can be depopulated.

N03, P03, R01, V05, Y03, Y04, V07, Y14, Y17, and W17 Pins: These pins support an additional PWM feature on the ADSP-21834/21835 processors as described in Table 2.

To use a PWM feature of the ADSP-21834/21835 processors while still maintaining the compatible PCB design, it is suggested to use a 0Ω resistor option to connect the PWM pins to interfacing devices (Figure 2).

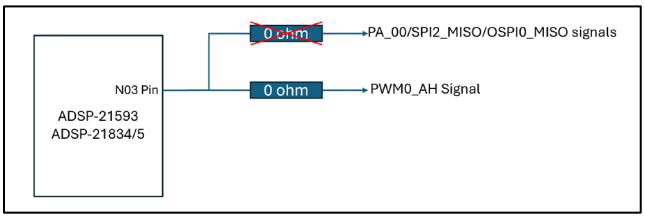


Figure 2. 0Ω Option to use PWM Function of the ADSP-21834/21835 Processors

Another option is to use a multiplexer IC to switch between the ADSP-21834/21835 PWM function and other common functions of the processor as shown in Figure 3.

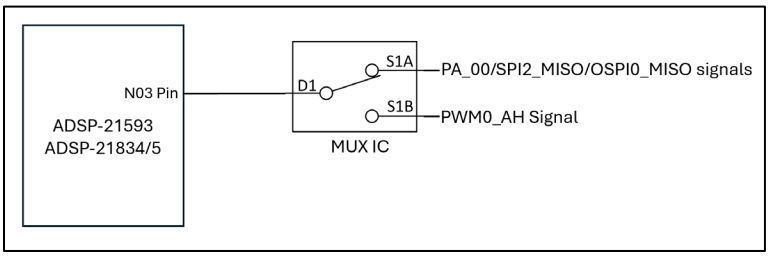


Figure 3. MUX Option to Use PWM Function of the ADSP-21834/21835 Processors

T02 Pin: FRACNPLL_FLOCK is an output to indicate FPLL Frequency lock interrupt. When using the ADSP-21593 processor, this pin can be treated as any other GPIO pin with other functions.

Boot Mode Port Difference (001 SPI Flash)

The processors have several mechanisms for automatically loading internal and external memory after a reset. The boot mode is defined by the SYS_BMODE[n] input pins. There are two categories of boot modes. In flash boot modes, the processors actively load data from serial memories. In external host boot modes, the processors receive data over a serial interface from an external host device.

When SPI flash boot mode is selected (SYS_BMODE[n] = 001), the default boot port differs between the processors: the ADSP-21593 processor boots from SPI2 (Figure 4), whereas the ADSP-21834/21835 processor boots from SPI1 (Figure 5). For a single PCB that supports either processor, provide a means to route the SPI boot flash device traces to the SPI1 or SPI2 port pins, based on the processor installed.

SYS_BMODE[n] Setting	Boot Mode
000	No boot
001	SPI2 flash
010	External SPI2 host
011	External UART0 host
100	External LP0 host
101	Octal SPI flash
110	Reserved

Figure 4. Boot Setting for ADSP-21593

SYS_BMODE[n] Setting	Boot Mode
000	No boot
001	SPI1 flash
010	External SPI2 host
011	External UART0 host
100	External LP0 host
101	xSPI flash
110	Extended LP0 host
111	Reserved

Figure 5. Boot Setting for ADSP-21834/21835

Summary

This EE note provides guidance for designing a PCB compatible with both ADSP-21593 and ADSP-21834/21835 processors. The note highlights the pin differences, boot mode port difference, and added PWM and fractional PLL functions in the ADSP-21834/21835 processors, as well as suggests circuit options such as filtering networks and multiplexers to maintain compatibility while utilizing these features.

References

[1] *https://www.analog.com/media/en/technical-documentation/data-sheets/adsp-2183x-adsp-sc83x.pdf*

[2] *https://www.analog.com/media/en/dsp-documentation/processor-manuals/adsp-2183x-adsp-sc83x-hrm.pdf*

[3] *https://www.analog.com/media/en/technical-documentation/eval-board-schematic/adsp21835w-ev-som-schem.pdf*

[4] *https://www.analog.com/media/en/technical-documentation/data-sheets/adsp-21593-21594-adsp-sc592-sc594.pdf*

[5] *https://www.analog.com/media/en/dsp-documentation/processor-manuals/adsp-2159x-sc591-592-594-hrm.pdf*

[6] *https://www.analog.com/media/en/technical-documentation/eval-board-schematic/ev-21593-som-schematic.pdf*

Document History

Revision	Description
Rev 1 – October 29, 2026 *by Shivakumar Puran*	Initial Release